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Current Source Gate Driver for dV/dt Testing of SiC Power Devices

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Summary

A current source gate driver circuit for testing the switching transient ruggedness of 1.2 kV SiC power semiconductor devices has been designed. This method can charge the internal parasitic capacitors quickly in order to attain high slew rates. This gate driver is incorporated into a Double Pulse Test (DPT) setup in order to test the devices at various power levels. In the simulation provided, a device model from Vendor E, with ratings of 1.2 kV and 90 A, is used to show that this setup can attain up to 800 kV/µs. A comparison of these simulations and experimental results is also explored.

Motivation

While Silicon Carbide (SiC) power semiconductor devices have pushed toward maturity and increased use in industrial applications, there are still reliability issues that need to be examined. A multitude of research has occurred in the areas of short-circuit withstand[1], body diode degradation[2], device lifetime[3], and gate oxide reliability[4], but the dV/dt failure has received less attention. The slew rate, dV/dt, capability indicates the ruggedness of the device during switching transients. Understanding the potential of these devices will enable opportunities for applications to push to even higher switching frequencies based on the well-known advantages of SiC MOSFETs. Therefore, the effects of high dV/dt must be tested in order to determine the Safe Operating Area (SOA) in terms of slew rate with relation to other device characteristics.

Preliminary Results

The final testing schematic and gating operation are shown in Fig. 1. This setup will be referred to as the Double-DPT, and the components of the experimental setup are given in Table 1. This configuration, similar to the concepts of a DPT, enables a build-up of gate and drain currents while limiting the maximum gate voltage to the Device Under Test (DUT).

The proposed method, used to incur a variable slew rate, was simulated in LTSpice using a DUT from Vendor E with ratings of 1.2 kV and 90 A. In this simulation shown in Fig. 2, all values are given as in Table 1 with a sweep of L_1 and L_2 to vary the gate and drain currents.

An experimental setup has been built for testing, as shown in Fig. 3(a). The DUT in the Double-DPT circuit is driven by the current source gate drive. The gating signals for *S1* and *S2* have been coded using a TI eZdspF28335 with optical isolation. The resulting waveforms are given in Fig. 3(b). Updates, including PCB design and adding a negative gate bias, are being completed for this hardware to avoid false turn-on occurrences as shown from a previous design.

With the hardware in place, the next step for this research is to experimentally test Vendor E devices. There will be a total of 5 devices tested to see the variation in a small population. The V_{ds} voltage will be increased incrementally until the device fails or the rated voltage of the device is attained. The same will also be done by varying the currents, I_g and I_d. After testing the devices, the experimental and simulated results will be compared for model limitations. The SOA, in terms of dV/dt capability, will be defined using the data collected from these tests.

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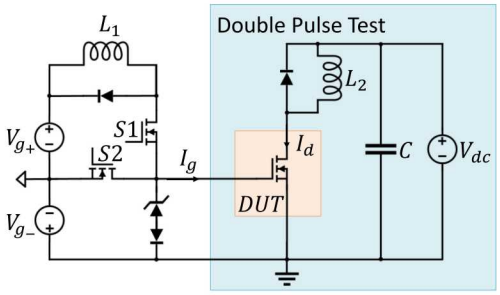
[1]Y. Zhou *et al.*, "Short–Circuit failure model of SiC MOSFET including the interface trapped charges," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, 2019.

[2]M. Kang *et al.*, "Body Diode Reliability of Commercial SiC Power MOSFETs," *2019 WiPDA*, 2019.

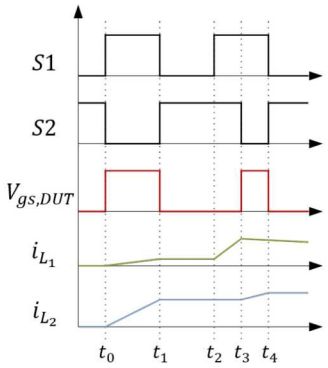
[3]Z. Ni *et al.*, "Overview of real-time lifetime prediction and extension for SiC power converters," *IEEE Trans. Power Electron.*, 2019.

[4]K. Puschkarsky *et al.*, "Review on SiC MOSFETs High-Voltage device reliability focusing on threshold voltage instability," *IEEE Trans. Electron Devices*, vol. 66, no. 11, 2019.

Figures



(a) Schematic.

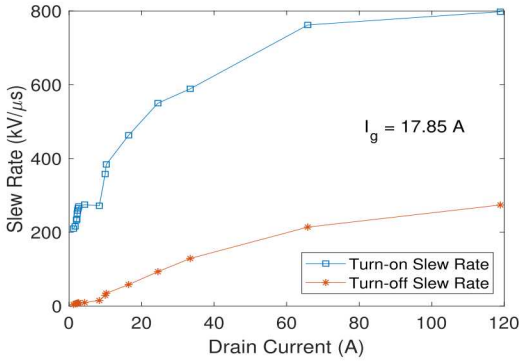


(b) Gating and current waveforms.

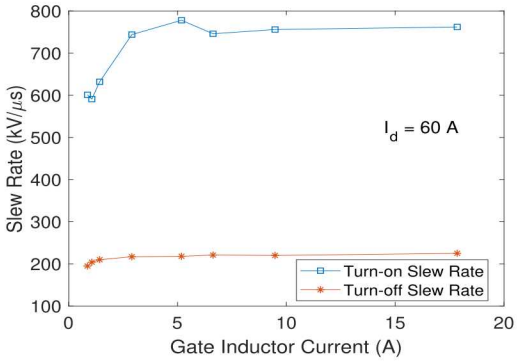
Table 1: Experimental Setup Double-DPT Components

Component	Value
V_{g+}	25 V
V_{g-}	5 V
L_1	1 µH
V_{dc}	800 V
L_2	360 µH
C	0.2 µF

Fig. 1: Double-Double Pulse Test (Double-DPT).

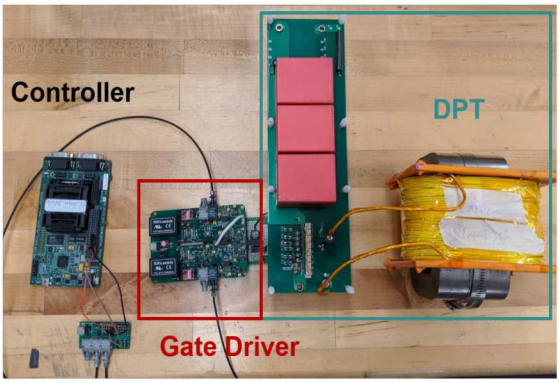


(a) dV/dt versus I_d.

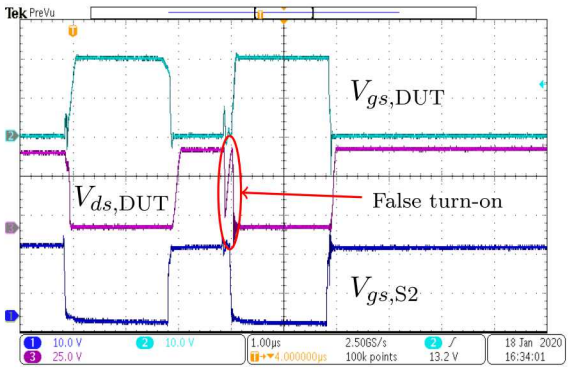


(b) dV/dt versus I_g.

Fig. 2: Variation of slew rate with respect to DUT currents.



(a) Experimental setup.



(b) Experimentally generated waveforms.

Fig. 3: Double-DPT experimental hardware.