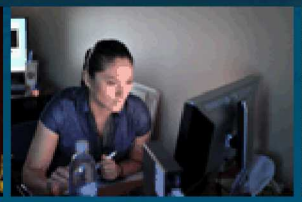
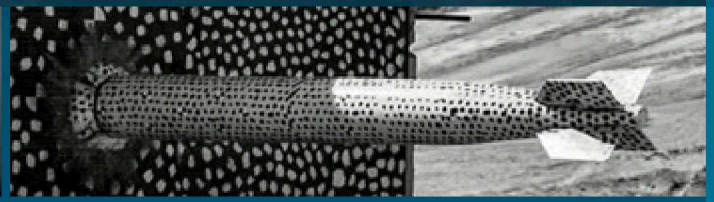
SAND2020-5842C

Optimal Power Module Design for High Power Density Traction Drive System





Lee Rashkin, Jason Neely, Lee Gill, Jack Flicker, Rachid Darbali-Zamora

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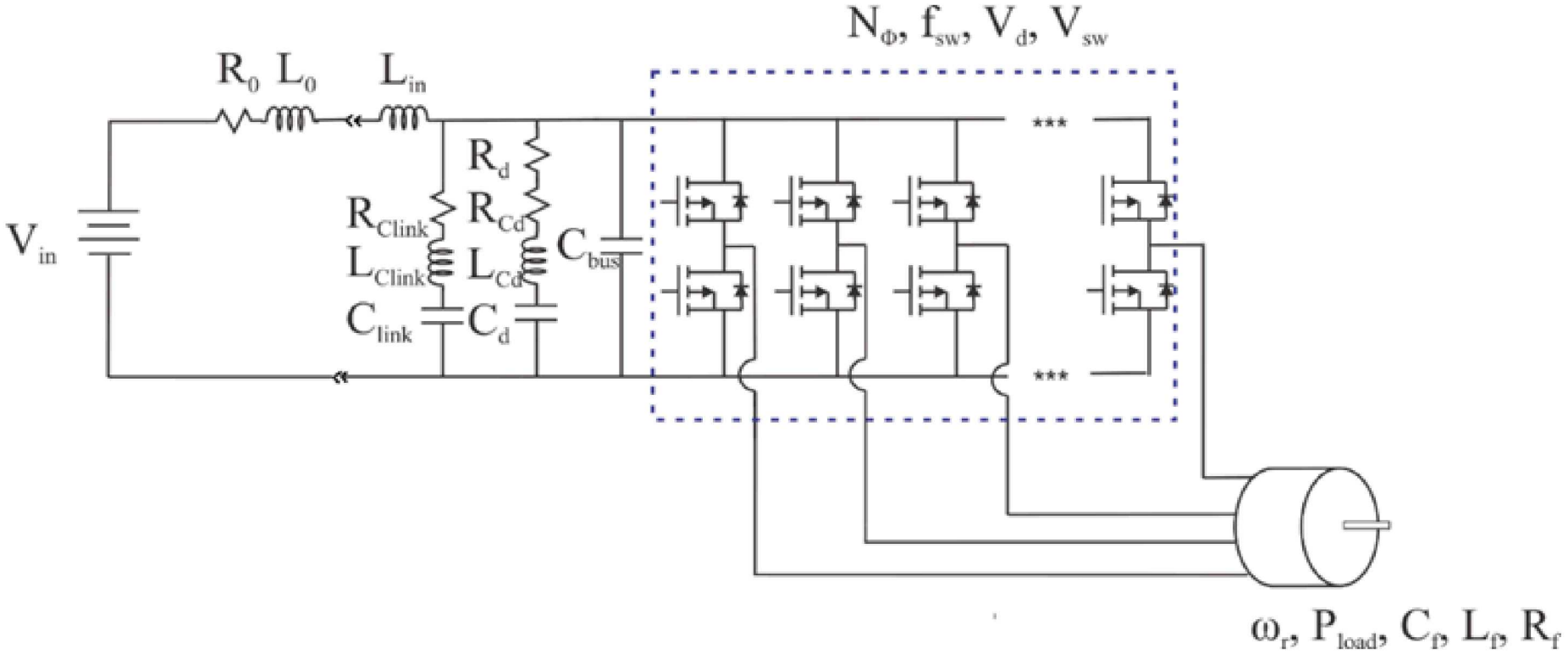
Introduction

This paper describes the design of a very high power density inverter drive module using aggressive high-frequency design methods and multi-objective optimization tools. This work is part of a larger effort to develop electric drive designs with >97% efficiency, power densities of 100 kW/L for the power electronics, and with predicted reliable operation to 300,000 miles. The approach taken in this work is to develop designs that utilize wide band gap devices (SiC or GaN) and ceramic capacitors to enable high-frequency switching and a compact integrated design. The multi-objective optimization is employed to select key parameters for the design.

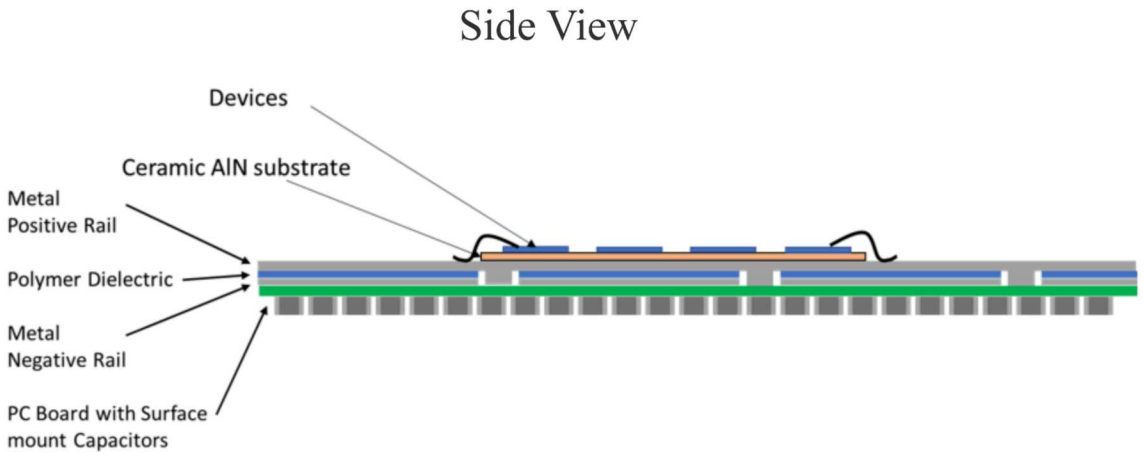
System Description

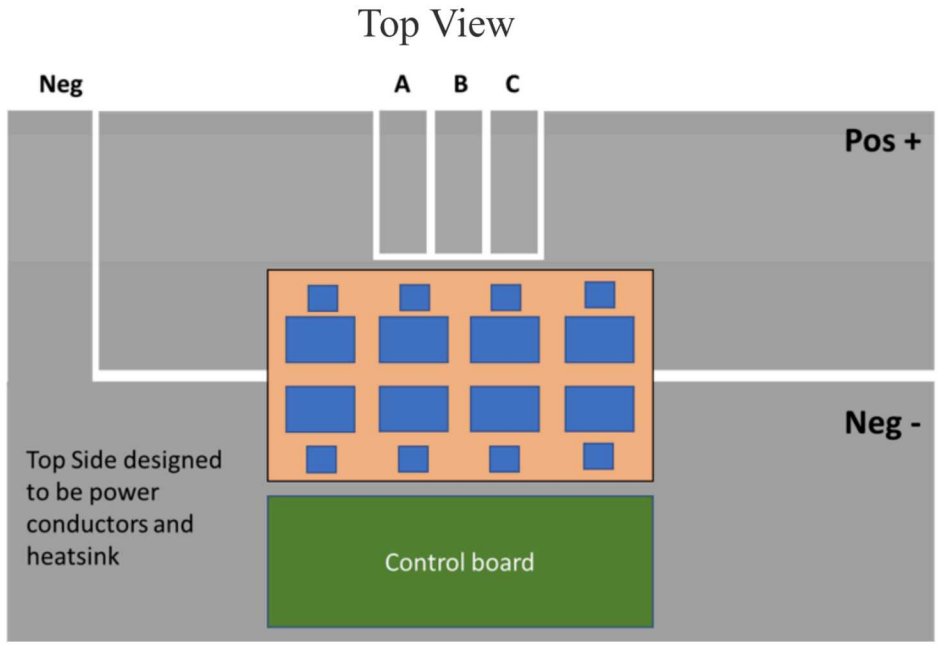


- Arbitrary number of phases
- Parasitics modeled
- Design parameters include battery voltage, input inductance, DC filter capacitor and damper, number of phases, switching frequency, motor speed, and AC output filter parameters

Flat Capacitor and Power Electronics Module Layout

- Module with devices, conductors, and flat capacitor assembly are packaged together.
- Allows surface mounted ceramic capacitors to be paralleled for large capacitance in small volume
- Advantages for thermal management and reduction of parasitics
- Dimensional analysis considers the required component sizes and voltage hold offs





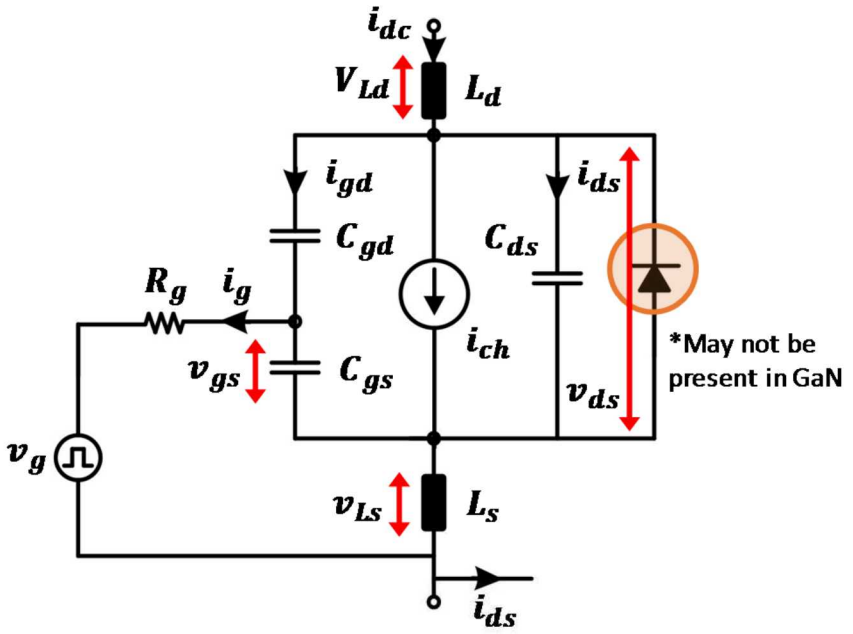
System Loss Modelling – Resistive and Switching Losses

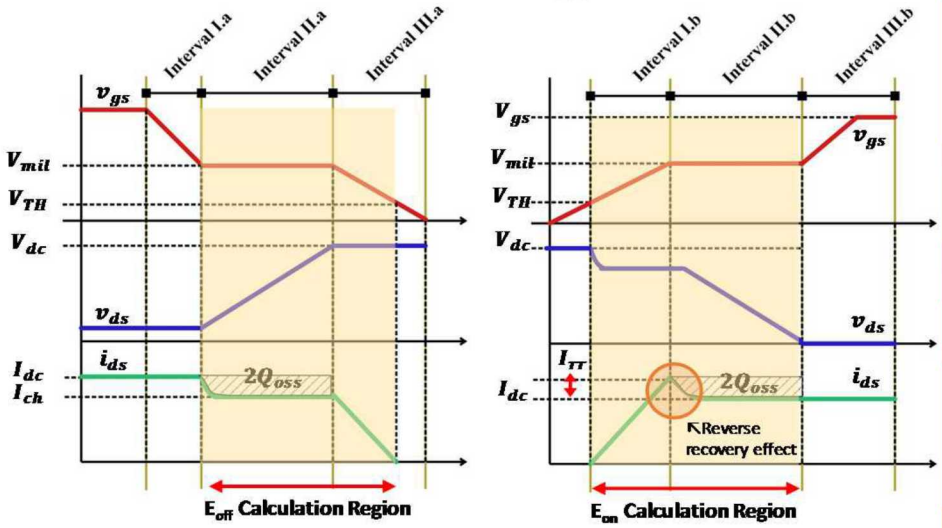
- Resistive losses including ESR modelled as I^2R losses
- Modeled based on [1]
  - Model modified to apply the model to both SiC and GaN devices.
  - The turn-on and turn-off switching losses are calculated based on the charge equivalent representation of the parasitic device parameters
  - Model depicted is linearized and includes the parasitic junction capacitances of the device (C_{gs}, C_{gd}, and C_{ds}), internal and external gate resistance (R_g), and the parasitic packaging stray inductance in the source and drain (L_s and L_d).
  - Body diode included for the SiC MOSFET

$$E_{off} = \frac{1}{2} V_{dc} I_{ch} t_{Interval\ II.a} + 1/2(V_{dc} + V_{Ld}) I_{ch} t_{interval\ III.a}$$

$$E_{on} = \frac{1}{2}(V_{dc} - V_{Ld})(I_{dc} + I_{rr}) t_{interval\ I.b} + \frac{1}{2}(V_{dc} - V_{Ld}) I_{ds} t_{interval\ II.b}$$

- Parameters used were based off of commercially available SiC and GaN devices

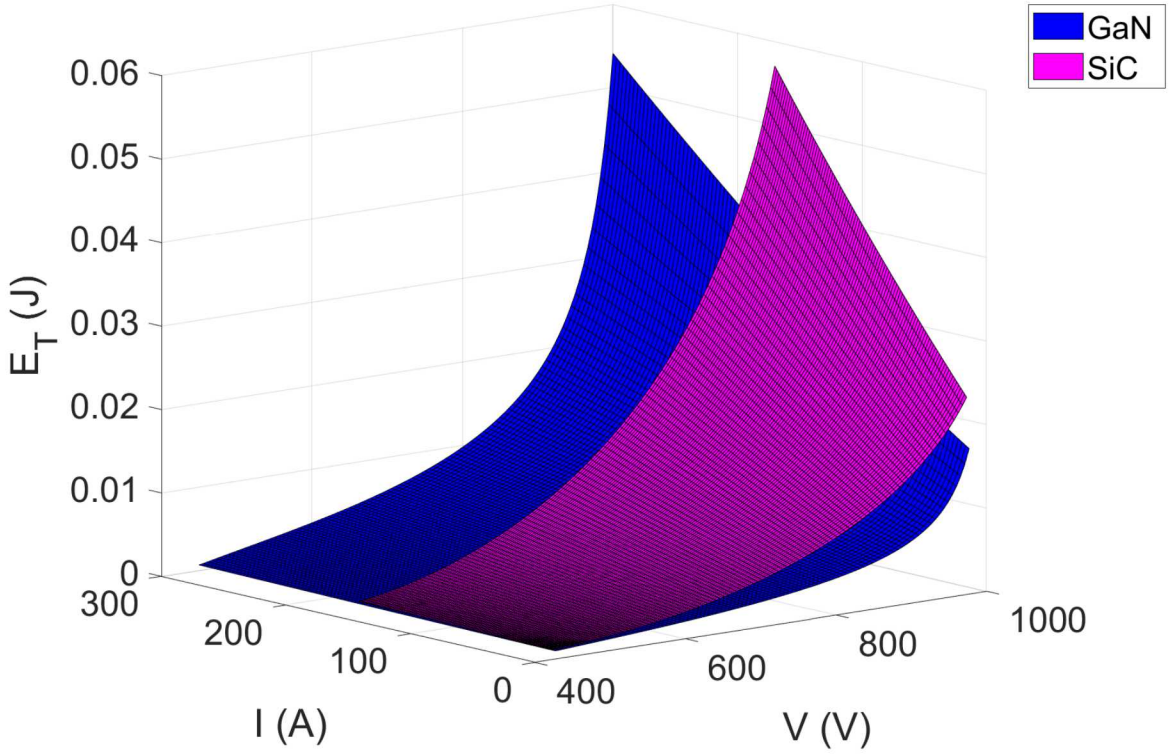




[1] D. Christen and J. Biela, "Analytical Switching Loss Modeling Based on Datasheet Parameters for mosfets in a Half-Bridge," in IEEE Transactions on Power Electronics, vol. 34, no. 4, pp. 3700-3710, April 2019.

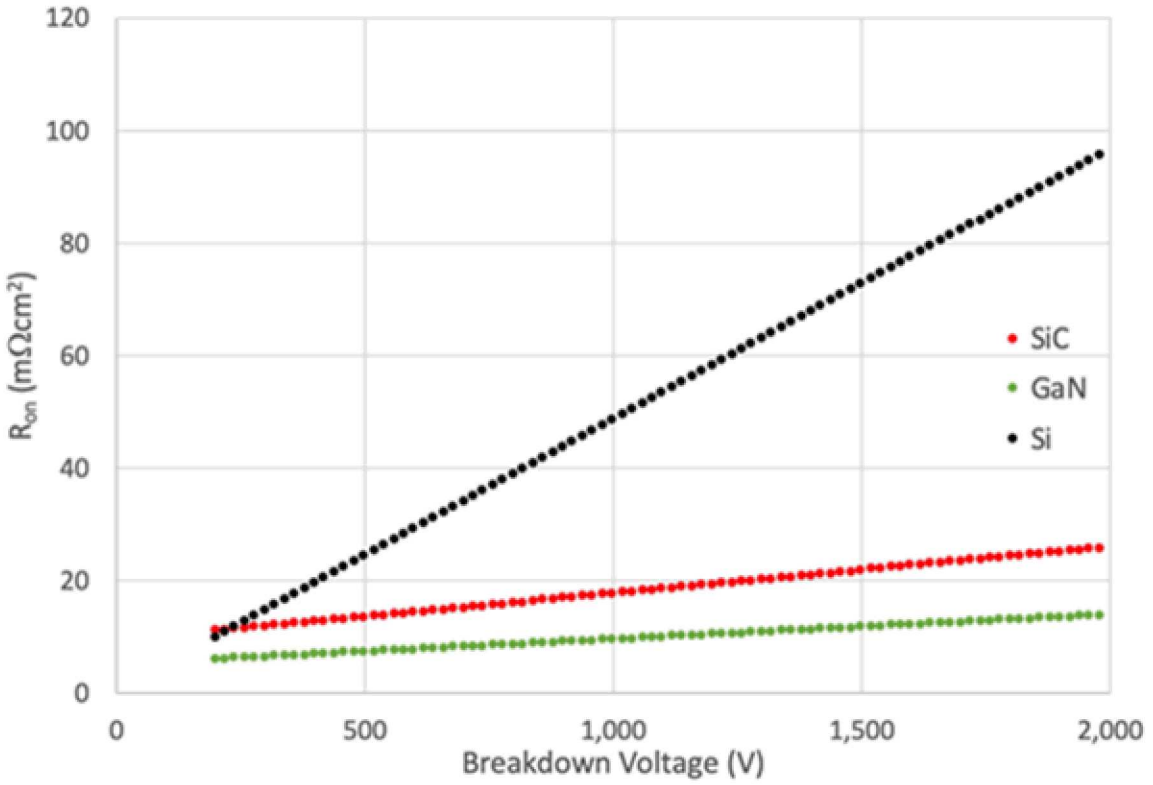
System Loss Modelling – Switching Losses

- Switching losses were calculated over a range of operating voltages and output currents
- Functions were fit to the resulting surfaces using least squares method
- Functions used to estimate losses in optimization code



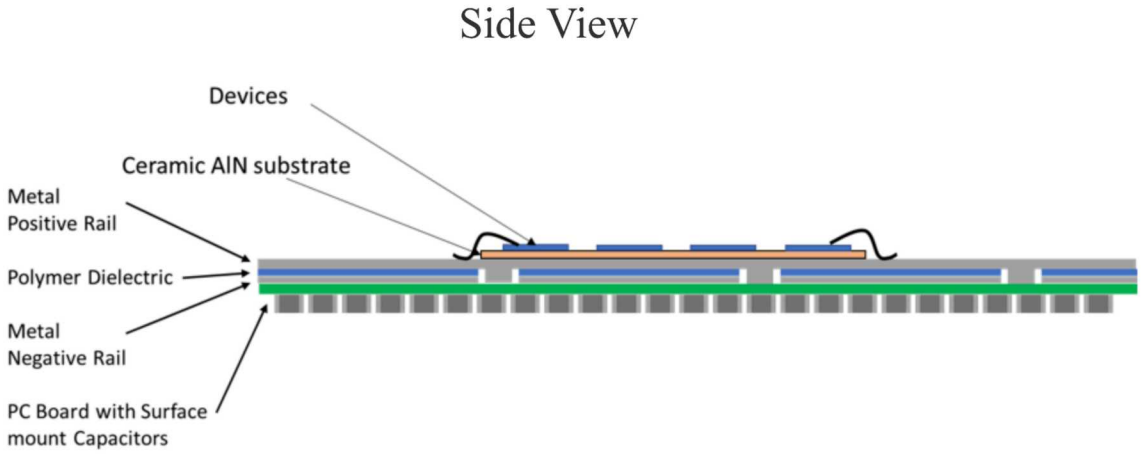
System Loss Modelling – Conduction Losses

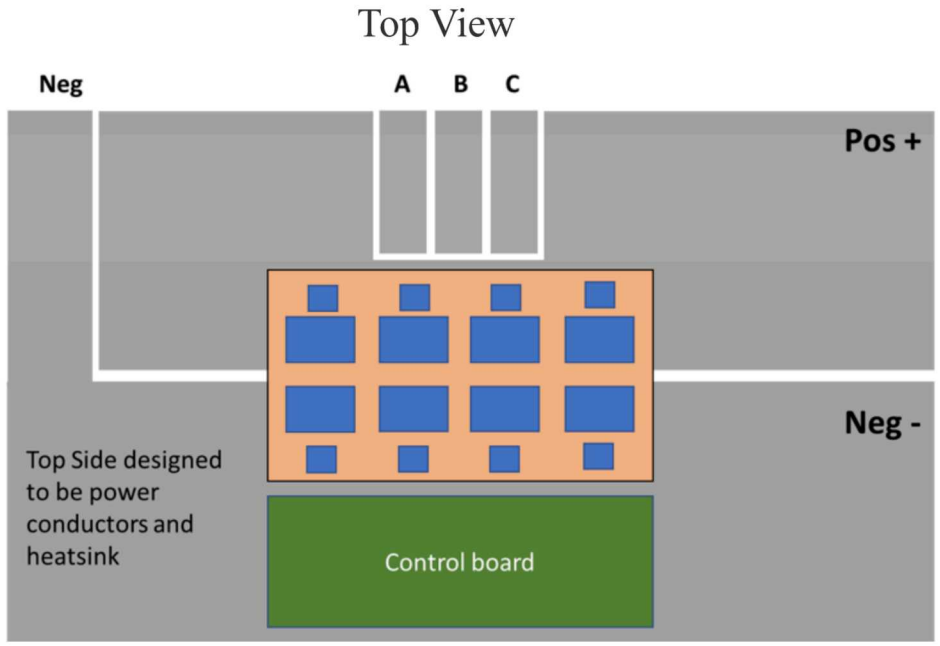
- Conduction resistance (R_{on}) was calculated for SiC and GaN vertical planar MOSFETs using the formalism and equations for intrinsic layer resistivity
- For SiC switches, a proposed SiC 1200V MOSFET with doping and layer thicknesses necessary to approximate the static operation of a commercially available device was modelled to find on-state resistivity.
- For GaN MOSFET had an architecture similar to the SiC MOSFET, namely the doping levels and physical dimensions of the gate, channel, and oxide layers.
  - Account for the differences in GaN critical field and mobility, the drift layer thickness was scaled to achieve a similar 1200V hold-off to the SiC MOSFET.



System Volume Modelling – Module and Capacitor Volume

- The power module and capacitor are highly integrated in a flat form factor design
- Dimensions of assembly are computed based on:
  - Number of phases
  - Voltage rating
  - Peak current and current densities of the devices
  - Value of DC link capacitance
  - Selection of capacitor product
  - Desired aspect ratio (length to width ratio) for the assembly
- Analysis assumes
  - Devices are mounted to a ceramic substrate
  - Two flat bus-plates with dielectric film between them are mounted below
  - DC link capacitor is realized as ceramic capacitors soldered to a printed circuit board (PCB) that connects to the bus plates at several locations

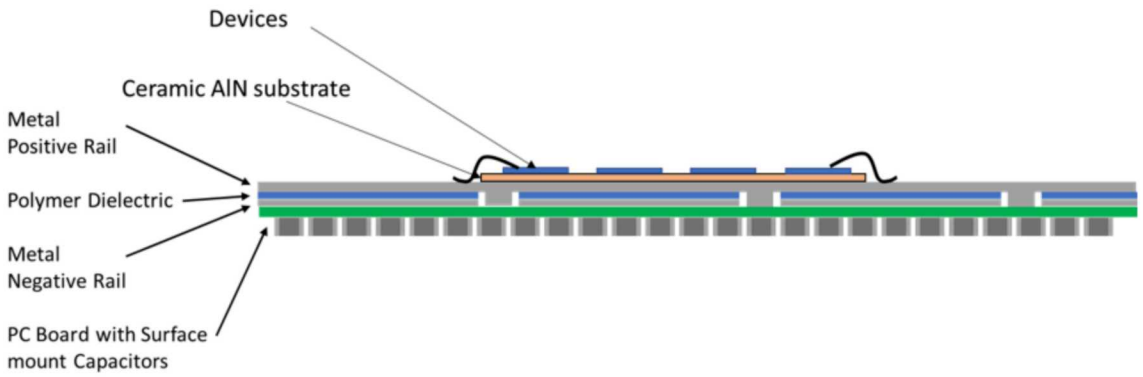




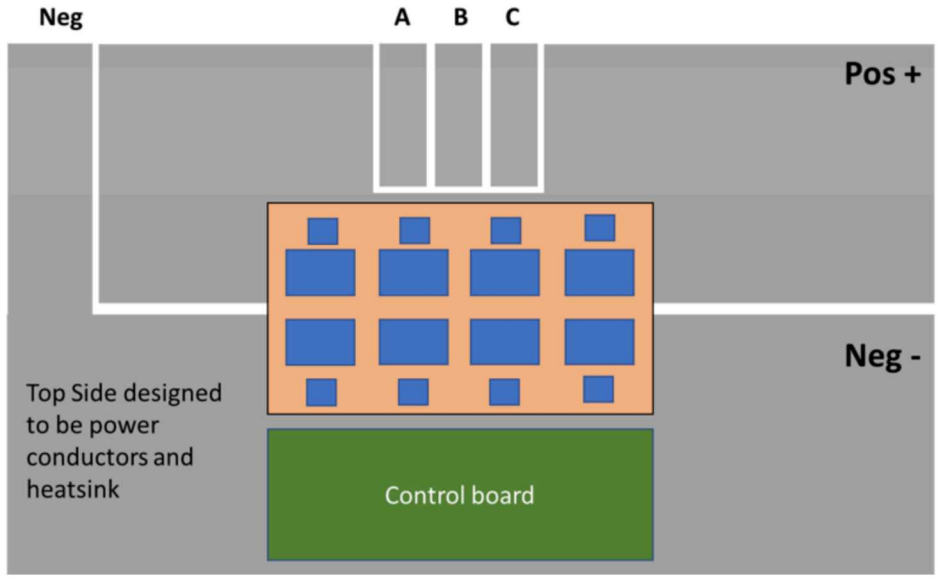
System Volume Modelling – Module and Capacitor Volume

- From the rated voltage, the required film thickness is calculated, and component spacings are computed based on required creepage.
- Based on component count and spacing, device layout is then determined to achieve the desired aspect ratio.
- This is done for the power devices and ceramic capacitors.
- Volume of the power module is simply the product of substrate length, substrate width, and total thickness (including substrate and device height)
- Volume of the capacitor is computed as the product of the PCB length, PCB width, and thickness (including bus plates, dielectric film, PCB thickness, and capacitor height).

Side View



Top View



System Volume Modelling – DC Inductor Sizing

- DC Inductor sizing was based on the area product approach
  - $A_{p,dc} = \frac{\left(L \cdot I^2 (10^4)\right)}{K_u \cdot B_m \cdot J} [cm^4]$
  - Includes core sizing and windings
  - K_u is the window utilization factor
  - J is the current density expressed in amperes per area
  - B_m is the flux density
  - L is the inductance
  - I is the current through the inductor
  - Area product ($A_{p,dc}$) is compared to catalog values to find smallest core

System Volume Modelling – Filter Inductor Sizing

- Filter inductor sizing is based on the AC inductor design version of area product approach
  - $A_{p,ac} = \frac{P_t \cdot (10^4)}{K_f \cdot K_u \cdot B_{ac} \cdot J \cdot f} [cm^4]$
  - P_t is the apparent power
  - K_u is the window utilization factor
  - K_f is the waveform coefficient
  - B_{ac} the operating flux density
  - f is the operating frequency
  - J is the current density

System Volume Modelling – Cooling System

- The cold plate sizing was determined based on commercially available data
- Fit function calculated as:

$$V_{cool} = 10^{(-1.6(\log(R_{th})+3)+3)}$$

  - V_{cool} is the cooling volume in cubic inches
  - R_{th} is the desired thermal resistance:

$$R_{th} = \frac{(T_c - T_a)}{P}$$

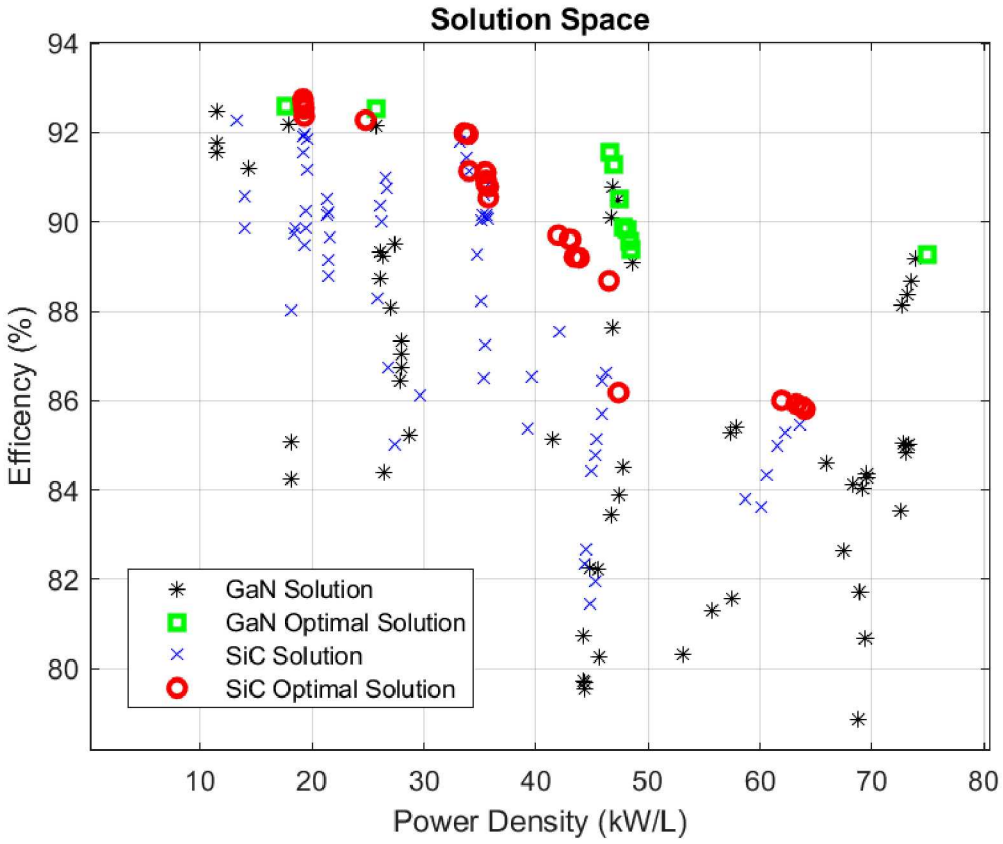
  - T_a is the ambient temperature of 25°C
  - T_c is the maximum junction temperature, set to 110°C for SiC and 150°C for GaN
  - P is the total loss in the module and capacitor board.

Genetic Optimization

- Strategy for generating design guidance and optimal designs is a global multi-objective optimization
- The genetic algorithm is a probabilistic method for optimizing multi-input systems with nonconvex solution spaces using the principles of genetics and user defined fitness functions
- Fitness functions are power density and efficiency
- Used the Genetic Optimization System Engineering Tool (GOSET) developed by Purdue University to perform genetic algorithm
  - MATLAB® based software package
  - Scripts for implementing and solving a genetic algorithm optimization problem
- Performance constraints
  - Allowable DC capacitor voltage ripple
  - AC voltage noise
  - battery current ripple

Genetic Optimization - Results

- Genetic optimization was run on 99 individuals over 100 generations
  - SiC devices
  - GaN devices
- Results show that GaN solutions are closer to the 100 kW/L power density target
  - Best solution that has a 74.949 kW/L at 89.27% efficiency
  - Three phase inverter
  - Input voltage of 915.42 V
  - Switching frequency of 343 kHz
  - 320 ceramic capacitors



Component	Volume (L)	Volume %	Loss (kW)	Loss %
Module	0.01	0.5557	0.3867	23.9519
Capacitor	0.2079	11.5969	0.0001	0.0082
Input Inductor	0	0	0	0
Filter Inductor	1.5116	84.331	1.2278	76.0399
Cooling	0.63	3.5165	N/A	N/A

Conclusions

In this paper, a genetic algorithm based procedure was used to design a motor drive while optimizing for power density and efficiency. The objective is to identify a design for a 100 kW inverter that meets the target performance of 100 kW/L and 97% conversion efficiency. The design code was run using both SiC and GaN based semiconductor devices. The results fell short of the power density target of 100 kW/L, but it can be seen that improving the sizing and losses in the AC filter inductors through new materials and geometeries is the best way to meet those targets.