SAND2019-11341D

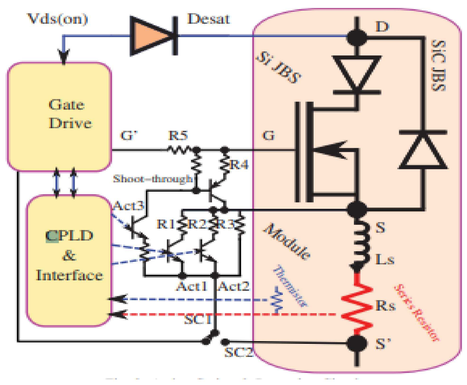
Advanced Power Conversion Systems featuring SiC MOSFETs with In-Situ Restoration Capabilities

Ranbir Singh, Subhashish Bhattacharya* and Stan Atcitty**
GeneSiC Semiconductor Inc. *FREEDM Center, North Carolina State Univ. **Sandia National Laboratories

Leveraging High Voltage/High Frequency capability of SiC power MOSFET-Diode based devices, the GeneSiC-NC State team is working to demonstrate a 400kVA Energy storage inverter featuring GeneSiC-pioneered 3.3 kV SiC monolithically integrated High Voltage SiC MOSFET-Diodes modules. The objectives of this SBIR Program is to demonstrated SiC-based power electronics platform that will offer:

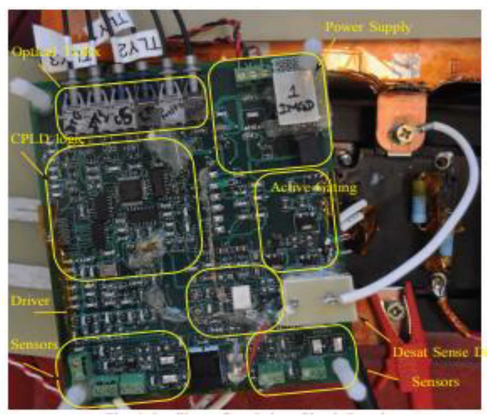
- Extend the voltage and current capability of the world's first monolithically integrated High Voltage SiC MOSFET-Diodes from 1200 V/20 A to 3300 V/50A per chip capability, with reduced inductance power modules
- Develop the first Intelligent Gate Driver for 3300 V SiC MOSFETs that provides fast, safe driving that senses and adjusts to drive conditions, and device health
- Neutral Point Clamped topology to convert 800V battery input into a direct utility connect at 13.8 kV 3-Phase 60 Hz at 10 kHz frequency to reduce the passive component size by >20X enabling smaller inverters and higher efficiencies of circuits

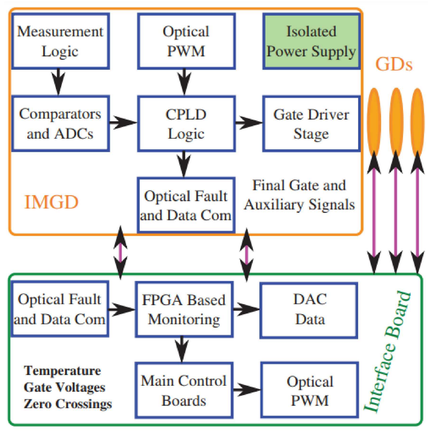
Intelligent Medium Voltage Gate Driver Development



- Due to the criticality of the application and high stress on the device, it is important to acquire operating data from the device under test for diagnosis/prognosis for predicting failure beforehand
- This is done by measuring the near-chip module temperature (Tmod), device on-voltage (Vds(on)) and device current (Id).
- Advanced gate-driving features such as active gating and shoot-through protection by controlled saturation is implemented as shown

Intelligent Gate Driver Circuit Board and Block Diagram

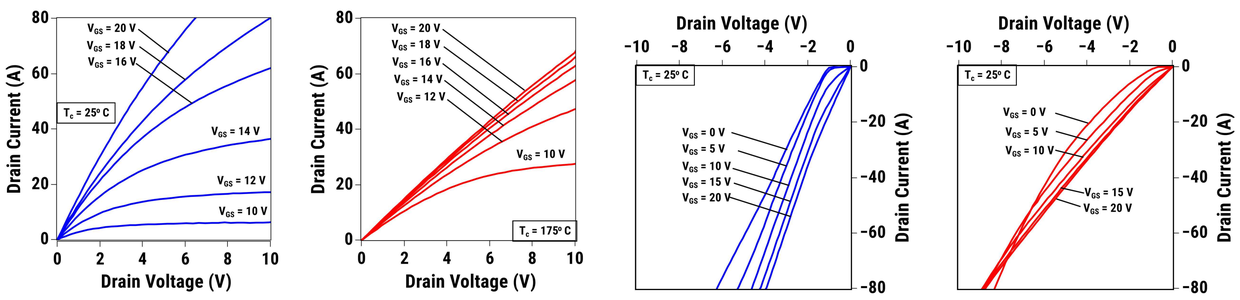




- A fully populated IMGD board and block diagram of the intelligent MV gate driver are shown. This board incorporates all the necessary restorative capabilities.

GeneSiC's 3.3 kV SiC MOSFET based mono-switch

Output and 3rd Quadrant Characteristics at 25 °C and 175 °C



- **Output characteristics show the impact of gate voltage on the drain current.**
- **These devices are normally-off at gate voltage of 0 V and can block up to 4000 V.**

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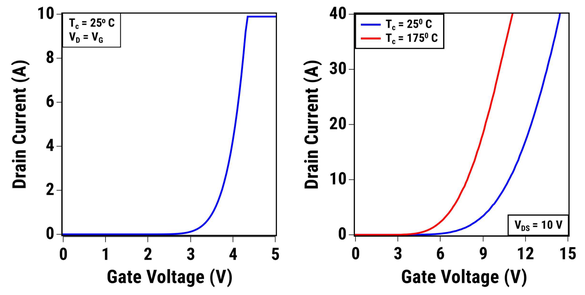
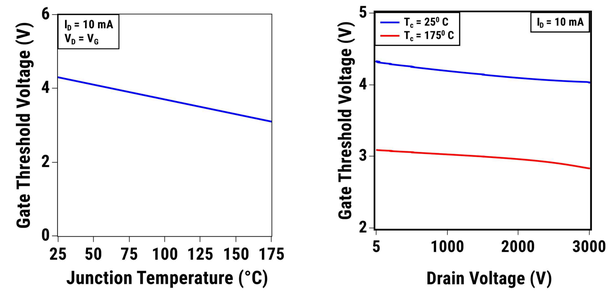
Transfer Characteristics



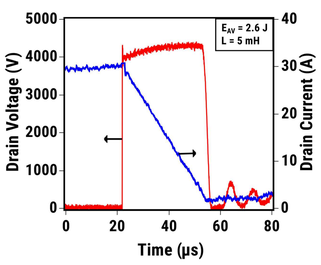
Threshold voltage variation



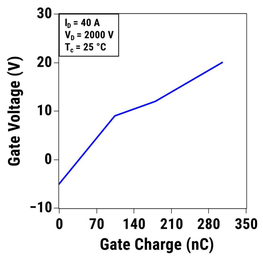
- **Transconductance of 10.5 S and 11.7 S is extracted at 40 A under 25° C and 175° C respectively.**
- **Modest 5-10% variation in threshold voltage is observed when drain voltage is increases up to 3 kV.**

Switching Characteristics

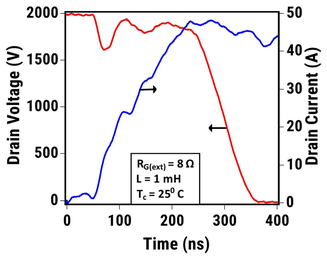
UIS Ruggedness



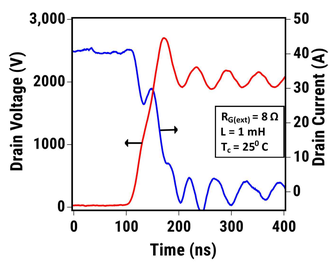
Gate Charge



Turn-on Switching



Turn-off Switching



- **Avalanche Energy of 2.6 J was recorded during UIS measurements.**
- **Total gate charge of 305 nC was measured at 2 kV and 40 A.**

Grant Details

- Period of Performance: July 1, 2019 – June 30, 2020 (SBIR Ph1)
- Principal Investigator:
  - –Dr. Ranbir Singh (GeneSiC Semiconductor) and
  - –Prof. Subhashish Bhattacharya (FREEDM Center, NCSU)
- Grantee Partners: GeneSiC Semi and NCSU

GeneSiC Semiconductor Inc.
43670 Trade Center Place
Suite 155; Dulles VA 20166
+1 703 996 8200 (ph)
ranbir.singh@genesicsemi.com

North Carolina State University
FREEDM Systems Center
Suite 100, Keystone Science Center
1791 Varsity Drive; Raleigh, NC 27606
sbhatta4@ncsu.edu

Acknowledgement: The authors thank Dr. Imre Gyuk for funding this SBIR work (Grant DE-SC0019797) and Dr. Stan Atcitty for technical contributions. Sandia National Laboratories is a multimission laboratory managed and operated by National Technology and Engineering Solutions of Sandia, LLC, a wholly owned subsidiary of Honeywell International, Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA0003525.