SAND2018-13956C

Non-volatile electrochemical memory utilizing TiO_2 for neuromorphic computing

PRESENTED BY

Yiyang Li, Elliot J. Fuller, Sapan Agarwal, A. Alec Talin

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Artificial neural networks and deep learning

Computers are fast and efficient at implementing task-specific instructions

$$\frac{dx}{dt} = x^2$$

```
x=1;
dt = 0.01;
for i = 1:1000 {
   dxdt = x.^2;
   xnew = dt*dxdt;
   x = xnew; }
end
```

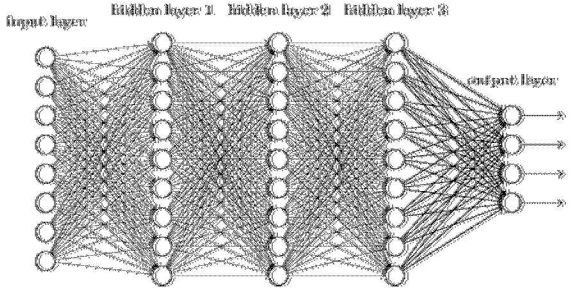
Computers struggle when there are no clear instructions for the task

Which one of these images is a cat?

Image recognition
Autonomous driving
Natural language processing

Artificial neural networks: use training examples and error backpropagation to find the matrix weights that correctly maps the input **x** onto the desired output **y**

$$\begin{bmatrix} y_1 \\ \vdots \\ y_m \end{bmatrix} = \begin{bmatrix} w_{1,1} & \cdots & w_{1,n} \\ \vdots & \ddots & \vdots \\ w_{m,1} & \cdots & w_{m,n} \end{bmatrix} \begin{bmatrix} x_1 \\ \vdots \\ x_n \end{bmatrix}$$

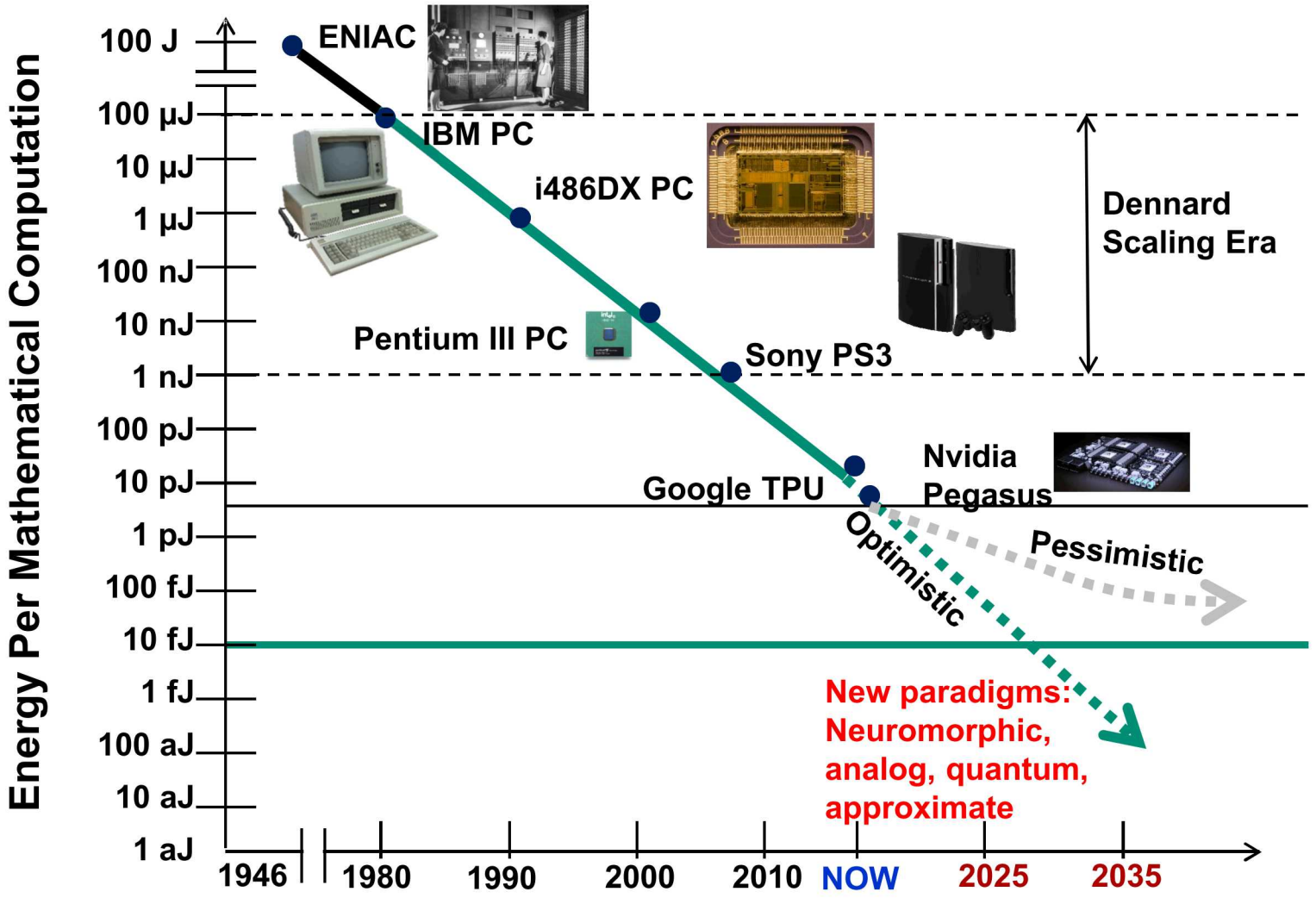


Artificial neural networks are power intensive

Andrew Ng, Coursera
Nawrocki et al. *IEEE Elec. Dev.* 2016

n, m > 1000

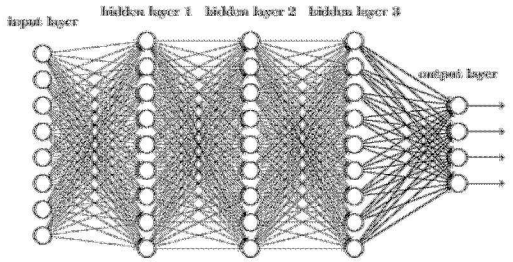
Evolution of Computing Machinery



3

Digital and analog implementations of neural networks

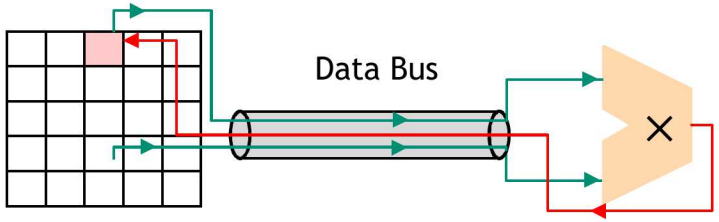
$$\begin{bmatrix} y_1 \\ \vdots \\ y_m \end{bmatrix} = \begin{bmatrix} w_{1,1} & \cdots & w_{1,n} \\ \vdots & \ddots & \vdots \\ w_{m,1} & \cdots & w_{m,n} \end{bmatrix} \begin{bmatrix} x_1 \\ \vdots \\ x_n \end{bmatrix}$$



Von Neumann Digital
Separate logic and memory structures

SRAM to store the weights

Arithmetic logic unit for multiplication

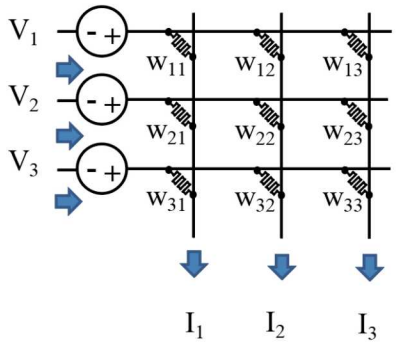


Uses established CMOS technology
Data bus results in latency and power

In-memory Parallel Analog
Use non-volatile memory

Crossbar for matrix multiplication

Conductance of each element can be changed in a predictable manner



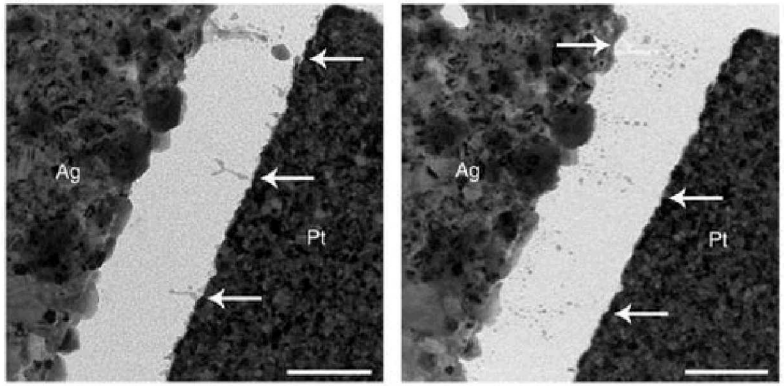
$$I_1 = V_1W_{11} + V_2W_{21} + V_3W_{31}$$

Simultaneous logic and memory
3 orders of magnitude less power

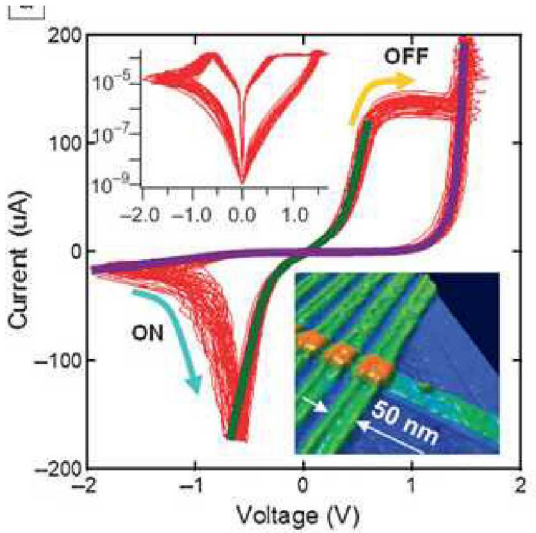
M. Marinella, *IEEE Circuits and Systems*, 8, 86-101, 2018
Zidan, Strachan, & Lu, *Nat. Elec.* 1, 22, 2018

Fundamental physics dictates memristor I-V

filament forming metal oxides (FFMO)

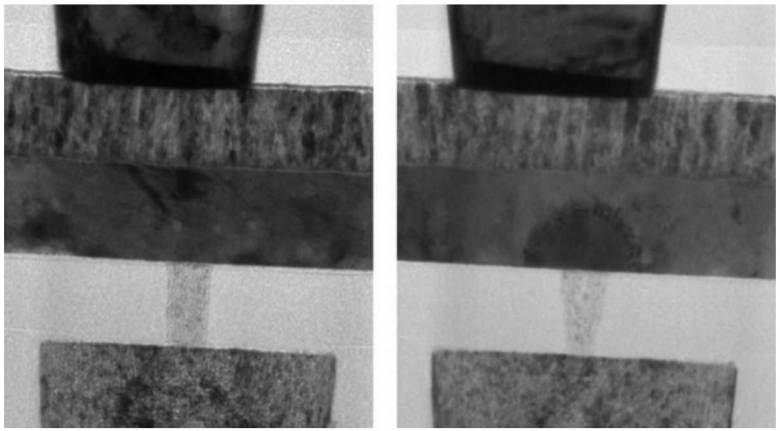


Yang et. al. *Nature Communications* (2012)

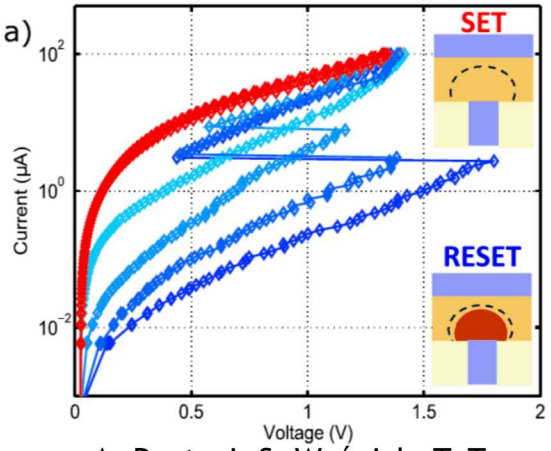


J. J. Yang , I. H. Inoue , T. Mikolajick , C. S. Hwang MRS Bull. 37, 131 2012

phase change materials (PCM)

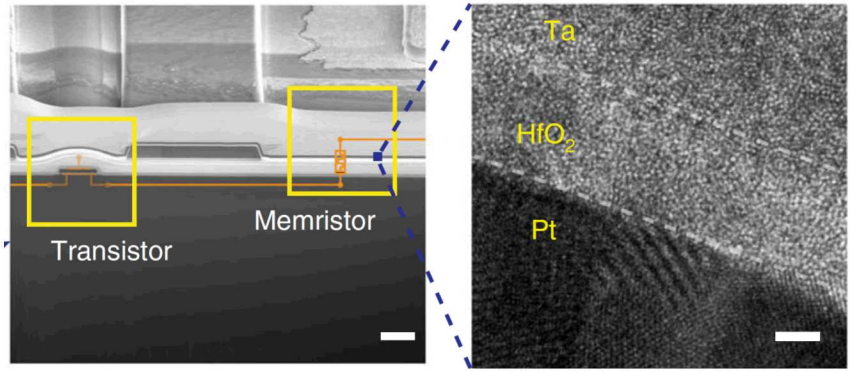


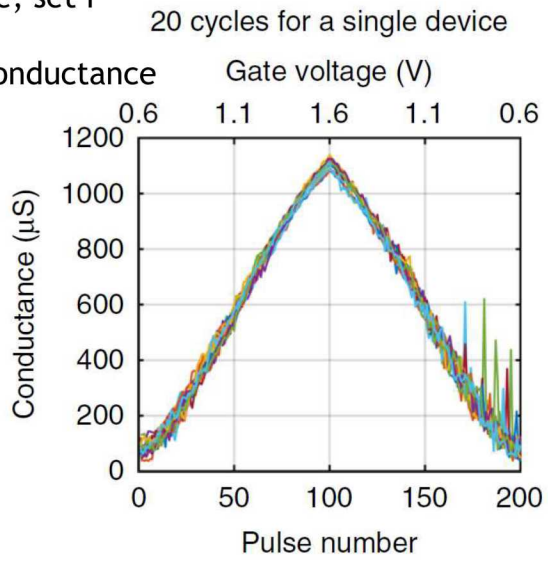
Breitwisch, Phase Change Materials: Science and Applications © 2009 by Springer



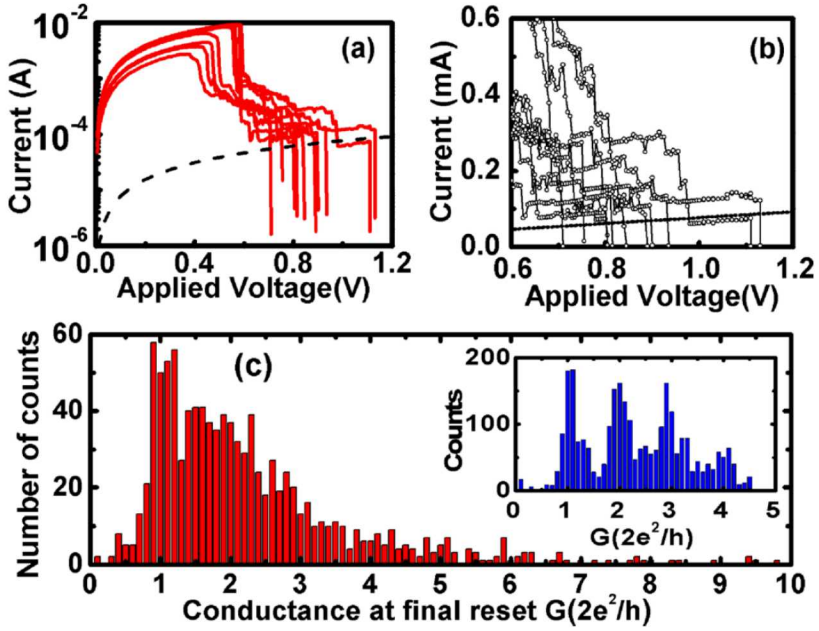
A. Pantazi, S. Woźniak, T. Tuma, E. Eleftheriou, Nanotech. 27 2016

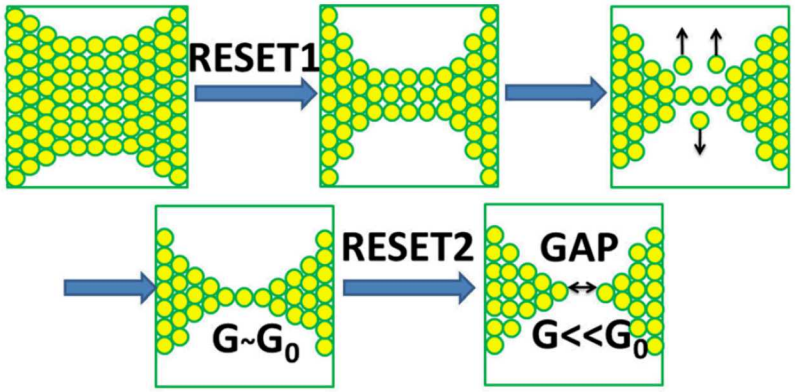
- Increase conductance → synchronized V+ to memristor, FET gate; set I compliance
- Decrease conductance→ reinitialize memristor, then increase conductance as above





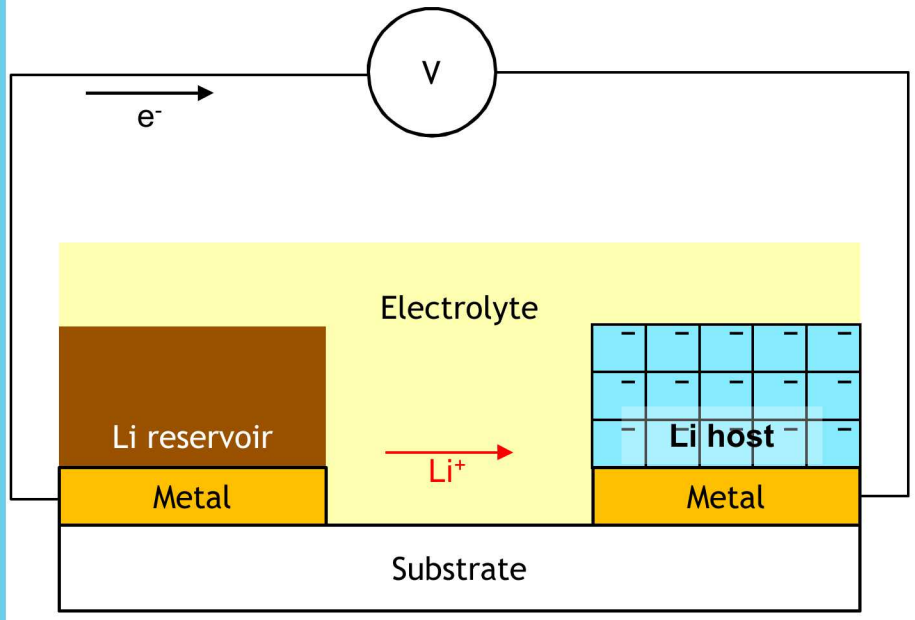
100 μS→
0.1mA @1V!

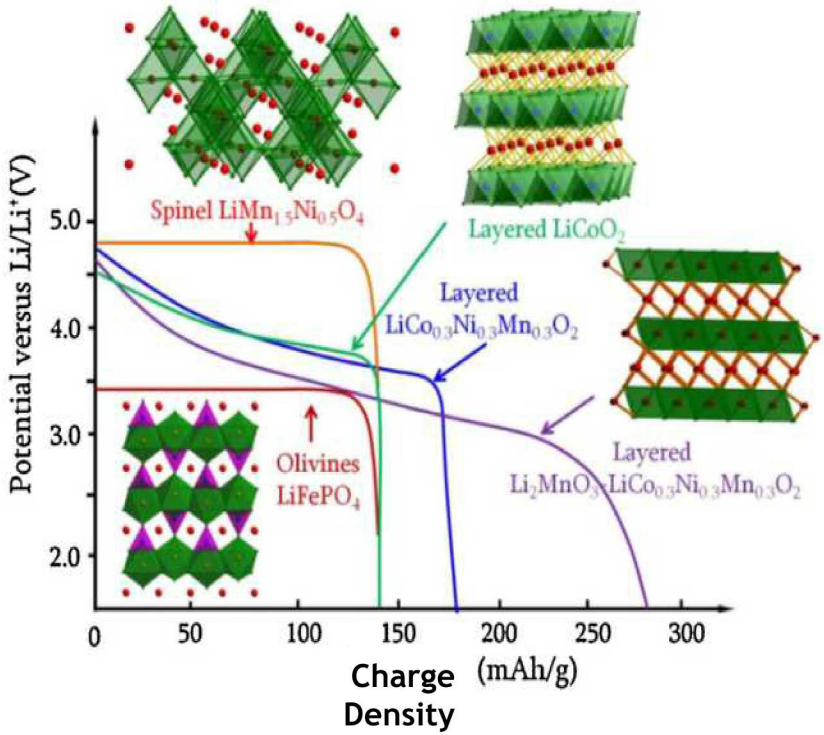




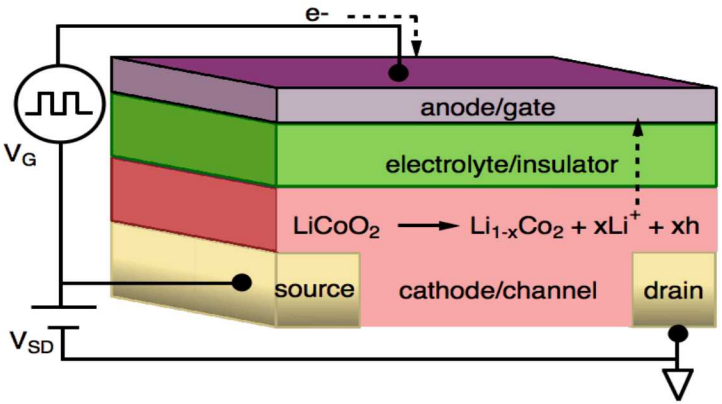
$$G_o = {}^{2e^2}/_{h} = 13k\Omega$$

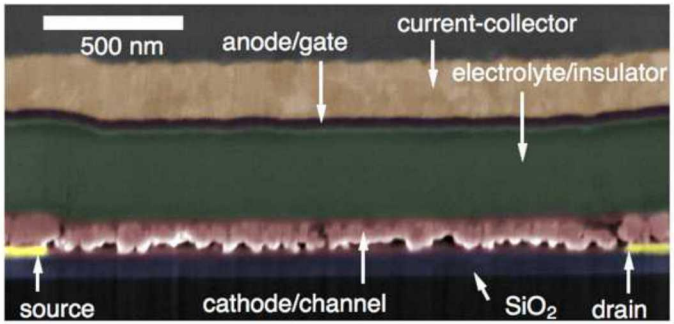
Ion-insertion electrodes for neuromorphic computing

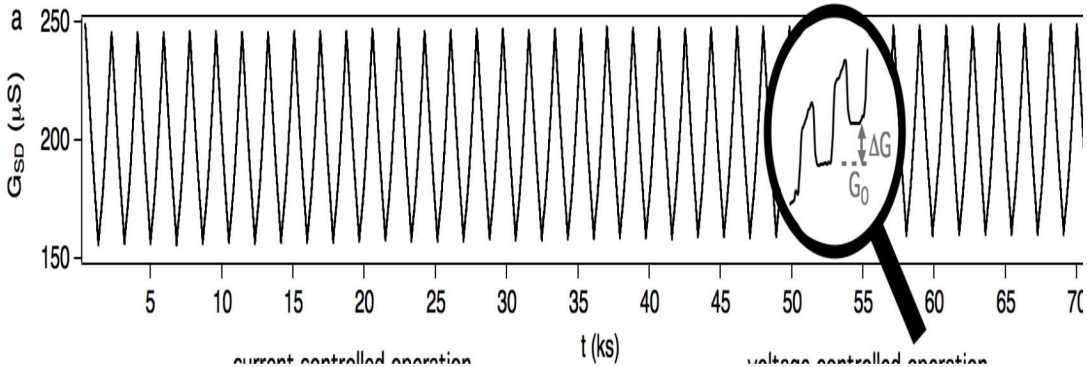


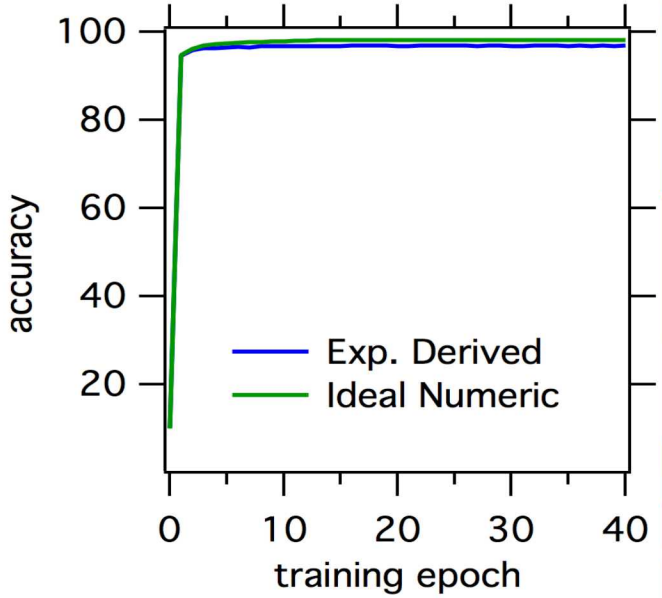


LISTA: 1st ion insertion artificial synapse



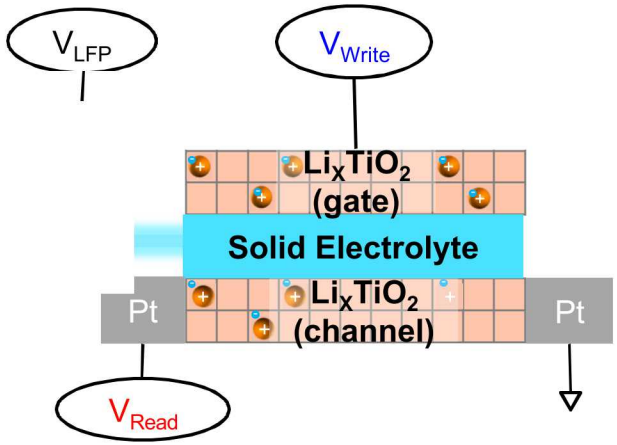


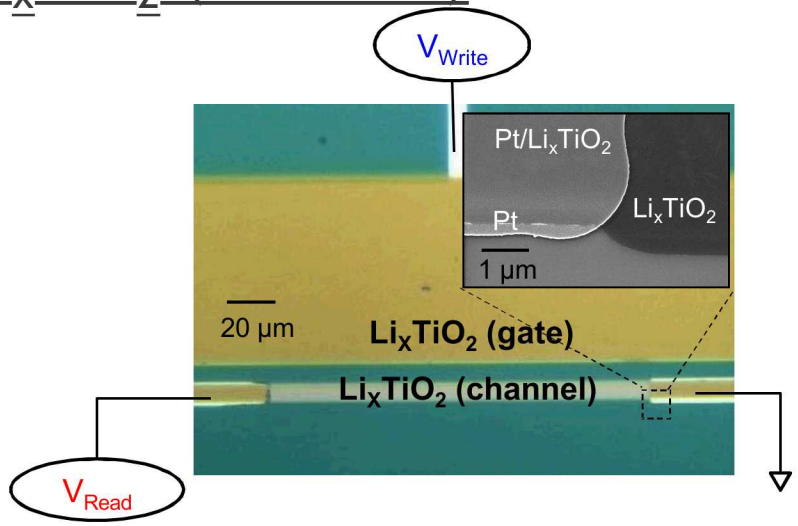


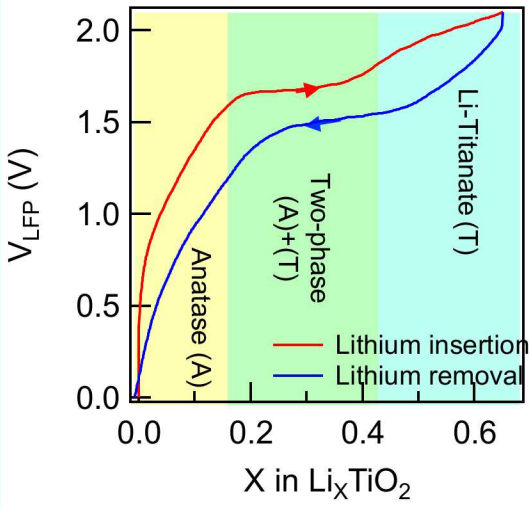


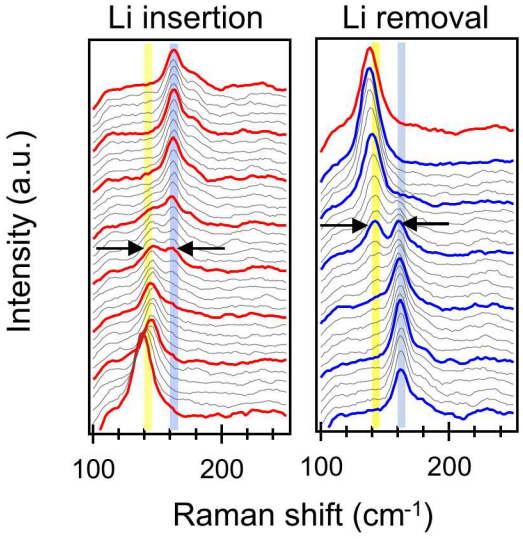
E. J. Fuller, F. El Gabaly, F. Léonard, S. Agarwal, S. J. Plimpton, R. B. Jacobs-Gedrim, C. D. James, M. J. Marinella, A. A. Talin, Adv. Mat., 29, 1604310, 2017

Lithium insertion into Li_xTiO_2 (anatase)

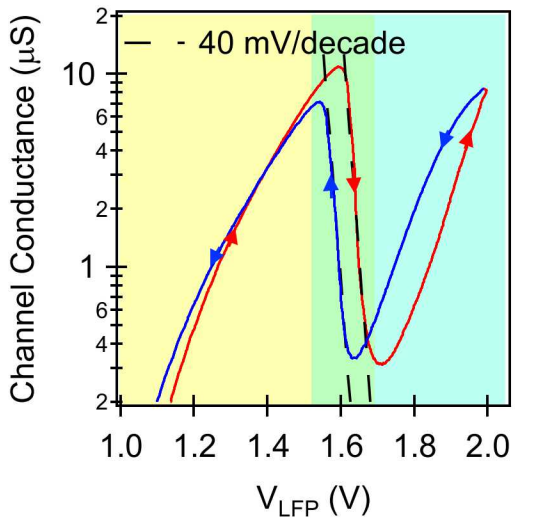






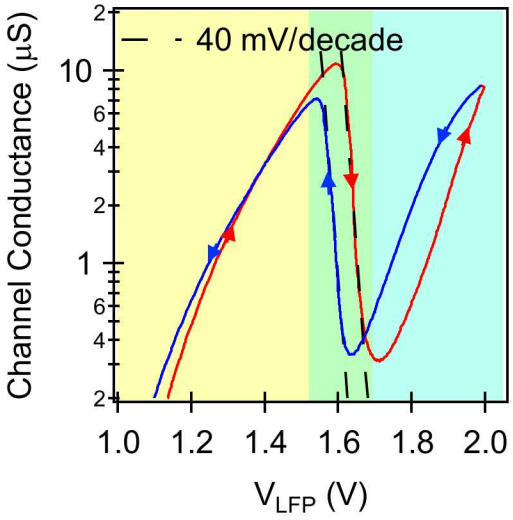


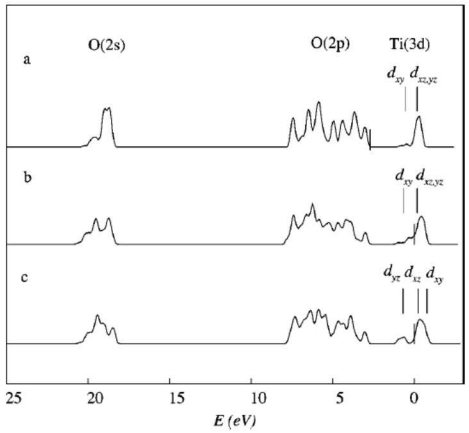
$$Li^+ + e^- + Ti_{Ti}^X \rightarrow Li_i^\circ + \boldsymbol{Ti'_{Ti}}$$



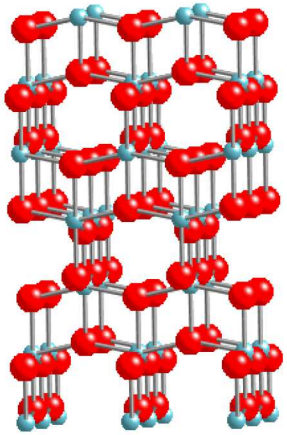
Decrease in conductivity due to correlation in $Li_{.5}TiO_2$

$$Li^+ + e^- + Ti_{Ti}^X \rightarrow Li_i^{\cdot} + \boldsymbol{Ti'_{Ti}}$$

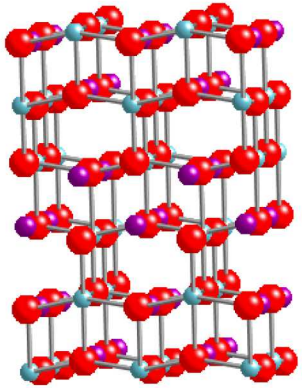




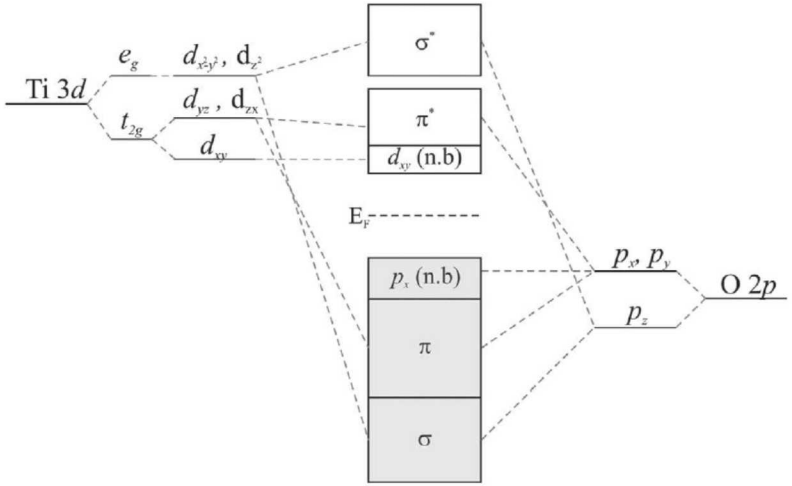
M. V. Koudriachova, S. W. de Leeuw, N. M. Harrison, Phys. Rev. B 69, 054106, 2004



tetragonal, *a*, *b*=3.787Å and *c*=9.515

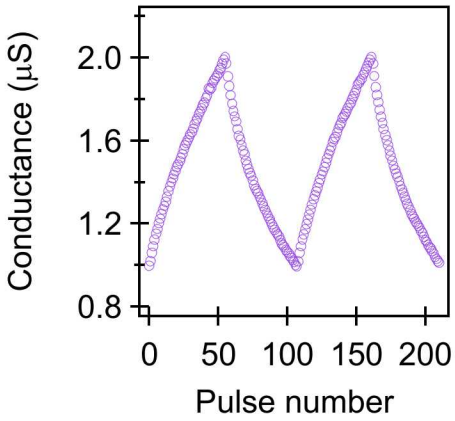


orthorombic, *a=3.819 b*=4.084 Å and *c*=9.066

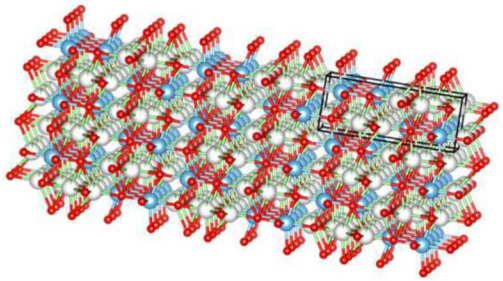


Linear programming and high accuracy

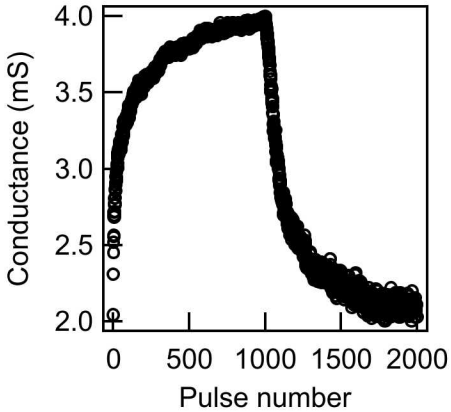
Li_XTiO_2 transistor
Voltage: ± 0.15 V



Ion insertion: stores information continuously as dopants in a crystal

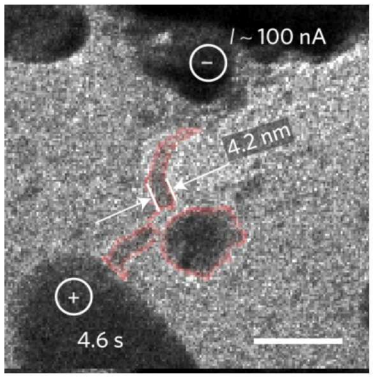


TaO_x Memristor
Voltage: ±1 V



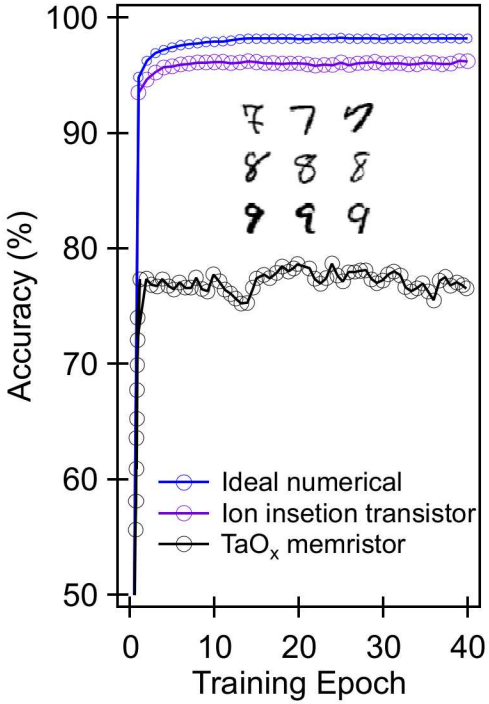
R. Jacobs-Gedrim et al. *ICRC*, 2017

Memristors: stores information at filaments



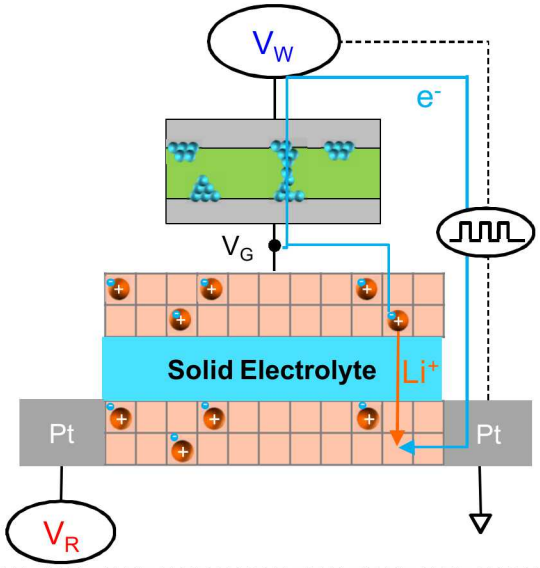
Wang et al. *Nat Mater.* 2017

Linearity is essential to train an accurate neural network



Crossbar Simulator

Low-voltage, Si-free electrochemical memory



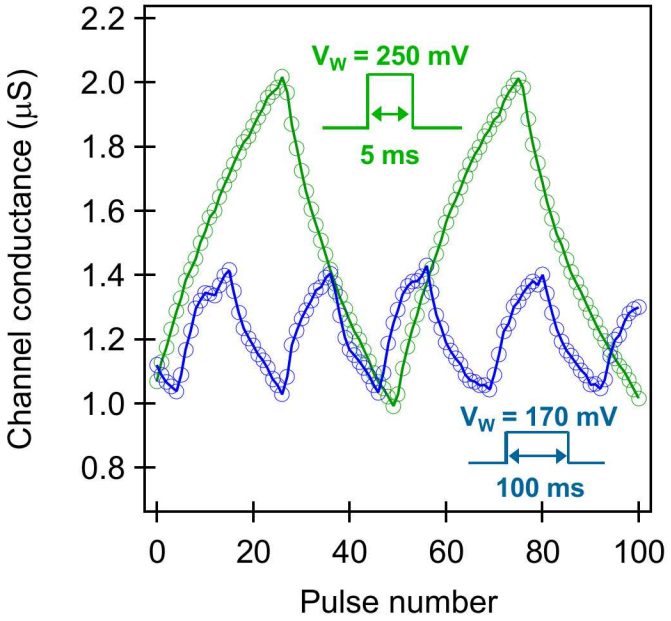
Diffusive memristor (Ag in SiO_X): high ON/OFF ratio

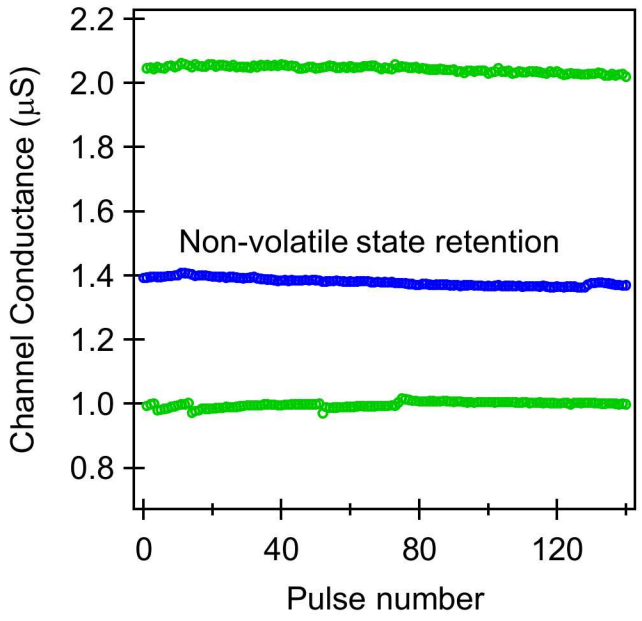
Ion insertion transistor: high charge density via bulk storage

Both: Low switching voltages

Wang et al. Nat. Mater. 2017

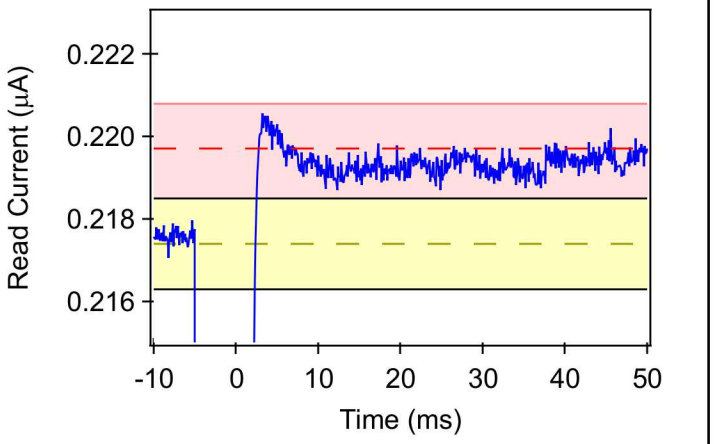
Non-volatile memory that switches at just 6 times the thermal voltage

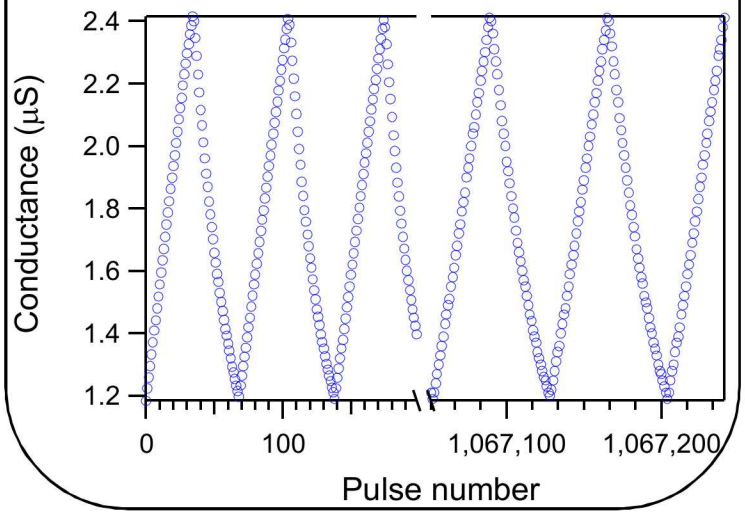




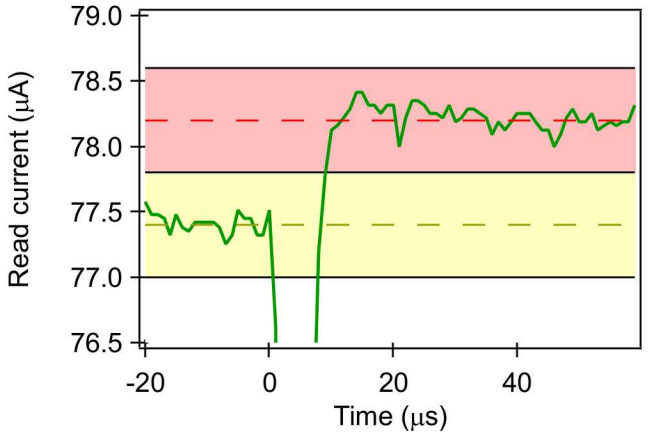
Switching speed and endurance

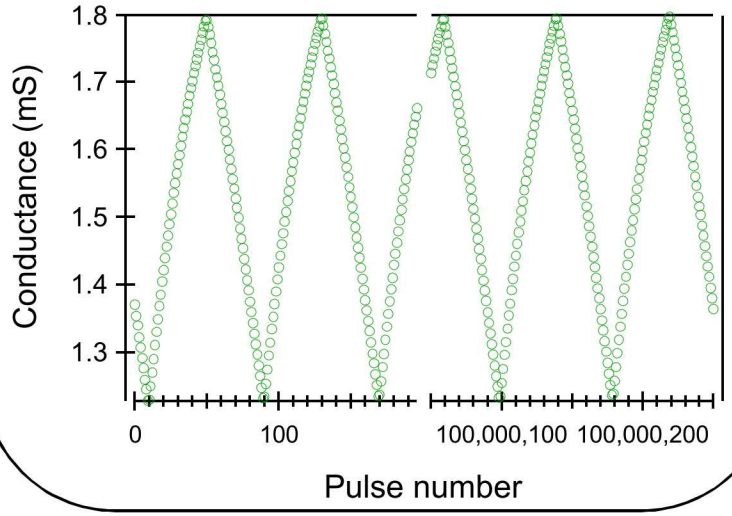
Inorganic (Li_XTiO_2) ~5 ms,
10^6 read/write cycles





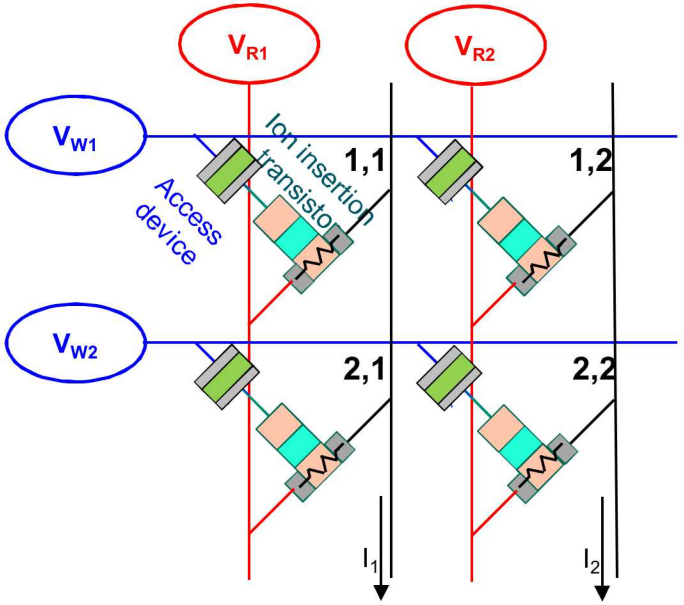
Organic (PEDOT/PSS) ~10 μs
10^8 read/write cycles



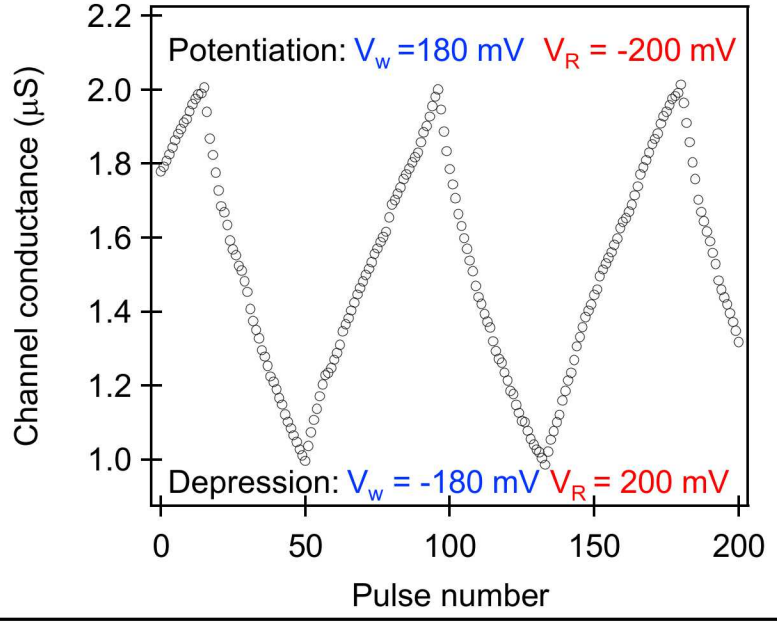


V/2 crossbar programming scheme

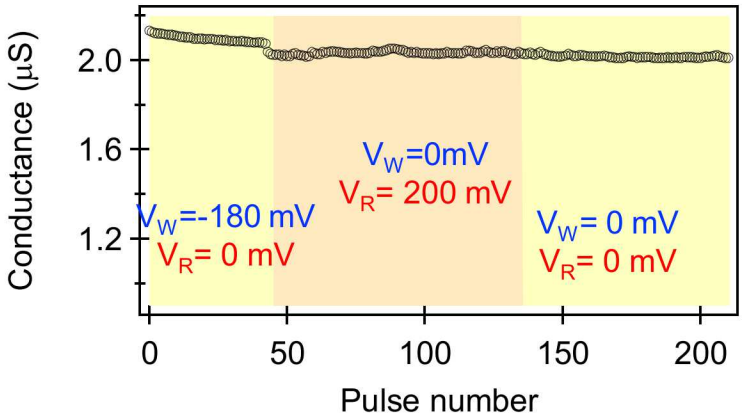
Devices are selected through applying the row and column voltages

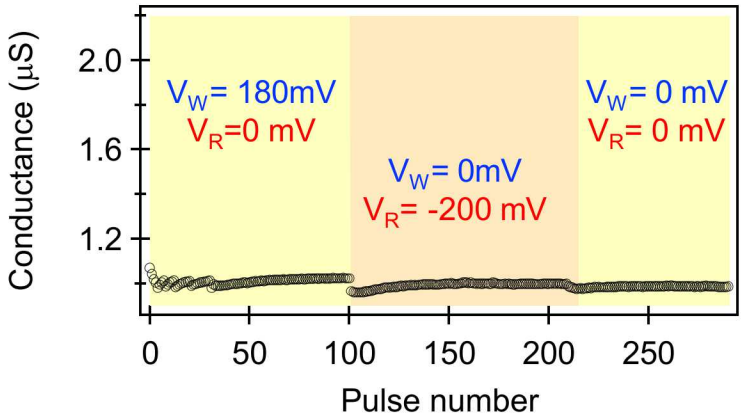


A device is programs when both the row and column is selected



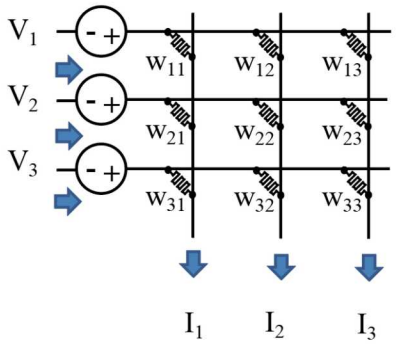
Selecting a row or column will not disturb the device

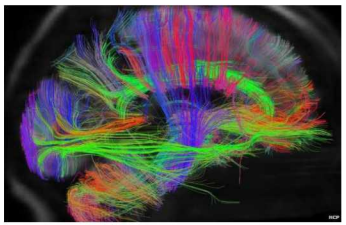




Ion insertion transistors for neuromorphic computing

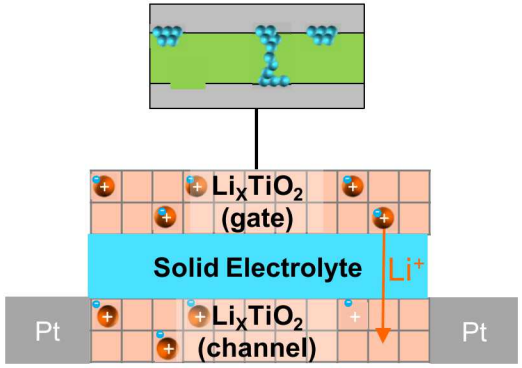
Analog neuromorphic computing provides lower energy and more parallelism compared to digital computing.

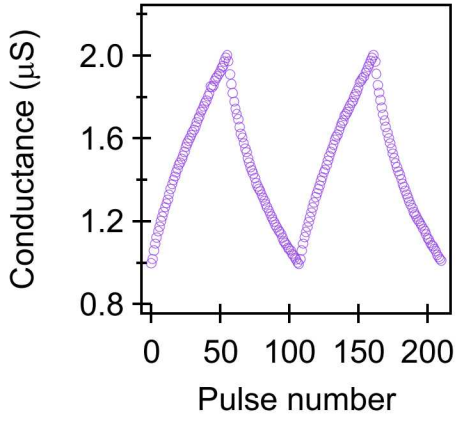




100 billion neurons
100 trillion synapses

Electrochemical ion insertion can be used to create highly linear, low voltage non-volatile analog transistors

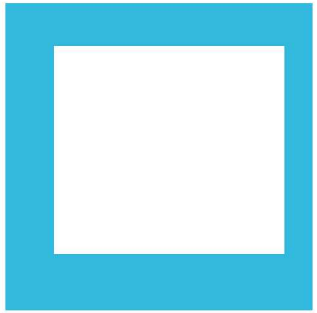




Acknowledgements

Sandia	**Stanford**
Zhiyong Li	Alberto Salleo
Farid El Gabaly	Scott Keene
Yuping He	

E. J. Fuller et al. *Adv Mater.* 29, 160413 (2017)
Y. van de Burgt et al. *Nat Mater.* 16, 414 (2017)



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