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TCAD simulation of a 1 kV, 10 A GaN MISFET Device

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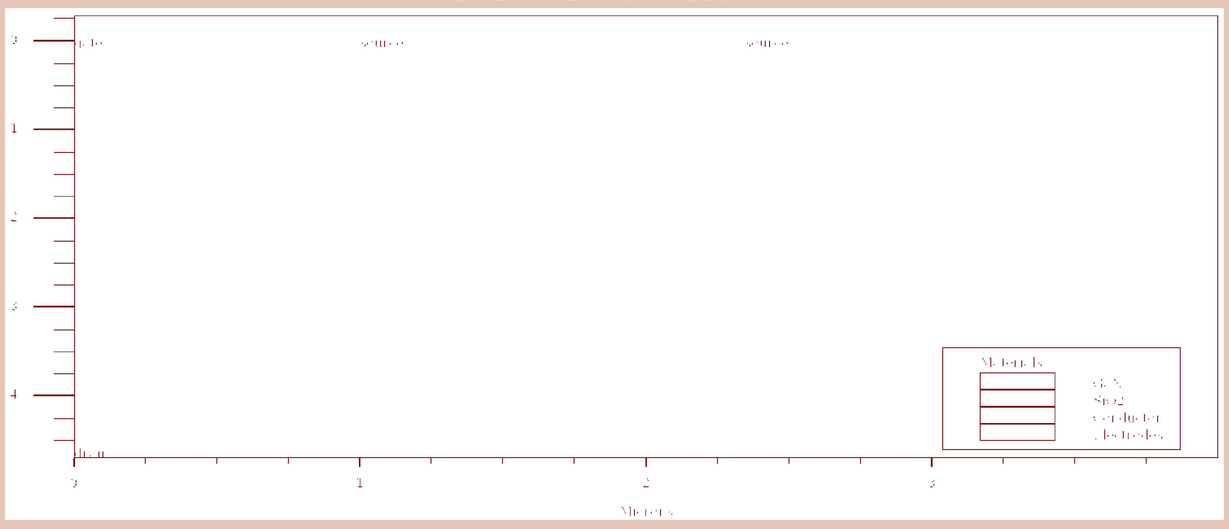
Here we report simulations of a vertical metal-insulator-semiconductor field effect transistor (MISFET) capable of blocking 1 kV and achieving 10 A of forward current. The vertical trench-gate structure eliminates the need for selective-area doping in the active region of the device, which is challenging in GaN. Optimization of dielectric/semiconductor interfaces, as well as electric field management, are critical to achieving the desired device performance. Simulations were performed using Silvaco TCAD (www.silvaco.com).

Device Structure



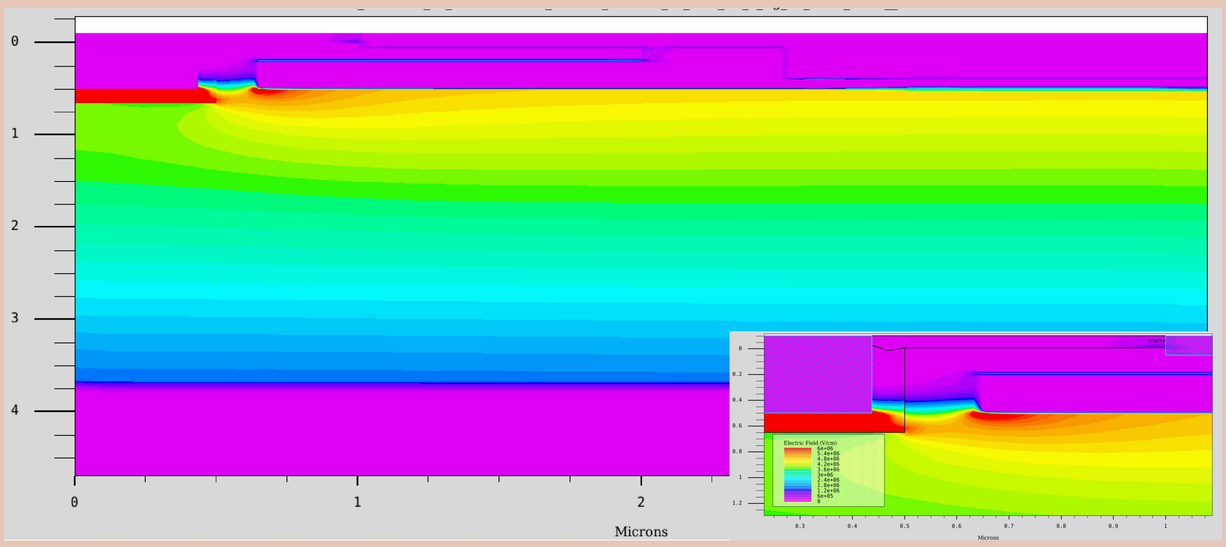
Key material parameters

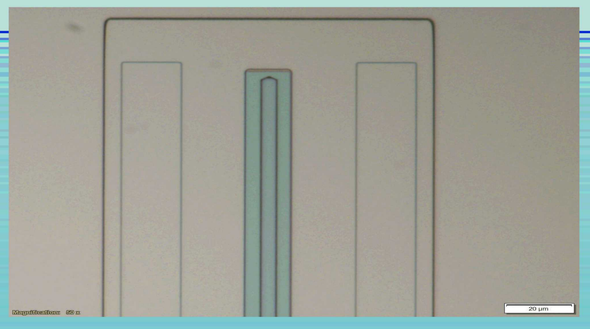
Source region doping/thickness:	n-type 5×10^{18} cm^{-3} / 200 nm
body region doping/thickness:	p-type 3×10^{19} cm^{-3} / 300 nm
Drift region doping/thickness:	n-type 4×10^{16} cm^{-3} / 3.3 μm
Critical field:	3.75 MV/cm @ 5×10^{15} cm^{-3}

Electron mobility: 1300 cm^2/Vs (bulk) | 25 cm^2/Vs (channel)

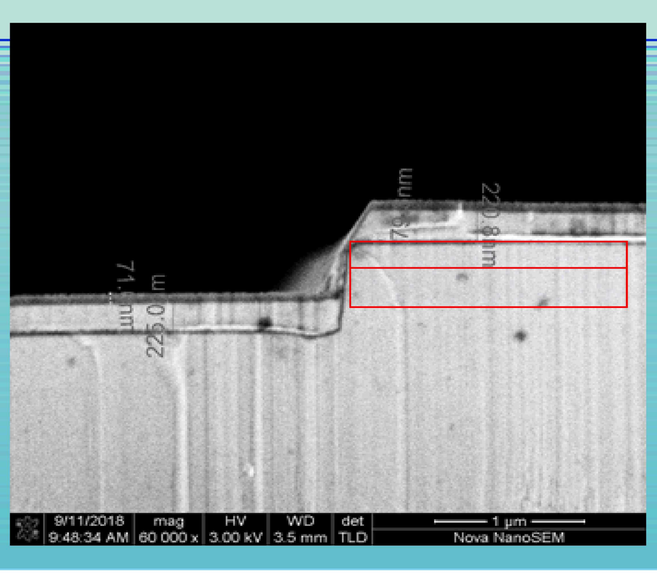
GaN interlayer thickness: 20, 60, 100, and 140 nm from oxide to p- region

Electric Field Profile at Breakdown

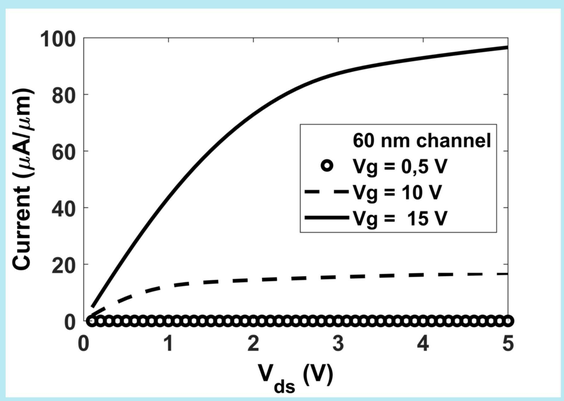




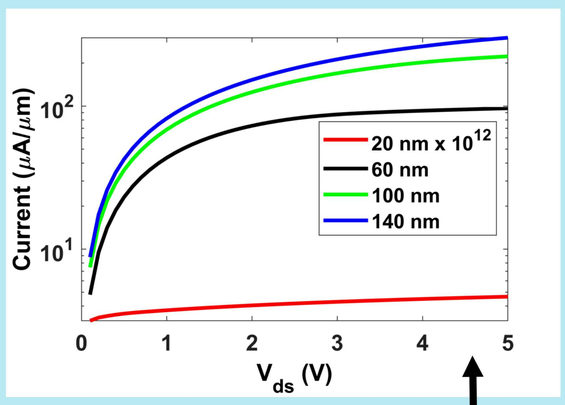
Top view and cutline of gate region of GaN MISFETs currently being developed at Sandia National Laboratories



Electrical Simulation Performance

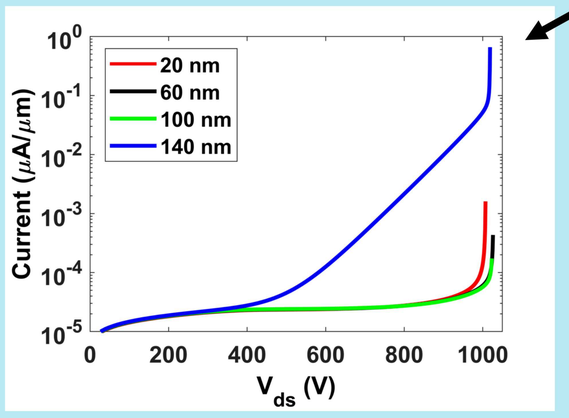


- 60 nm channel width
- V_G = 0, 5, 10, and 15 V

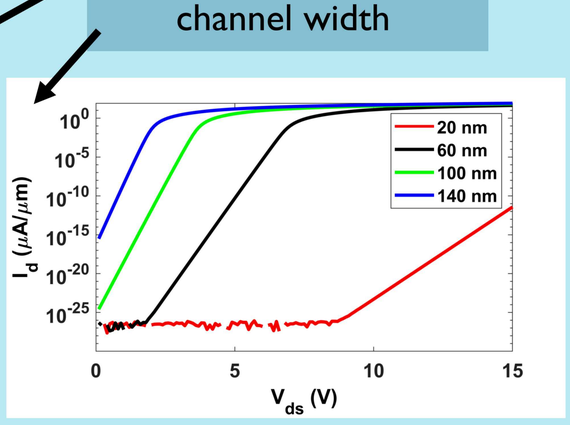


- V_G = 15 V

20, 60, 100, and 140 nm channel width



- I_D-V_D for V_G = 0 V
- At 140 nm, the channel is no longer fully depleted and the gate leaks substantially.



- I_D-V_G for V_D = 0 V
- At 20 nm, a very high gate voltage is needed to allow current through the channel.

Summary

- A 1kV, 10 A GaN MISFET device was successfully modeled.
- The channel width is a key parameter for determining operating conditions for a vertical trench gate MISFET.
- Achieving 10 A, 1 kV device requires high material quality and a gate dimension of 10 cm. No bulk or interface traps were modeled.

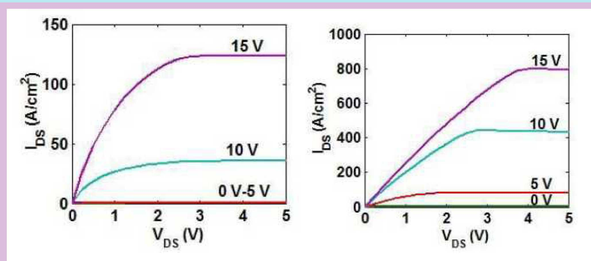


Fig. 3. Output I–V characteristics (I_{DS} – V_{DS}) for both samples, without GaN interlayer (**left**) and with GaN interlayer (**right**) at different gate voltages in steps of 5V (0V-15V).

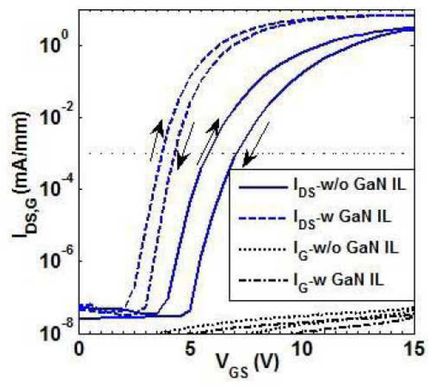


Fig. 4. Transfer I–V characteristics (I_{DS} – V_{GS}) and gate leakage (I_G – V_{GS}) characteristics for both samples, without GaN interlayer (w/o GaN IL) and with GaN interlayer (w GaN IL) at V_{DS} = 1 V.

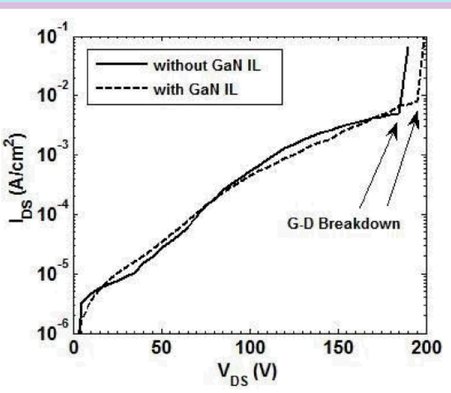


Fig. 5. Off-state characteristics for both samples, without GaN interlayer and with GaN interlayer at V_{GS} = 0 V.

OG-*FET*: An In-Situ Oxide, GaN Interlayer-Based Vertical Trench MOS*FET*

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