

MOTIVATION

An order of magnitude improvement in efficiency and dramatically reduced size are promised by a “single volume neutron scatter camera” (SVSC) that resolves multiple neutron-proton elastic scatters within a single volume of fast plastic scintillator. (Fig. 1) The spatial and temporal separations of successive neutron scattering interactions are of order 1 cm and 1 ns, causing the associated scintillations to overlap in time in a single, optically contiguous block of scintillator. Simulations using realistic physical assumptions have shown that possessing a list of photon positions and arrival times at the scintillator surface leads to a camera with useful performance^[1]. A minimal cubical experimental prototype detector to test this monolithic SVSC concept with each face instrumented by 64 photon-detecting pixels would result in 382 channels. Instrumenting that number with traditional rack-based nuclear electronics rapidly becomes challenging in cost, space and power--making a custom designed compact waveform digitizer assembly an attractive alternative. The Sandia Laboratories Compact Electronics for Modular Acquisition (SEMA) was developed to construct prototype detectors initially by mating specifically with a Photonis Planacon but is intended to be adaptable to other fast-timing pixelated photodetectors as well.

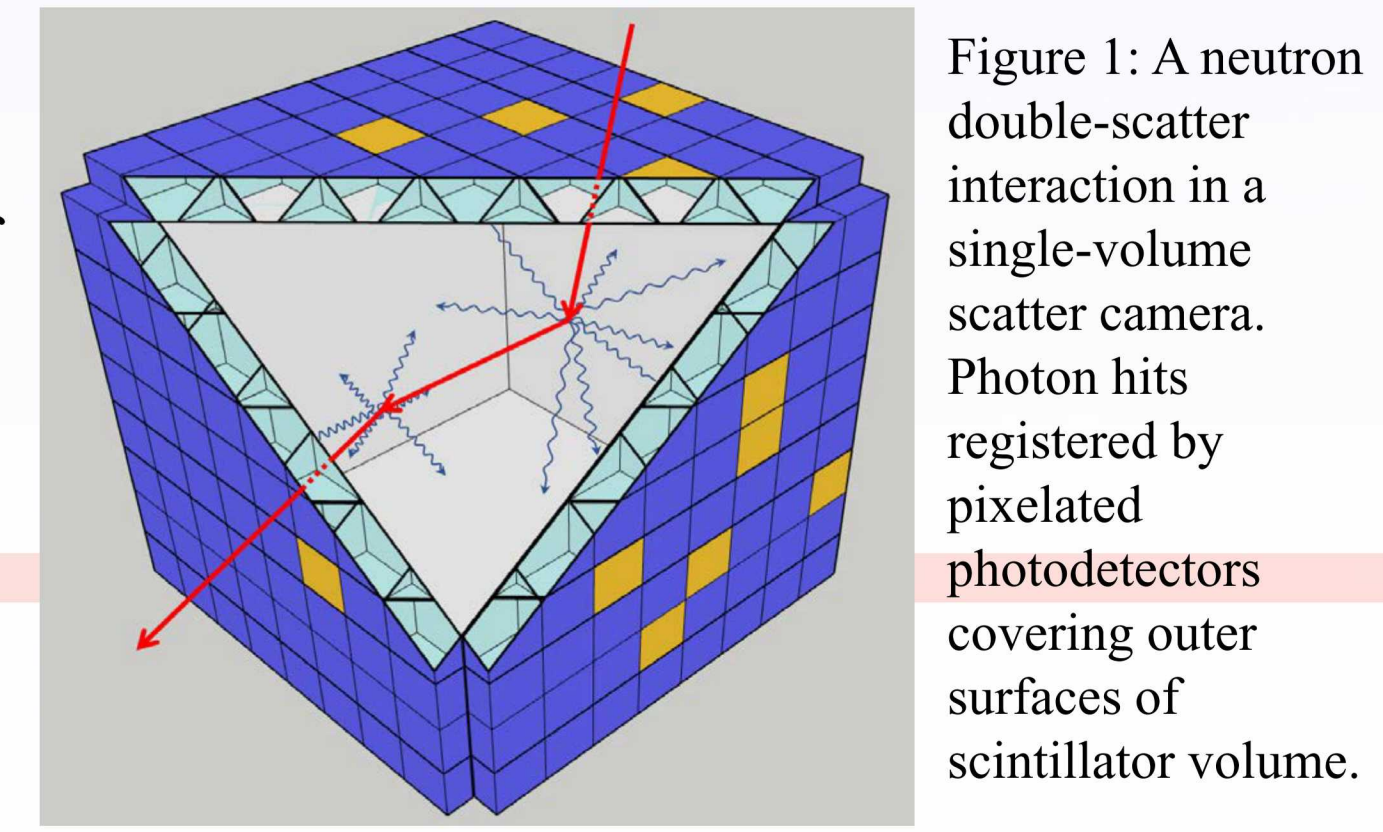


Table 1: Summary of SEMA module design parameters and measured performance values.

Number of channels	16 (+2)
Waveform sampling rate	0.7-5 GS/s
Trigger capability	external trigger
Minimum achievable dead time	32 us
Input dynamic range	1 V p-p
RMS noise	0.5 mV
Time resolution	< 30 ps
Bandwidth	~ 650 MHz (from impulse rise time)

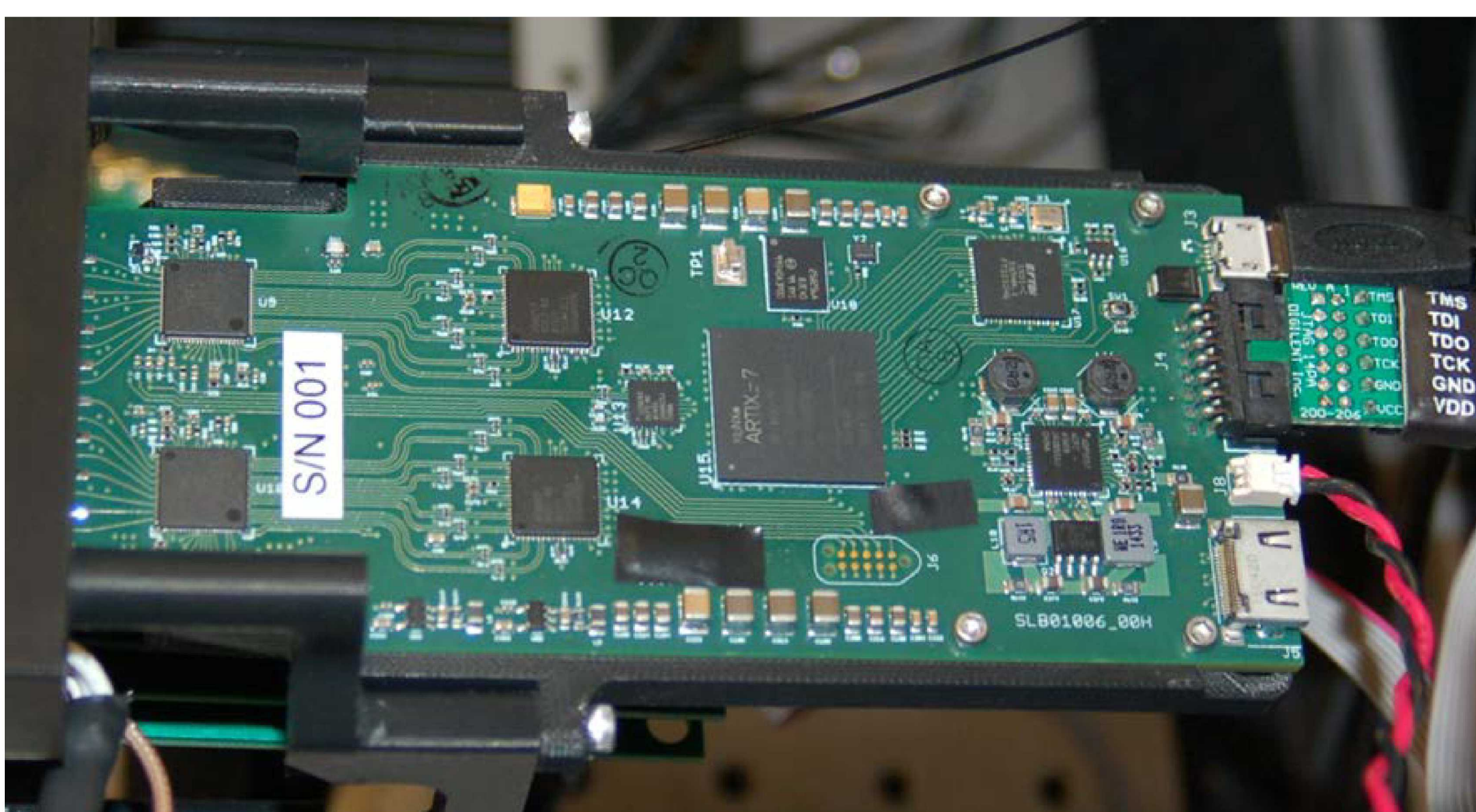


Figure 2: Photograph of top side of SEMA assembly.

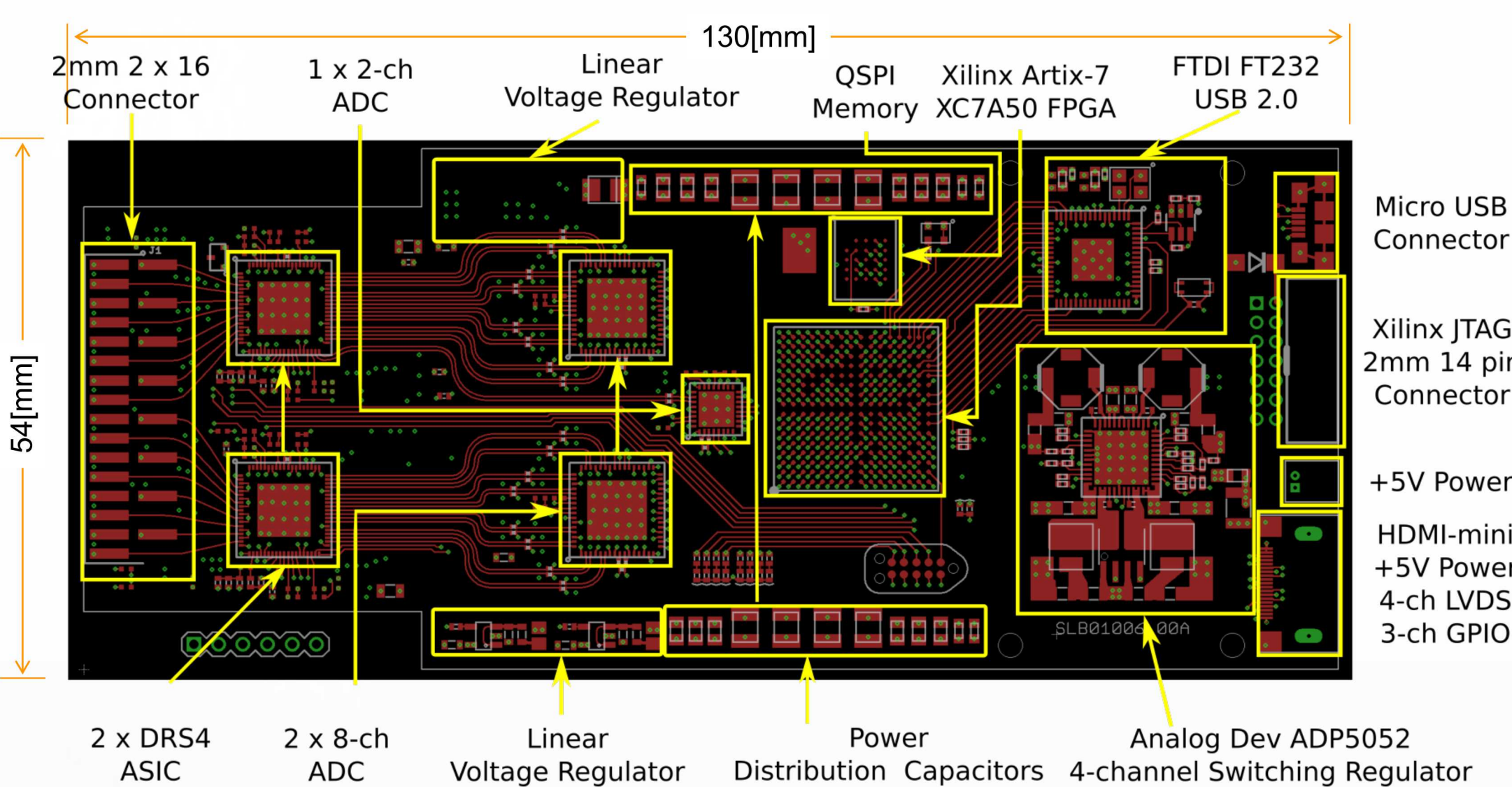


Figure 3: Annotation of some elements of SEMA assembly.

SEMA ASSEMBLY DESIGN

Digitizing waveforms to extract sub-nanosecond timing information recommends using a multi-giga-hertz sampling rate that is typically difficult to realize using commercial flash ADCs without consuming significant amounts of power and space. Switched capacitor arrays (SCA) implemented with conventional ASIC manufacturing processes offer high burst sampling rates compactly with low power by using a scheme that separates the analog sampling done with the SCA from the digital conversion process carried out by conventional ADCs later and more slowly--saving power, space and with improved quality.

Of several SCA offerings available, we chose the “Domino Ring Sampler 4” (DRS4) made by the Paul Scherrer Institut^[2]. The DRS4 offers 9 channels, each with 1024 sampling cells, up to 5 GS/s, and a way to readout all channels in parallel to reduce conversion deadtime.

The DRS4 requires external digitizers. We chose Analog Devices multi-channel 14-bit serial LVDS ADCs--2x AD9257 Octal ADCs for the 16 anodes wired to channels 1-8 of each DRS4, and 1x AD9645 Dual ADC for the 9-th channel of both DRS4s, which are reserved for timing calibration and capturing a Planacon’s MCP-out or similar photo-detector sum signal.

A Xilinx Artix-7 XC7A50T FPGA was chosen to do the digital control functions, and a FTDI FT232 chip provides a USB 2.0 interface to PC.

The diverse chip families required 7 different volt supplies, and a 16-layer PCB was arranged with care to provide each with a power/ground plane pair as well as sufficient dedicated signal layers for controlled impedance and equalized routing.

Firmware and software development required appreciable effort.

A notable design choice to save space and power eschews the inclusion of a buffer amplifier stage between each anode and its corresponding DRS4 analog input. Instead, the anodes directly drive the negative inputs and a common reference voltage the positive of each differential DRS4 input in single-ended fashion. SPICE shows gain and bandwidth are not appreciably degraded without buffer. In the case of the Planacon, its proximity to the DRS4s nearly eliminates transmission line effects of any non-uniform/non-standard impedance in this important signal segment.

The assembly includes 24 16-bit DAC channels used to set analog operating points. One channels sets the common reference bias for all DRS4 channels. 18 channels set the bias for the 16 pixel inputs and the 2 “spare” channels, these 2 dedicated to timing calibration and triggering functions. Together these 19 DAC channels enable in situ amplitude calibrations. The assembly includes a 100 MHz sine generator to accomplish in situ timing calibrations.

A mini-HDMI connector is included to utilize the four 100-ohm shielded twisted pairs and remaining single wires for inter-assembly signaling and power distribution. No attempt is expected to use the HDMI protocol itself.

AMPLITUDE CALIBRATION

The DRS4 chip exhibits unique offset and to a lesser degree gain characteristics for each capacitor in the array. Neglecting compensation via cell-by-cell calibrations presents a substantial additional noise term. Using the onboard DACs, the offset and gain correction for each cell can be determined. Figure 4 summarizes voltage gain/offset calibration steps and the resultant noise and linearity behavior. After applying corrections, the SEMA shows a ~0.5 mV RMS residual noise and deviation from linearity of less than 2 mV over a 0.7 V range, with larger deviations at higher voltages.

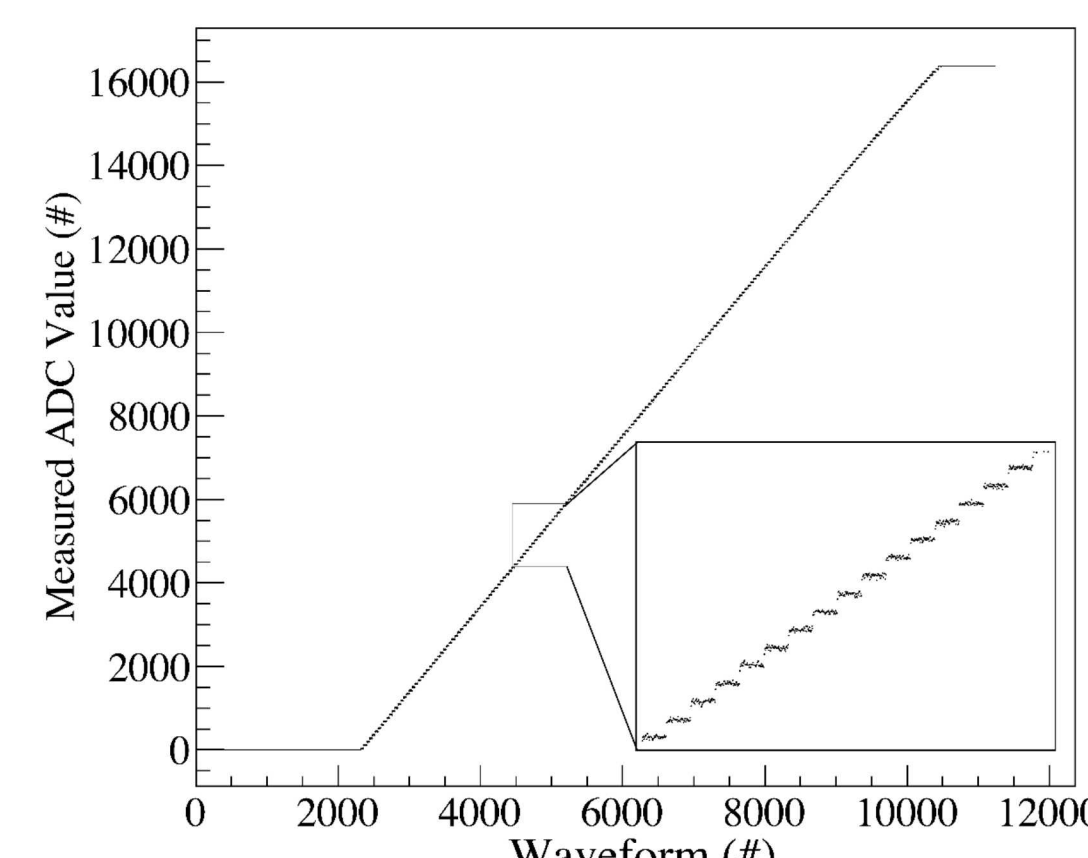


Figure 4 (a) Full history of data collected for a single cell. The steps represent holding the voltage input to the DRS4 at a constant value and recording 40 waveforms.

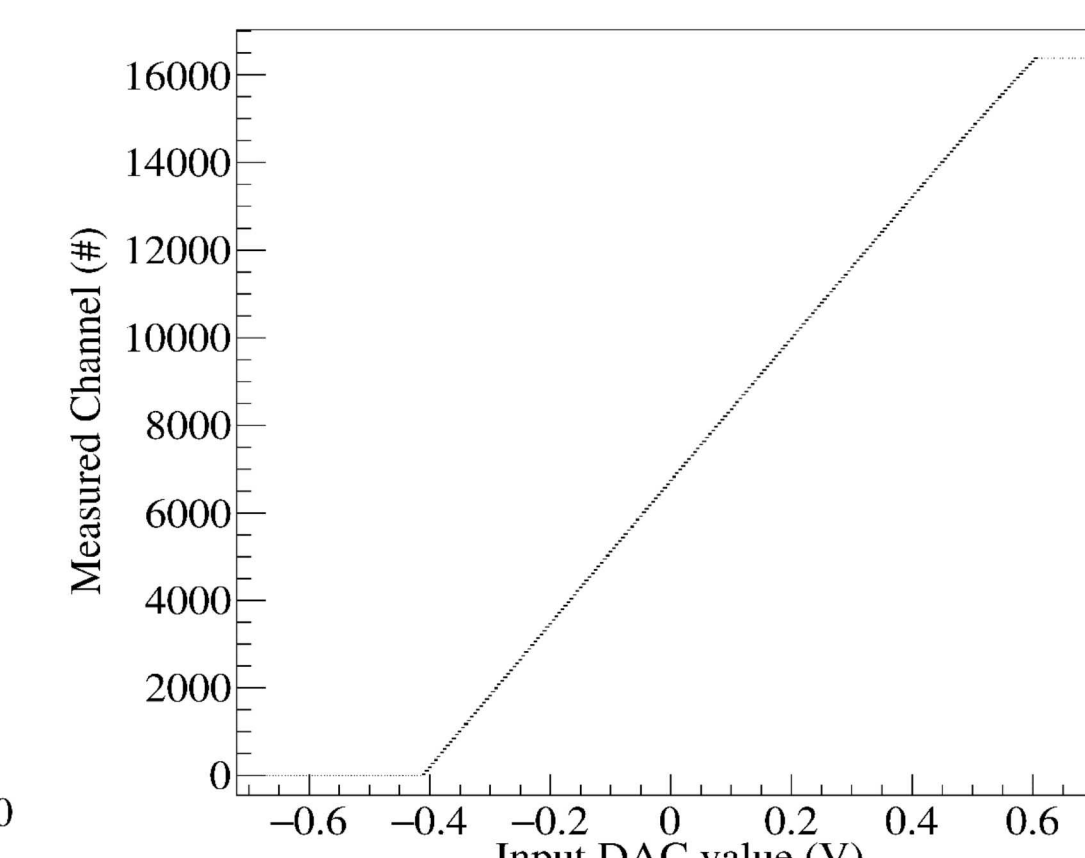


Figure 4 (b) The results of averaging each of the steps shown in Fig. 4a. A linear fit to these points determines both the zero point and slope for the given cell in the switched capacitor array. The center point of the 1 V p-p input dynamic range is adjustable. Here it was set such that the effective linear range spans -0.4 V to 0.6 V.

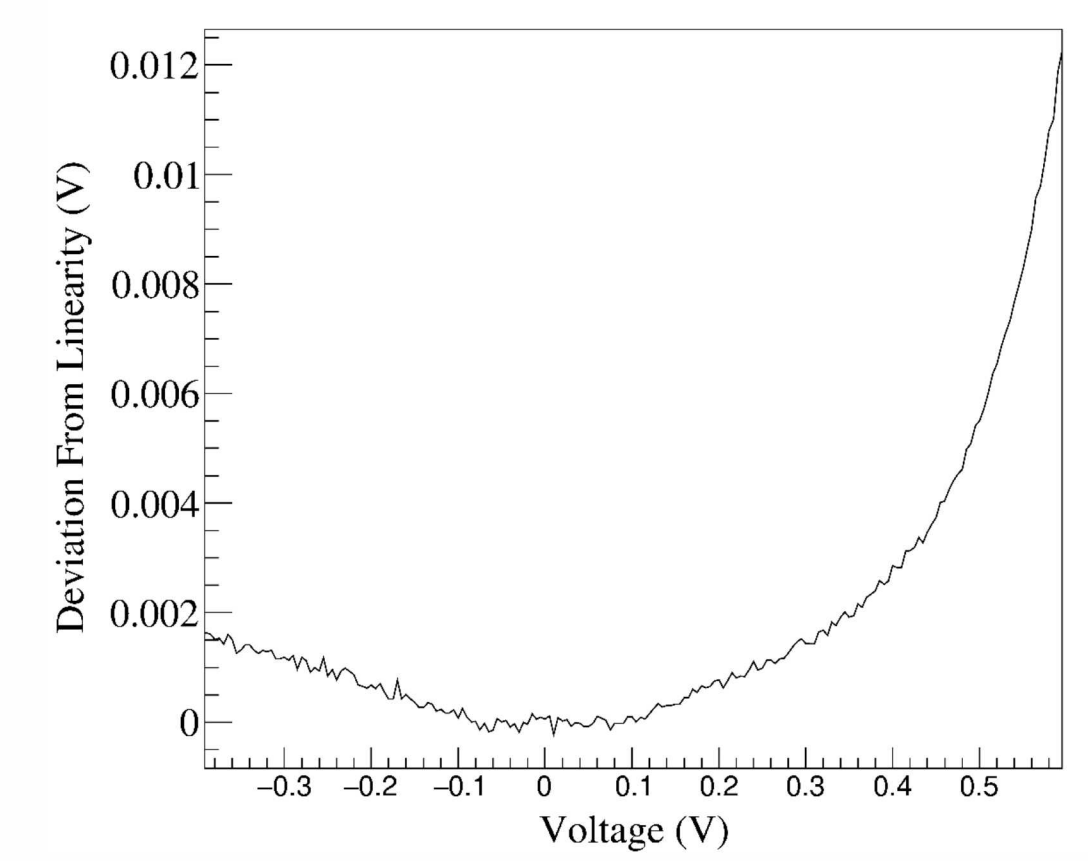


Figure 4 (c) The resultant deviation from linearity shown by comparing the calibration data with the gain and offset corrections applied to the known input voltage.

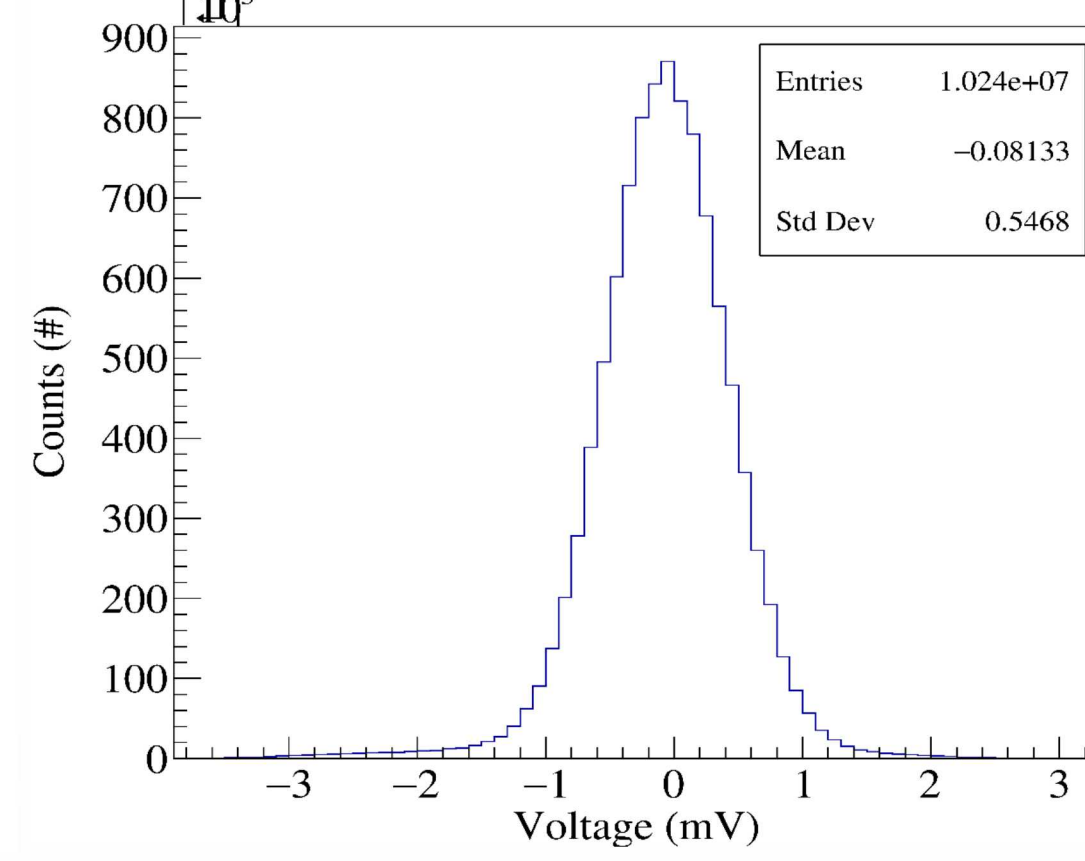


Figure 4 (d) After calibrations, a new set of 10,000 waveforms was collected with the input voltage fixed to 0. A histogram of all the observed voltage values for the 1024 cells of one channel is plotted here to represent the typical noise level after calibrations.

TIMING CALIBRATION

Similar to the amplitude response, the DRS4 chip exhibits unique timing characteristics for each capacitor in the array, which primarily manifests as a non-uniform sampling time step from cell to cell. Most of this non-uniformity comes from the domino-ring delay-line itself, and it is common to all channels of a single chip. Thus, it suffices to first order to determine the unique time steps using one channel and apply those on a corresponding cell by cell basis to the remaining channels, leaving a residual fixed pattern uncertainty on their timing of approximately 10 ps per reference [3]. The timing calibration procedure developed for the SEMA assembly was inspired by the methods outlined in references [3] and [4]. Local and global calibration procedures were developed with the goal of minimizing both differential and integral timing non-linearity and use a comparison between a known input signal and observed output voltage values, requiring the amplitude calibrations to be completed before the timing calibrations are done. The final results suggest that for times less than ~100 ns (10 periods) the standard deviation of a temporal measurement should be less than ~12 ps.

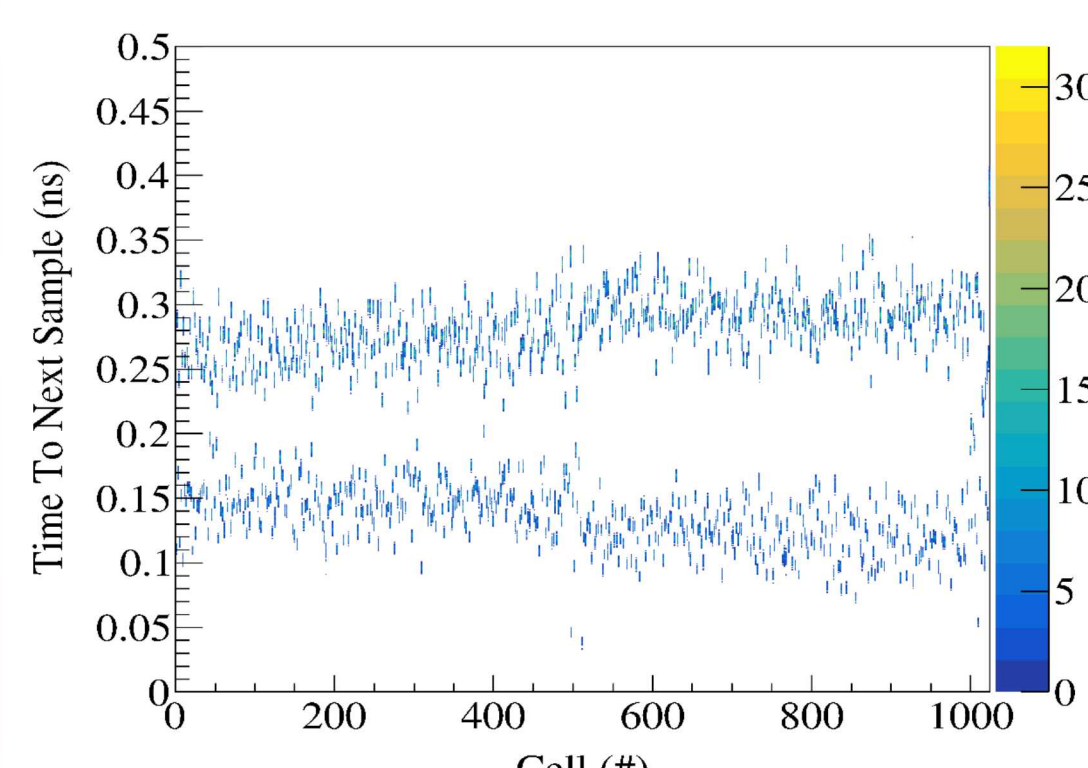


Figure 5 (a) Local calibration procedure shows DRS4’s characteristic oscillating time differentials between a small and large time step and shows a shift near the midpoint of the switched capacitor array where the difference between the distributions increases. For each cell, the mean of the distribution was taken as the local time estimate.

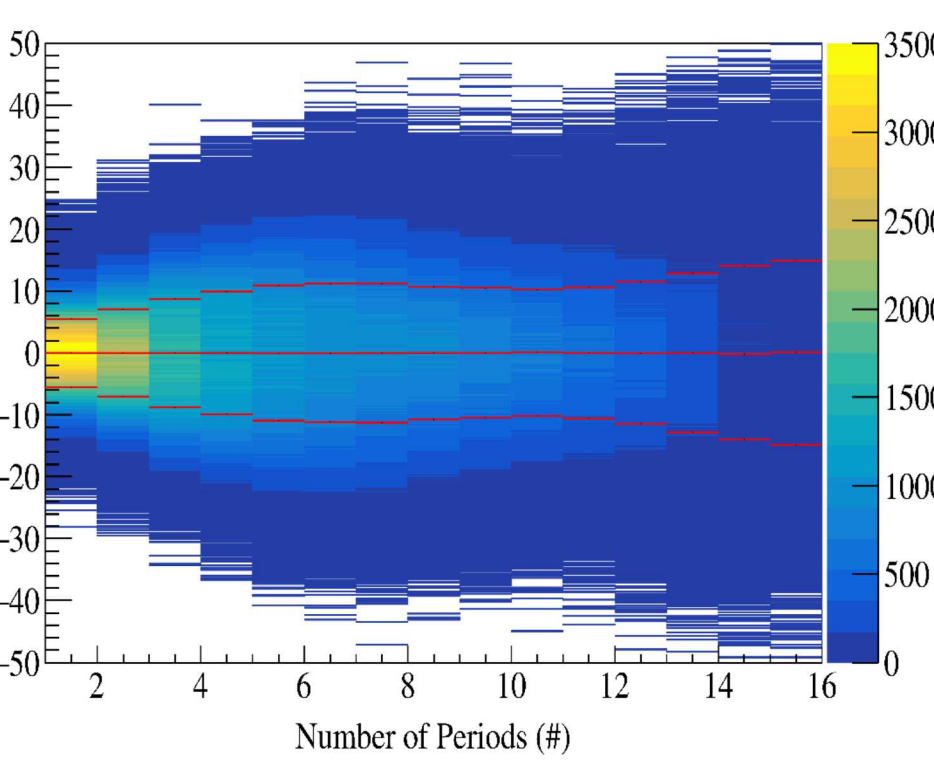


Figure 5 (d) Final time calibration. The horizontal axis is the number of periods between the zero crossings considered. The top and bottom red lines reflect the +/-1σ deviation about the mean residual time difference.

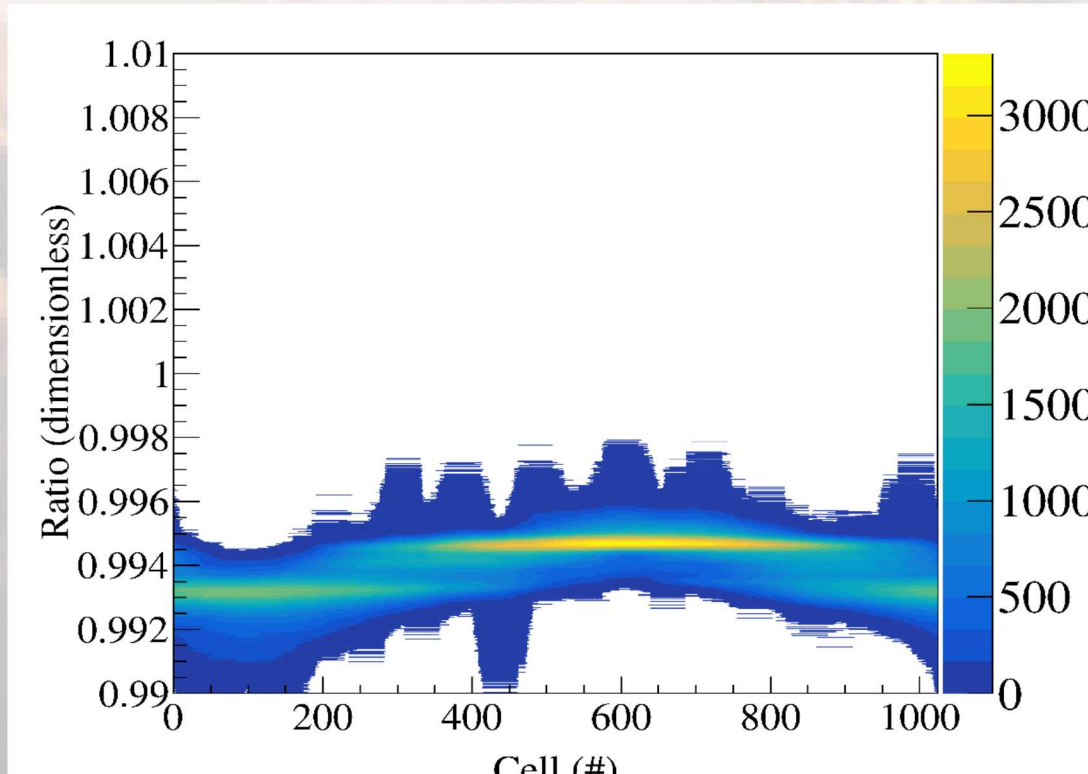


Figure 5 (b) Global calibration procedure seeded by local calibration generates an initial distribution of the ratios between expected and observed times for all combinations of zero crossings over the roughly 20 100 MHz sine wave cycles that fit within the 1024 cells at 5 GS/s.

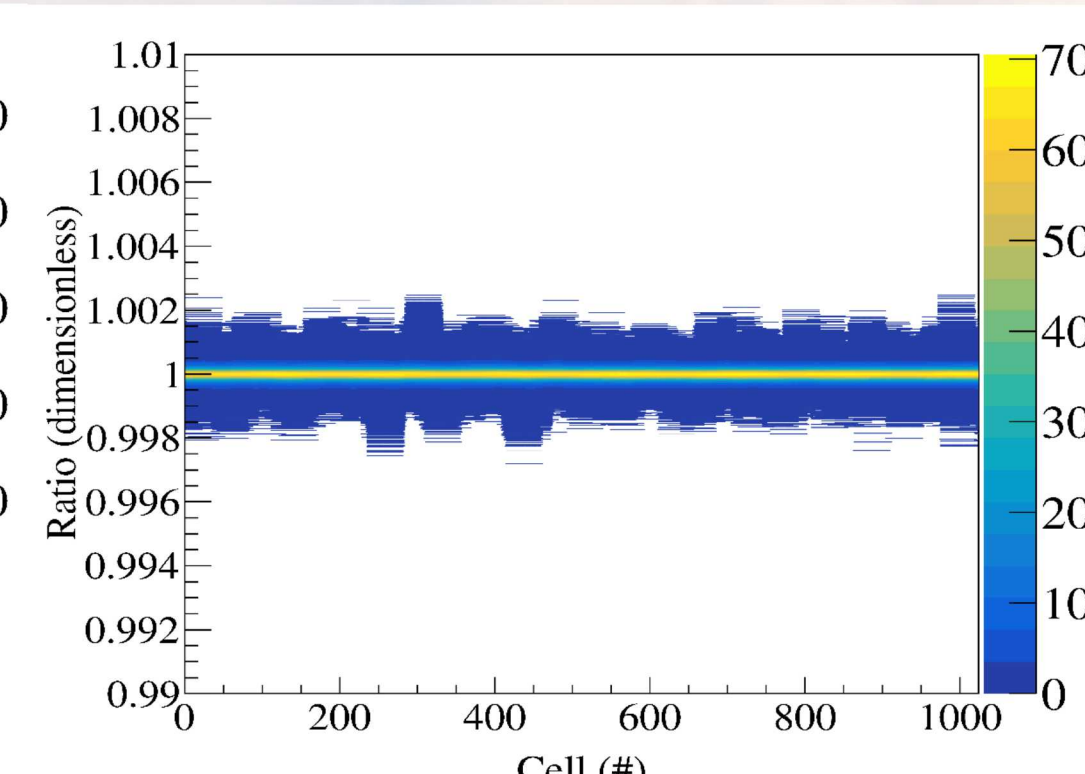


Figure 5 (c) After 80 iterations using the mean of the ratio distribution to scale the current values of the differential times for each cell. The resultant ratios are primarily distributed about one as anticipated. The observation of outliers is likely due to noise in the signal surrounding the zero crossing.

PULSE PAIR TIMING RESOLUTION

The SVSC prototype requires using numerous SEMA assemblies together in synchronized fashion, and hardware and firmware features are offered to distribute common clock and trigger signals to achieve this synchronous operation. To measure the channel-to-channel time resolution for small signals similar to anticipated single photon signals, a Photek LPG-405 ps-class laser was set to provide many photons to the photocathode of a Photek PMT-210 to provide a consistent time structure, where the bias was selected so that the amplitude was about 10 mV, similar to a single-photon signal at high gain. The signal from the PMT-210 was split and fed into two cables. One branch of the split could be delayed using an appropriate length of additional cable. The laser sync signal was connected to the trigger input of the module(s) under test. The basic setup is represented schematically in Figure 6a. The best case pulse-pair timing performance is, as expected, between channels on the same DRS4 chip, where the standard deviation of the distribution is 22.1 +/- 0.1 ps. The worst case pulse-pair timing performance is, also as expected, between channels on different SEMA assemblies, where the standard deviation of the distribution is 28.4 +/- 0.2 ps. (Fig. 6(c))

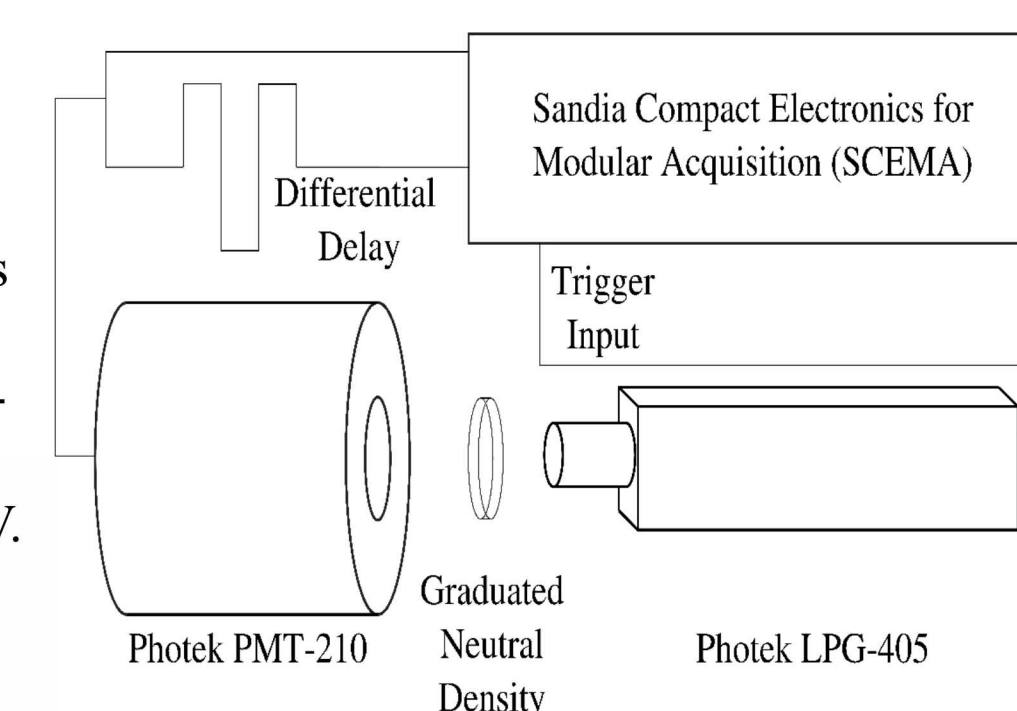


Figure 6 (a) Schematic of the basic layout for the pulse pair resolution test.

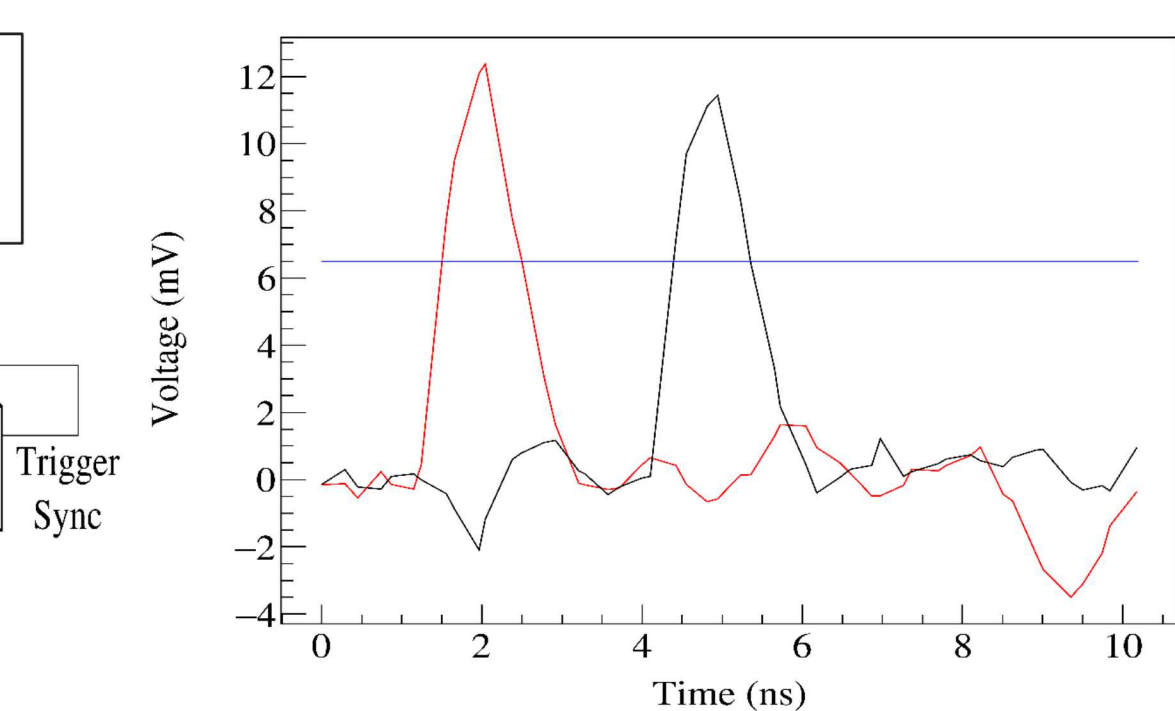


Figure 6 (b) A characteristic event from the pulse pair test using a Photek PMT-210 and a Photek LPG-405 ps-class pulsed laser. The pulse shape observed is a good approximation to the instrument response function, given that the FWHM of a PMT-210 pulse is ~130 ps.

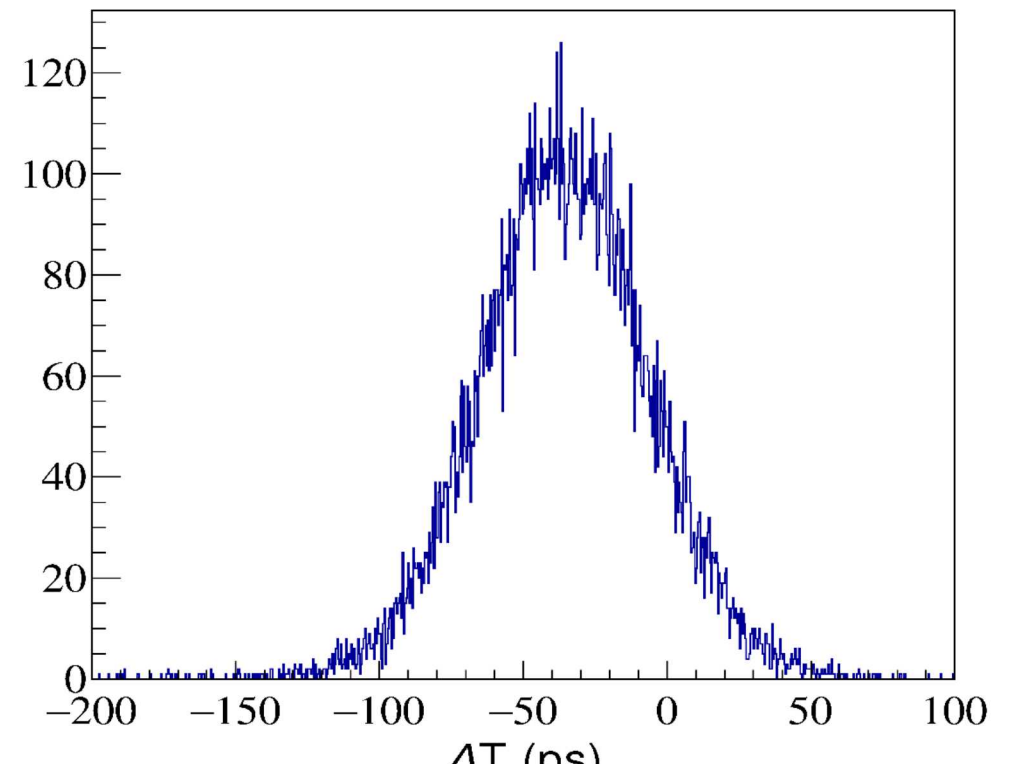


Figure 6 (c) Temporal distribution resulting from the accumulation of the time difference of events from a split pulse observed in different modules. The standard deviation, estimated using a fit to a normal distribution, is 28.4 +/- 0.2 ps. This too is much lower than the anticipated single photon time jitter for the pixelated photodetectors under consideration.

SINGLE PHOTON TIMING RESOLUTION

To demonstrate SEMA’s single-photon detection performance, the laser and PMT-210 were adjusted such that nearly all events were single photons with mean pulse height of 10 mV to match pulse pair timing tests. A LeCroy Waverunner 640zi oscilloscope sampling at 40 GS/s was used as a known, high performance digitizer as a point of comparison, and its test setup was verified to substantially reflect a combination of the PMT-210’s single-photon transit time spread and the laser pulse width. From Figure 8, the standard deviation of the distribution for the Waverunner and SEMA are 28.5 +/- 0.2 ps and 31.5 +/- 0.5 ps, respectively, establishing that the design goal of having the SEMA be a small contribution to the temporal error of single-photon detection using fast photodetectors was met.

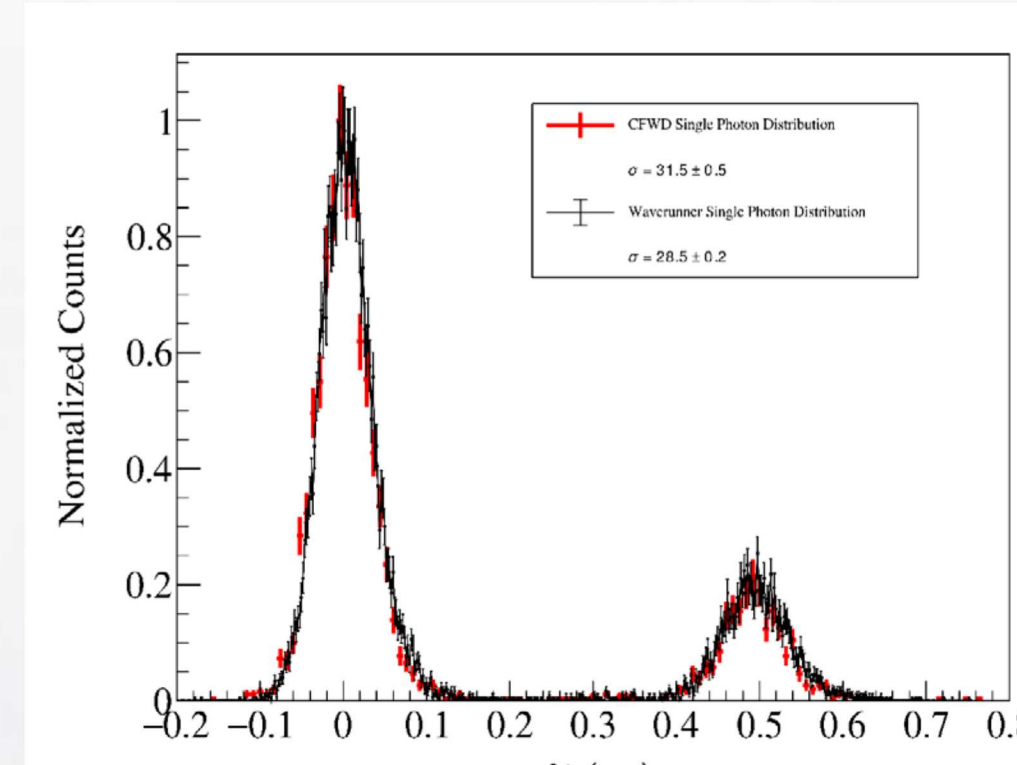


Figure 8: Comparison of distributions resulting from measuring the time difference between the laser sync signal of a Photek LPG-405 laser and a single photon observation on a Photek PMT-210. SEMA response is red. LeCroy Waverunner 640zi 40 GS/s oscilloscope response is black. In case you were wondering, the second peak is an artifact of the LPG-405 laser.

REFERENCES

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