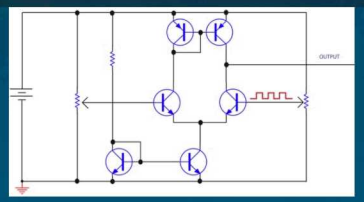
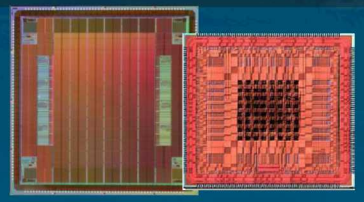
SAND2018-12739C

Xyce: Open Source Simulation for Large-Scale Circuits





PRESENTED BY

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The Xyce™ Parallel Electronic Simulator Analog Circuit Simulator

SPICE-Compatible syntax (Berkeley 3f5)

Two versions, **Serial** and…

Distributed Memory Parallel (MPI-based)

Unique solver algorithms

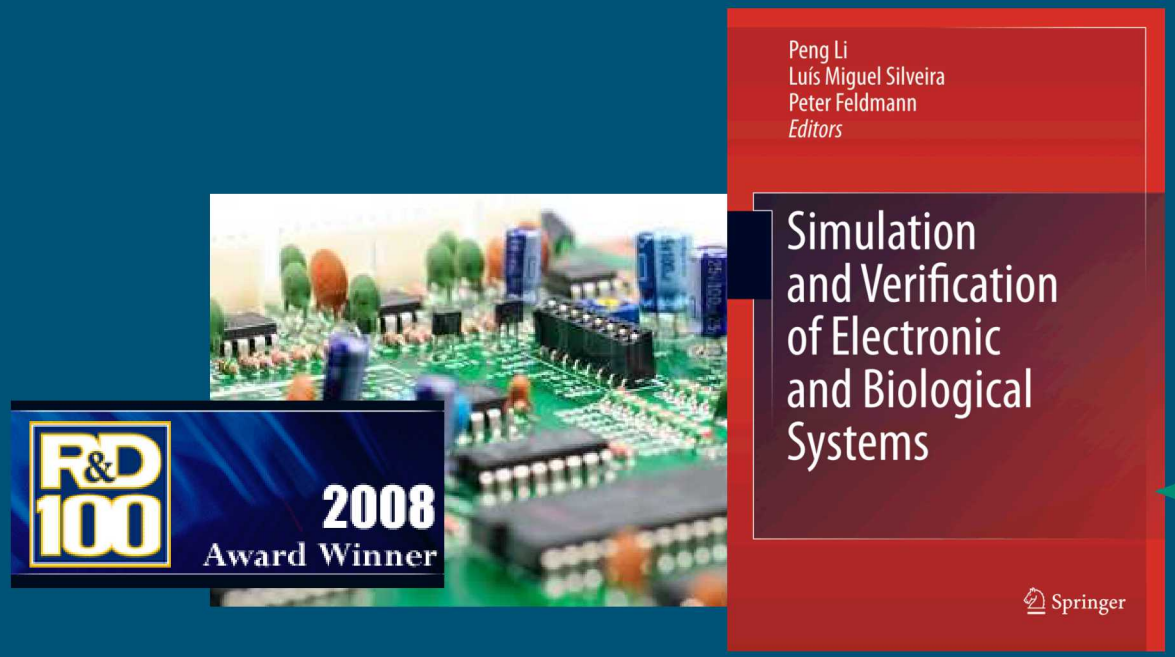
Industry standard models

Non-traditional models
- Neuron/synapse
- TCAD (PDE-based)

Open Source, GPLv3
- Since September of 2013 (Xyce 6.0)

Xyce Release 6.10
- November, 2018; 23rd major release
- >3,900 external downloads

http://xyce.sandia.gov



Keiter, et al., "Parallel Transistor-Level Circuit Simulation"

Xyce Capabilities

Typical

DC, Transient, AC, Noise
- .DC, .TRAN, .NOISE, .AC (and .STEP)

Post Processing:
- Fourier transform of transient output (.FOUR)
- Post-simulation calculation of simulation metrics (.MEASURE)

Output (.PRINT)
- Text Files (tab or comma delimited)
- Probe (PSPICE)
- Gnuplot, TecPlot, RAW (SPICE 3f5)

Analog Behavioral Modeling

Expressions, functions, parameterizations…

Others

Harmonic Balance Analysis (.HB)
- Steady state solution of nonlinear circuits in the frequency domain

Random Sampling Analysis
- Executes the primary analysis (.DC, .AC, .TRAN, etc.) inside a loop over randomly distributed parameters

Sensitivities
- Computes sensitivities for a user-specified objective function with respect to a user-specified list of circuit parameters ($\partial O/\partial p$…)
- DC or Transient
- E.g., an output voltage's dependence on a capacitance

Xyce-isms

Xyce defaults are conservative

- The industry standard is, "The simulator must never fail to provide an answer"
- …even if it's wrong.
- The Xyce philosophy: provide a numerically accurate answer, and fail if asked to do something "wrong."

Simulations in Serial vs. MPI Parallel

- Distributed parallelism can take more tuning:
  - device distribution, direct vs. iterative linear solvers,…
- Very large parallel simulations are "hard" (need to find the "right" linear solver)
- Leverages Sandia's Trilinos HPC solver framework

Xyce is the simulator (like HSPICE, SmartSpice, Spectre,…)

- There is no Schematic Design/Capture Front End (like Virtuoso, Tanner AMS, Gateway,… i.e., a GUI)
- …for now?

Others:

- Xyce is not (at the moment) 100% compatible with any other simulator
- There may be an expected feature that we don't (yet) support; e.g., .OP functionality is limited

Near-Term Work

Commercial Simulator Compatibility
- (netlist compatibility is often easier than feature compatibility; we are working on both)
- PSPICE netlist conversion tool (Sandia-only at the moment)
- HSPICE compatibility: under development (netlist and feature)
- Spectre compatibility: targeted for future development

PDK Support
- Strongly tied to simulator compatibility (HSPICE is the current path)
- Initially targeting Global Foundries 14 nm

Mixed-signal support (Verilog via VPI, VHDL via VHPI)

S-parameter analysis implementation

Build system moving to CMake

Performance Improvements
- Industry Standard Compact Models: speed improvements (Verilog-A compiler based on ADMS)
- Solver performance: solvers for parallel, choice of default parameters

Xyce Team Acknowledgements

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