AMS Verification for Enabling POSH SoCs

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Designs Thrust

Overview

Design methodology in support of large-scale, highly complex SoC technologies is crucial to support future Department of Defense (DoD) applications. One strategy for efficiently enabling future systems is to develop a common open-source hardware ecosystem; but doing so will require software and hardware verification tools that are substantially more powerful than those presently available. For this project, we intend to produce several open-source software and prototyping tools targeted at large mixed-signal design. This is an enabling technology for the rest of the POSH program.

Background

AMS/RF Verification: Analog/Mixed-Signal (AMS) and RF subsystems have become an essential part of most integrated systems today.

- With the trend towards digitally-assisted analog/RF, digital functionality not only surrounds, but is also present within analog/RF subsystems.
- Design, validation and debugging of mixed-signal systems can be very challenging because “analog issues” such as variability, noise/interference, nonlinear analog dynamics, analog waveshapes, timing/phase lags, etc.
- For simulation of mixed-signal systems, simulation of the analog portions of the system are a significant bottleneck that cannot be avoided, as verification methods often require analog simulation results as an input.

Analog/RF Simulation in SPICE-style Simulators

- Traditional circuit simulation solves a coupled set of nonlinear DAEs

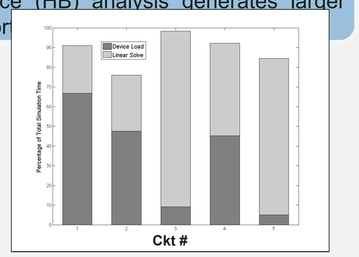
$$f(x(t)) + \frac{dq(x(t))}{dt} = b(t),$$

which does not scale well beyond tens of thousands of unknowns due to reliance on a large single matrix that is treated by direct matrix solvers.

- SPICE-accurate simulation is often a prohibitive bottleneck, mitigated by only simulating individual modules or relying on commercial fast-SPICE solvers.
- “Fast-SPICE” simulators rely on circuit-level, hierarchical partitioning algorithms to perform faster, large-scale circuit simulation. The approximations inherent to such algorithms can break down for modern feature sizes, especially post-layout.
- The analog runtime scales super-linearly with increasing circuit size, and this issue is present in all varieties of analog circuit simulator.
- For RF and microwave applications, the scalability problem can be even worse than for transient because harmonic balance (HB) analysis generates larger matrices that lack sparsity for the nonlinear por

TABLE I
CIRCUITS: MATRIX SIZE(N), CAPACITORS(C), MOSFETS(M), RESISTORS(R), VOLTAGE SOURCES(V), DIODES (D).

Circuit	N	C	M	R	V	D
ckt1	15622	7507	10173	11057	29	0
ckt2	25187	0	71097	0	264	0
ckt3	116247	52552	69085	76079	137	0
ckt4	688838	93	222481	176	75	291761
ckt5	1944792	400234	211486	795827	36100	199992



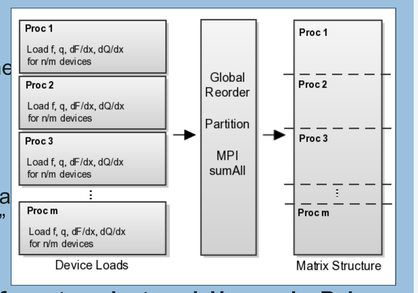
Innovation

Produce an efficient, open-source, parallel analog simulator which can be used as part of the tool flow for analog-mixed signal circuits.

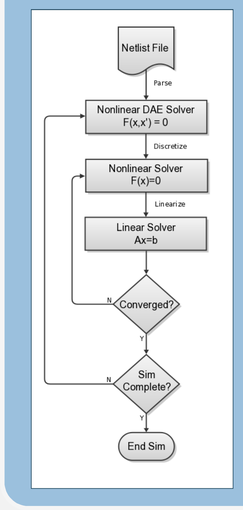
- Provide a simulator, based on the Xyce circuit simulator (https://xyce.sandia.gov), that will reliably and robustly simulate very large integrated circuits (>1M devices) for both transient and Harmonic Balance analysis. [**AMS/RF Simulation. (POSH TA-1. L2)**]
- Provide the ability to operate as a “true-SPICE” parallel simulator (for accuracy), while integrating hierarchical “fast-SPICE” techniques (as needed) for scalability.
- Leverage modern computing hardware and infrastructure (inexpensive computer clusters, multi-core technology, and cloud computing) to mitigate the analog bottleneck.

The Xyce Parallel Circuit Simulator is a SPICE-style analog circuit simulator, developed from-the-ground-up using a distributed memory paradigm, that provides a modular framework for developing state-of-the-art continuation algorithms, time-integration methods, preconditioned linear solvers, and parallel partitioning techniques. [1]

- **Xyce separates device distribution from matrix partitioning**
  - Cost of device evaluation unrelated to matrix partitioning
  - Enables each to separately determine the distribution that is efficient for communication and computation.
  - Hierarchical information will be leveraged in either distribution to ena efficiencies or integrate “fast-SPICE” techniques.



- **Xyce uses a modular design to perform transient and Harmonic Balance analysis**



- Provides a suite of robust continuation methods to assist initial condition calculations.
- Provides direct and iterative linear solvers to balance robustness and speed.
  - For very large integrated circuits, the bulk of the computational time is spent in solving linear systems.
  - Accuracy of direct matrix solvers is rarely needed in either transient or Harmonic Balance analysis.
  - Iterative linear solvers can enable scalable circuit simulation, dependent upon preconditioning strategy.
  - Hybrid direct-iterative techniques are promising and robust, map well to hierarchical structure in circuit matrices.

Impact

Contribute to the open-source hardware ecosystem by leveraging a history of scalable simulation research and integration of models for modern technology nodes.

- **AMS/RF Simulation. (POSH TA-1. L2):** *Deliver open-source tools, software, documentation and example use cases for other teams and POSH performers.*
- **Xyce has already succeeded in performing scalable simulation of postlayout ASICs with >1M devices [2] and a history of developing specialized parallel linear solvers [3,4] to enable efficient simulation on modern architectures.**

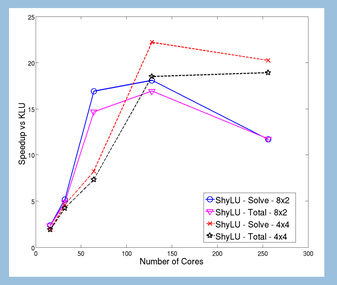


TABLE III
COMPARISON OF TOTAL LINEAR SOLVE TIME (SEC.) OF VARIOUS SPARSE DIRECT SOLVERS FOR OUR TEST CIRCUITS; (-) INDICATES SIMULATION FAILED TO COMPLETE.

	ckt1	ckt2	ckt3	ckt4	ckt5
KLU	**80.8**	162.2	9381.3	7060.8	**14222.7**
PARDISO (16)	128.6	**105.3**	**715.0**	**6690.5**	-
SuperLU	-	10294.1	-	-	72176.8
SuperLU_Dist (16)	-	-	-	-	-

Ckt5: 1.6M devices, 1.9M unknowns. Strong scaling of Xyce simulation time and linear solve time (ShyLU) for different configurations of MPI Tasks X Threads per node.

DAPRA POSH project first 6 months:

- Emphasis on process nodes of interest to DAPRA IDEA/POSH
- 7nm, 14nm GF/TSMC
- BSIM CMG model implementation/calibration
- Emphasis on circuits based on asynchronous logic (Yale)
- Parallel scaling at these nodes

Mixed signal

- Support for VPI interface
- Link to Yale discrete event simulator
- Xyce version 6.10 to be released in fall 2018 (GPL license)

References

- **[1]** "Parallel transistor-level circuit simulation," Eric R. Keiter, Heidi K. Thornquist, Robert J. Hoekstra, Thomas V. Russo, Richard L. Schiek and Eric L. Rankin, in *Advanced Simulation and Verification of Electronic and Biological Systems*, Peng Li, Luís Miguel Silveira, and Peter Feldmann, Eds. New York, NY: Springer, 2011, ch. 1, pp. 1-21.
- **[2]** "A Hybrid Approach for Parallel Transistor-Level Full Chip Circuit Simulation," Heidi K. Thornquist and Siva Rajamanickam, in Daydé M., Marques O., Nakajima K. (eds) *High Performance Computing for Computational Science – VECPAR 2014*, Lecture Notes in Computer Science, vol 8969. Springer, Cham.
- **[3]** "A parallel preconditioning strategy for efficient transistor-level circuit simulation,” Heidi K. Thornquist, Eric R. Keiter, Robert J. Hoekstra, David M. Day and Erik G. Boman, in *IEEE/ACM Int. Conf. Computer-Aided Design (ICCAD)*, San Jose, CA, 2009, pp. 410–417.
- [4]"Basker: A Threaded Sparse LU Factorization Utilizing Hierarchical Parallelism and Data Layouts," J. Booth, S. Rajamanickam and H. Thornquist, in *Proceedings of the 2016 IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW)*, Chicago, IL, 2016 pp. 673-682.

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