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Investigation of interfacial impurities in m-plane GaN regrown p-n junctions for high-power vertical electronic devices

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arpa·e CHANGING WHAT'S POSSIBLE

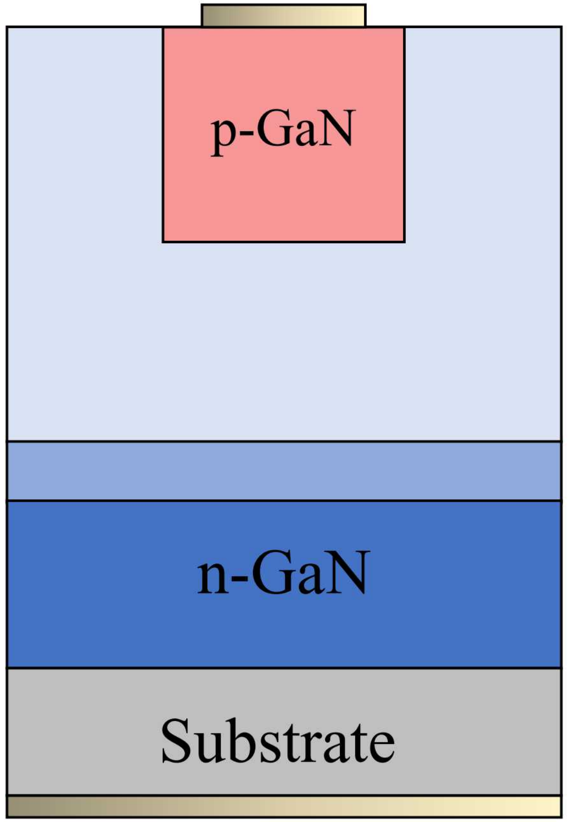
CHTM

Outline

- ❑**Background –** The appeal of gallium nitride for power electronics devices
- ❑**First Experiment** – Induction of interfacial impurities
- ❑**Second Experiment** – Effect of interfacial impurities on p-n diodes
- ❑**Third Experiment** – Effect of wet etch treatment on interfacial impurities and p-n diodes
- ❑**Conclusion**

Gallium Nitride for Power Electronics

- Gallium nitride is rapidly becoming an important candidate for succeeding silicon as a high-power electronics material
- The interest in gallium nitride for optoelectronics has led to important developments that benefit gallium nitride for power electronics, e.g. high-quality substrates.
- Gallium nitride possesses a bandgap (3.4 eV) more than 3 times that of silicon (1.12 eV), allowing it to operate at higher temperatures than silicon [1]
- Gallium nitride possess a larger critical electric field (3.3×10^6 V/cm) than silicon (0.3×10^6 V/cm) [1]
  - Allows for higher Baliga Figure of Merit
  - $BFOM \propto E_c^3$ [1]
  - $BFOM = \frac{V_{BR}^2}{R_{on}}$ [2]



[1] Flack, T. et al., Journal of Electronic Materials 45 (2016).

[2] Ohta, H. et al., IEEE Electron Device Letters 36(11), 1180–1182 (2015).

Applications

Wind Turbines

Ship Propulsion Systems

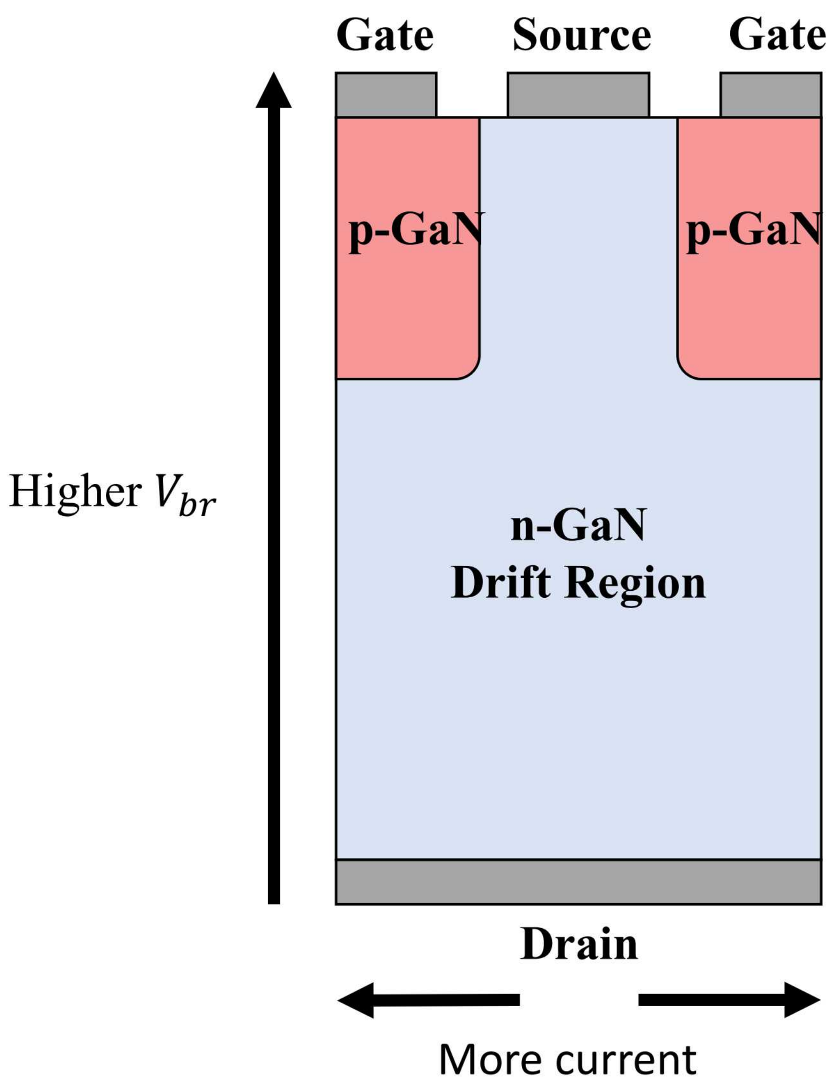
Electric Grid

Solar Inverters

Consumer Electronics

Data Centers

GaN Power Device Architectures



- Vertical geometries are preferred over lateral geometries for power devices for two reasons
  - Increase the breakdown voltage V_{br} by growing a thicker drift region
  - Increase current handling by designing devices with wider lateral dimensions
- Vertical Junction Field Effect Transistor (VJFET)
  - Applying a bias to the gate terminals modifies the depletion region between the p-GaN regions allowing the modulation of current flowing through the source and drain.
  - Simulations by researchers from Arizona State University demonstrated a Vertical Cavity JFET achieving $V_{br} = 1260\ V$ and $R_{on} = 5.2 m\Omega \cdot cm^2$ for a drift region of 11 µm [3]. Compares well with other devices.
    - Performs similarly to a SiC MOSFET by Mitsubishi [4]:

$$V_{BR} = 1200\ V, R_{on} = 5\ \text{m}\Omega \cdot cm^2$$

[3] Ji, D. and Chowdhury, S.,IEEE Transactions on Electron Devices 62(8), 2571–2578 (2015).

[4] Miura, N. et al., 2006 IEEE International Symposium on Power Semiconductor Devices and IC’s, 1–4 (2006).

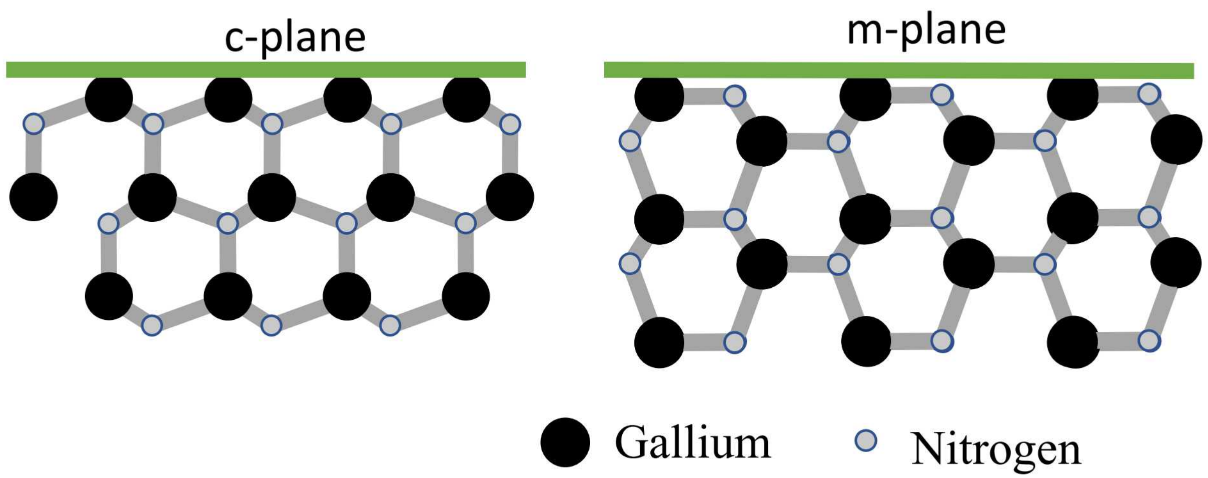
Concerns on Impurity Incorporation

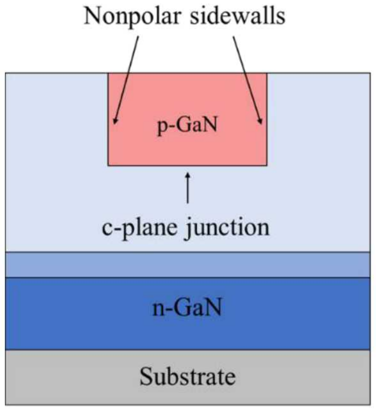
- GaN devices with complex designs such as JFETs often require selectively doped regions embedded into the device.
  - Such selectively doped regions are achieved by selective etch then regrowth of the embedded region.
  - p-n junctions at these regrowth interfaces show considerable leakage currents

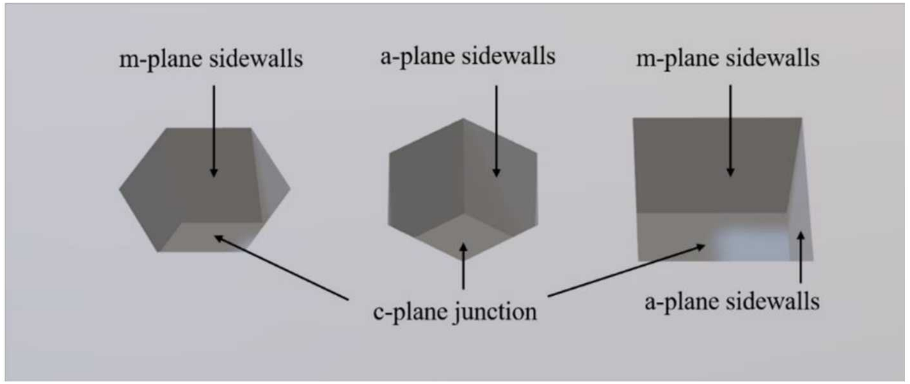
- Impurity incorporation from shallow dopants oxygen and silicon, or the deep level acceptor carbon at these regrowth interfaces might be a factor in the leakage currents.

- Further, studies have shown that different substrate orientations such as m-plane incorporate impurities differently than c-plane. This is possibly due to the higher density of nitrogen sites [5-7].

- For that reason, it is important to consider the contribution that non-basal sidewalls might have to the leakage current.





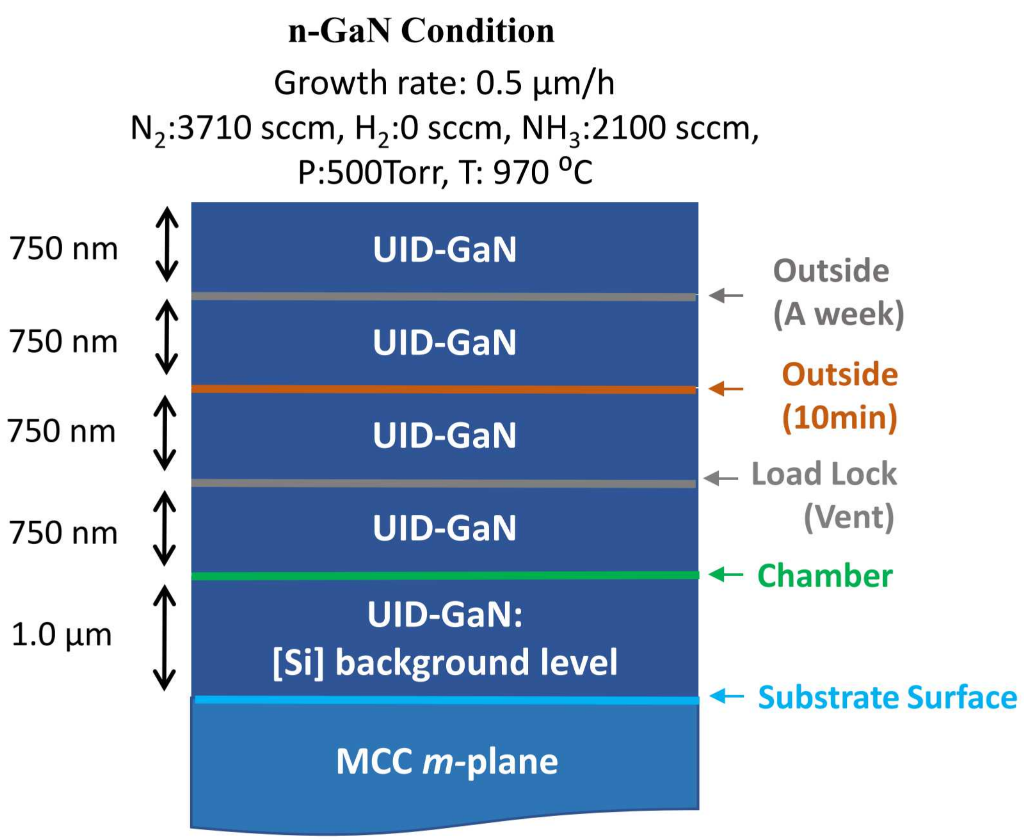


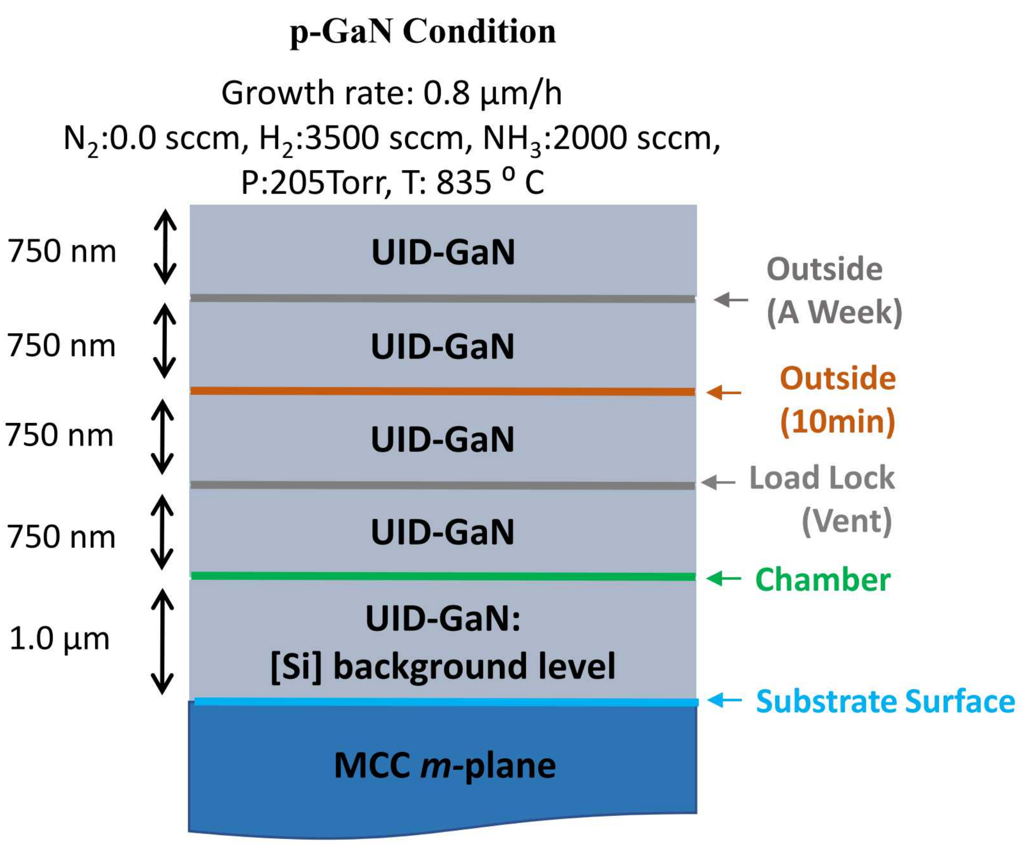
[5] Fichtenbaum, N. A. et al., Journal of Crystal Growth 310(6), 1124–1131 (2008).

[6] Cruz, S. C. et al., Journal of Crystal Growth 311(15), 3817–3823 (2009).

[7] Browne, D. A. et al., Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films 30(4), 041513 (2012).

Experiment 1-Induction of interfacial impurities



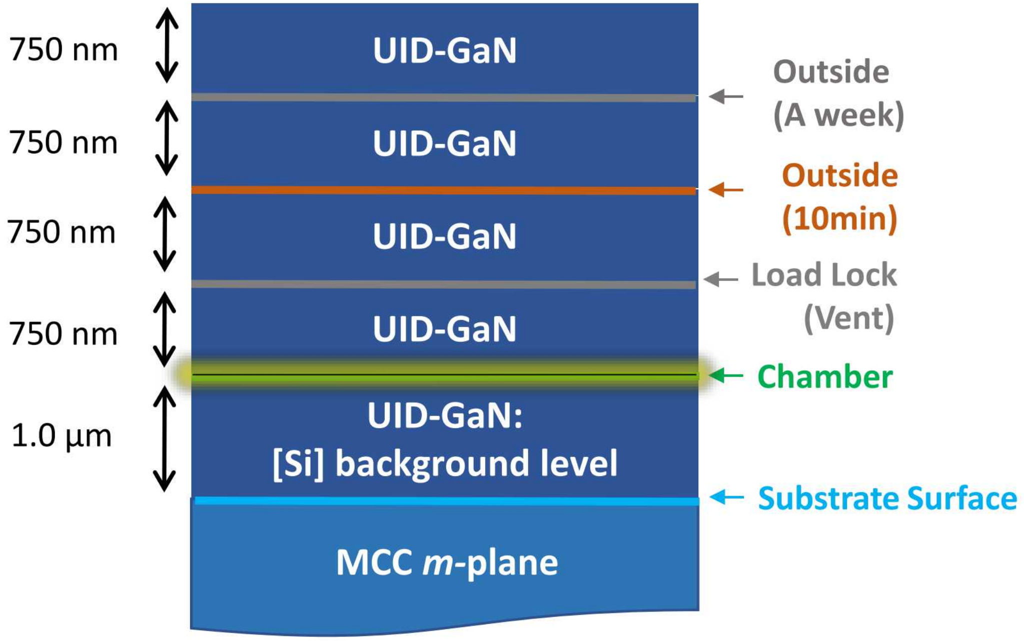


- ❑ How do growth interruptions and re-initiations affect impurity levels?
- ❑ How does regrowth affect impurity levels?
- ❑ How do growth conditions affect impurity levels?
- ❑ No SiH_4 or Cp_2Mg flowed into the chamber

Experiment 1-Induction of interfacial impurities

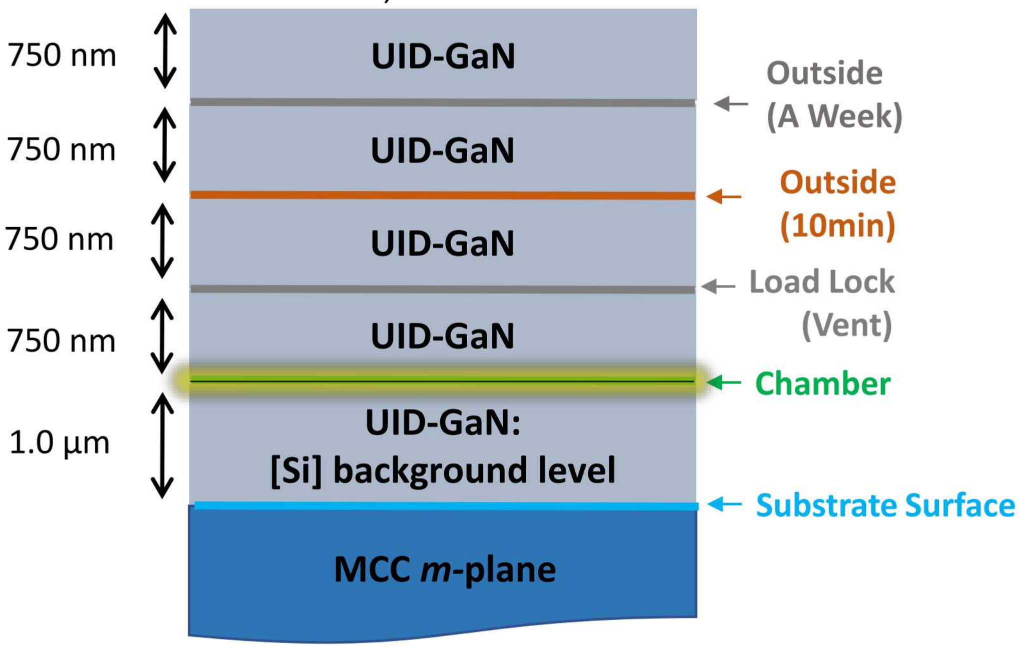
n-GaN Condition

Growth rate: 0.5 µm/h
N_2:3710 sccm, H_2:0 sccm, NH_3:2100 sccm,
P:500Torr, T: 970 °C



p-GaN Condition

Growth rate: 0.8 µm/h
N_2:0.0 sccm, H_2:3500 sccm, NH_3:2000 sccm,
P:205Torr, T: 835 ° C



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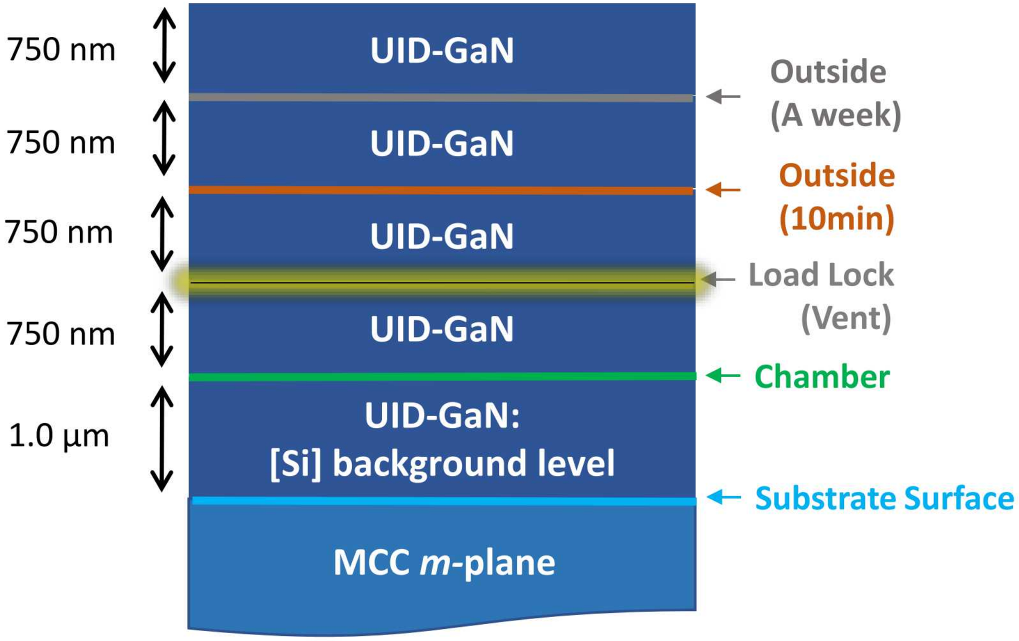

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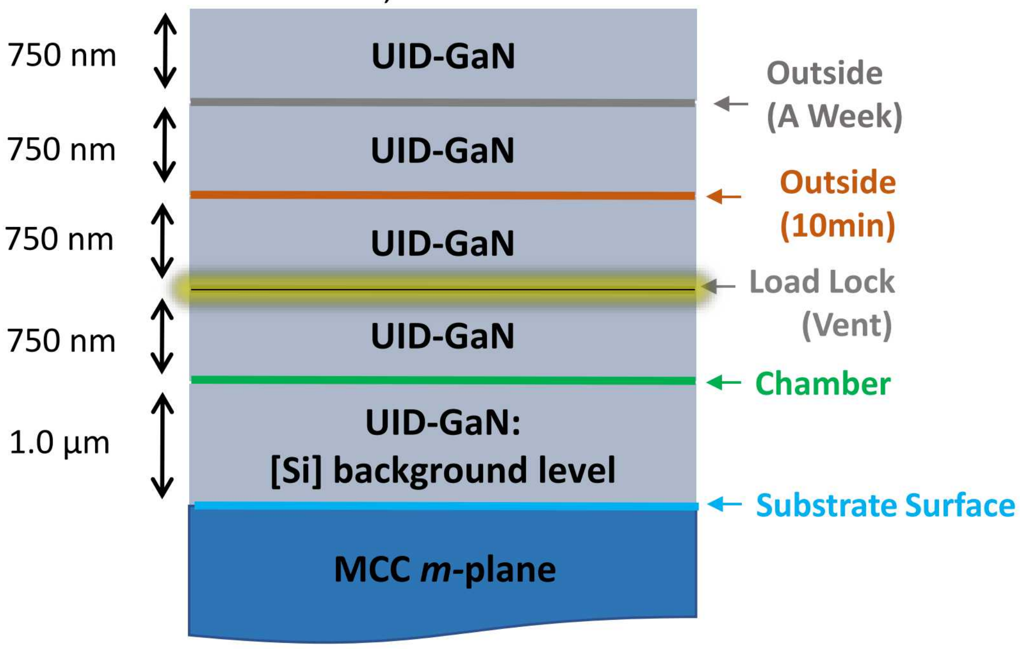

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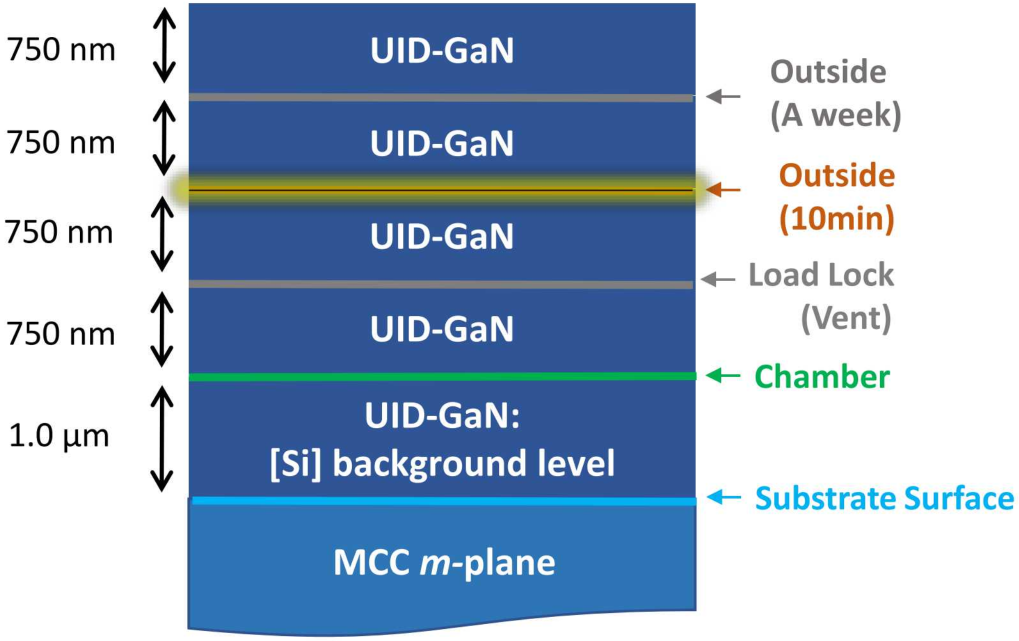

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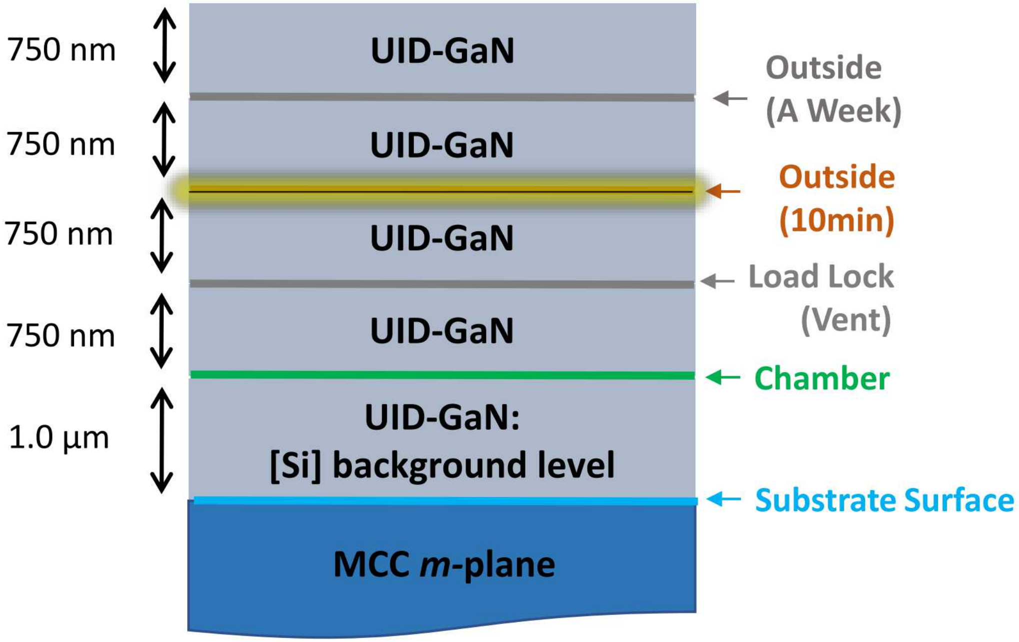

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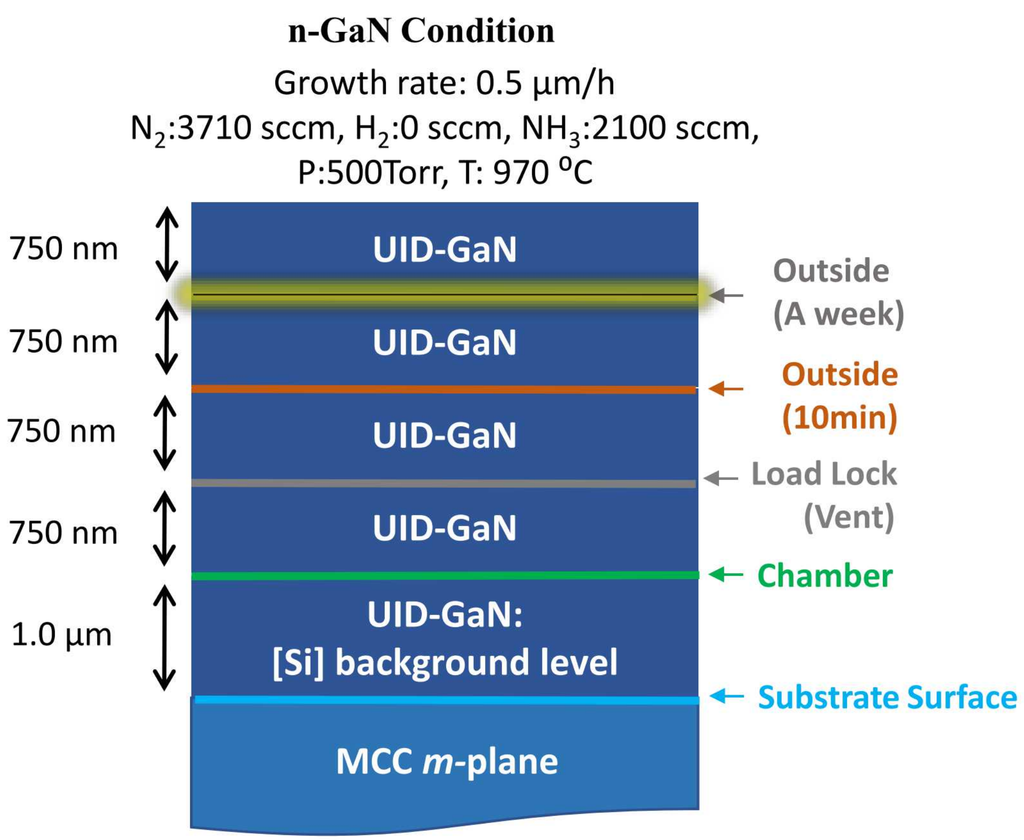

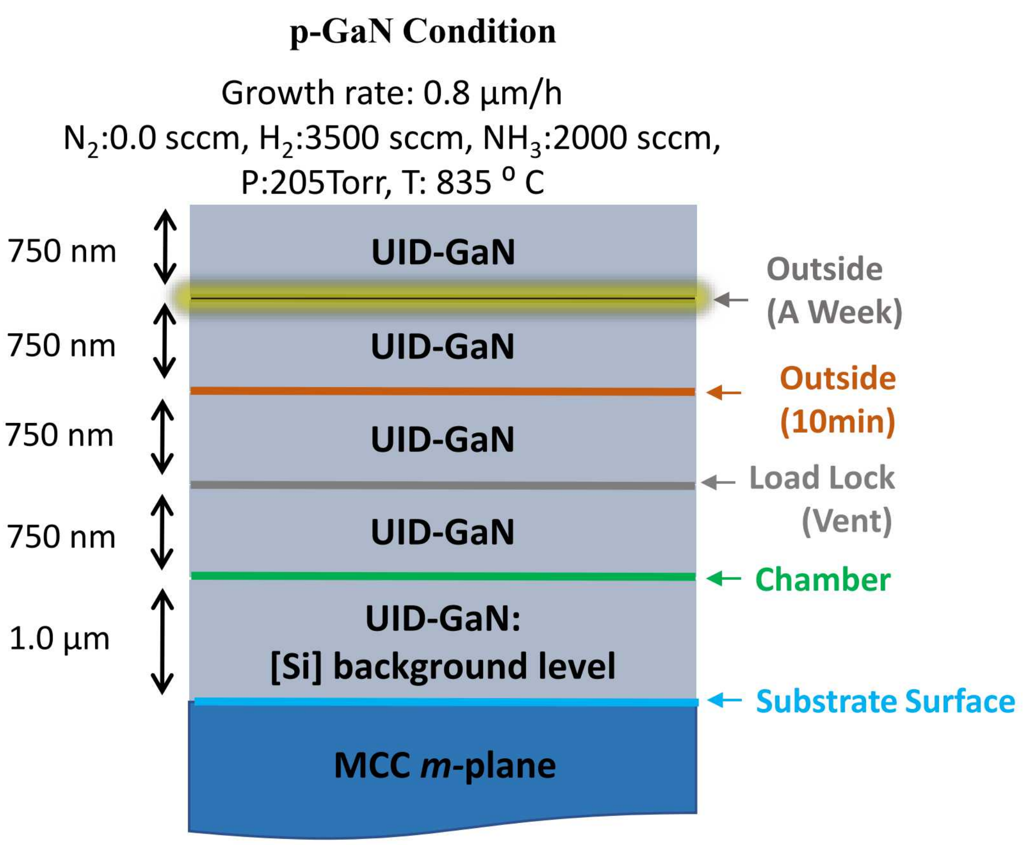

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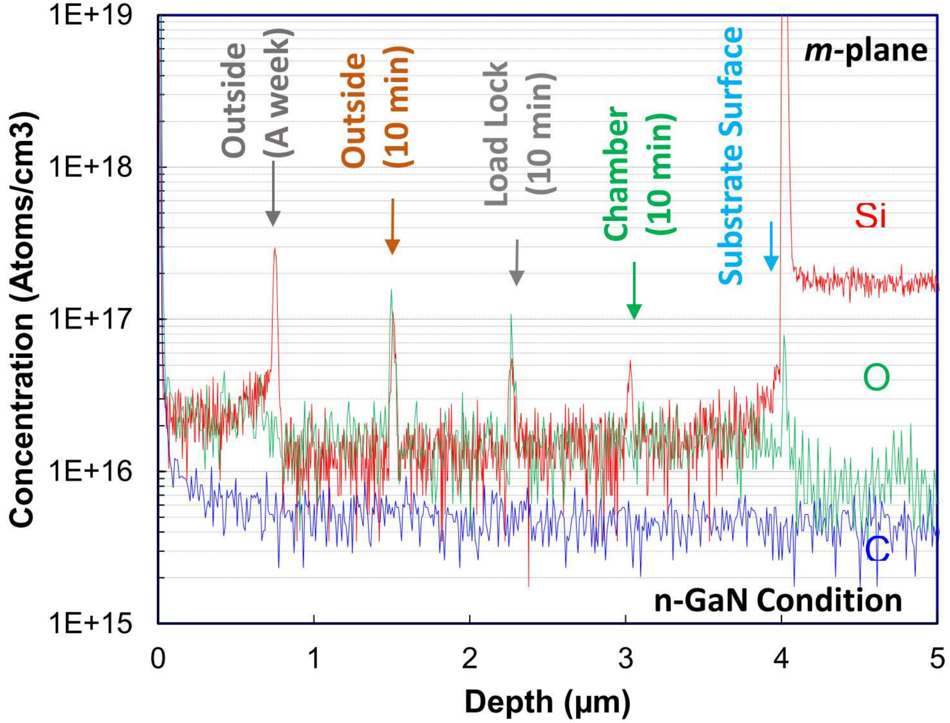

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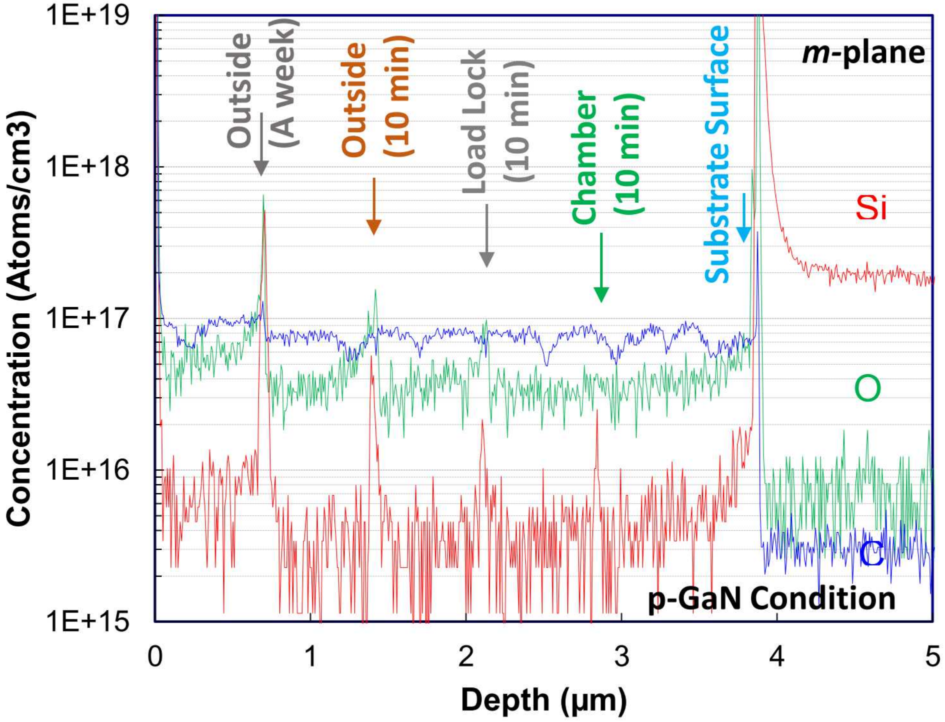
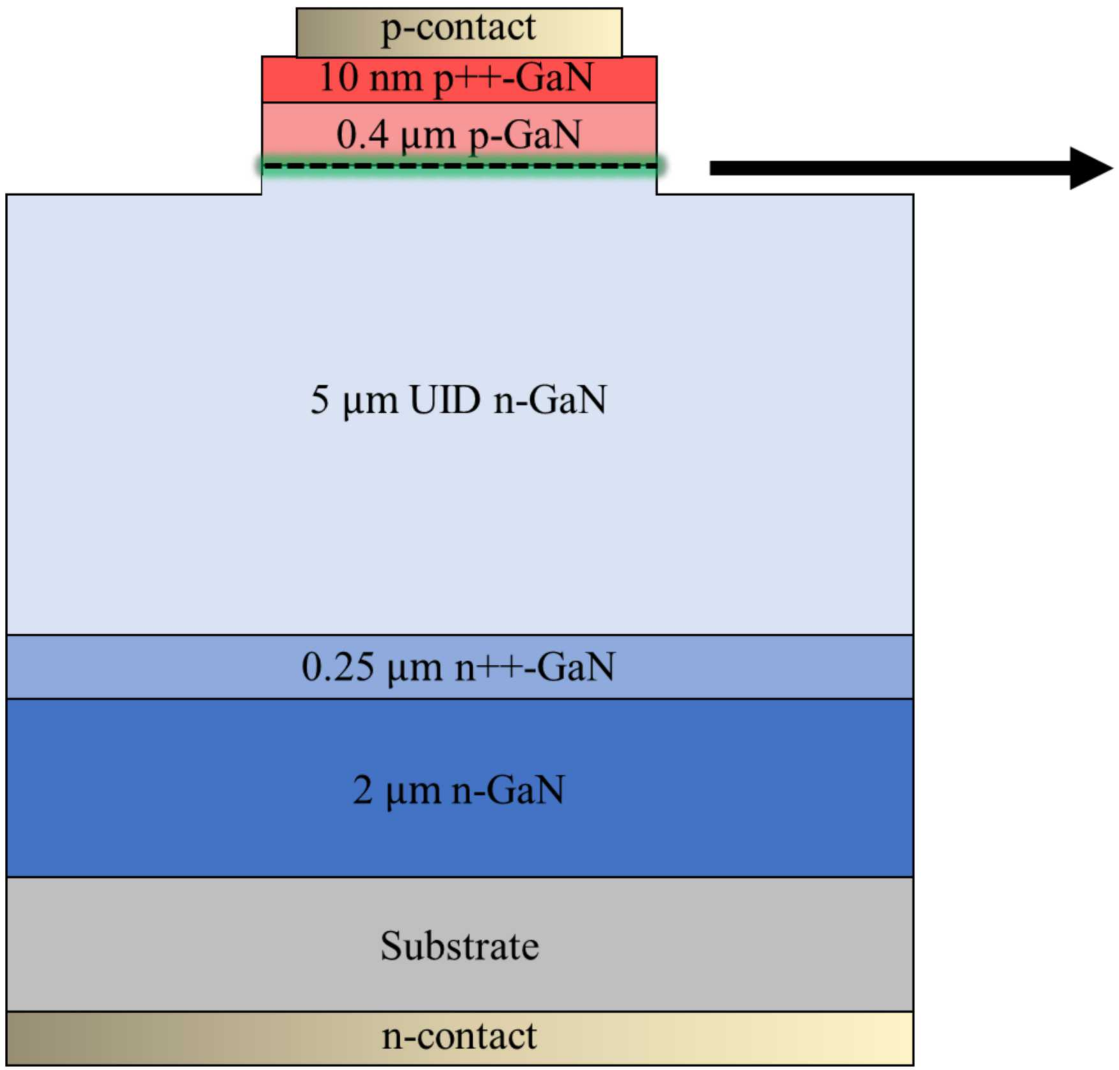


- ❑ Secondary ion mass spectrometry (SIMS) profile analyses were performed by EAG Laboratories.
- ❑ The largest impurity spikes were due to the outside interruptions followed by the load lock interruption then by the in-chamber interruption.
- ❑ The impurity levels appear to be relatively benign. How do they affect performance?

Experiment 2 - Effect of interfacial impurities on p-n diodes

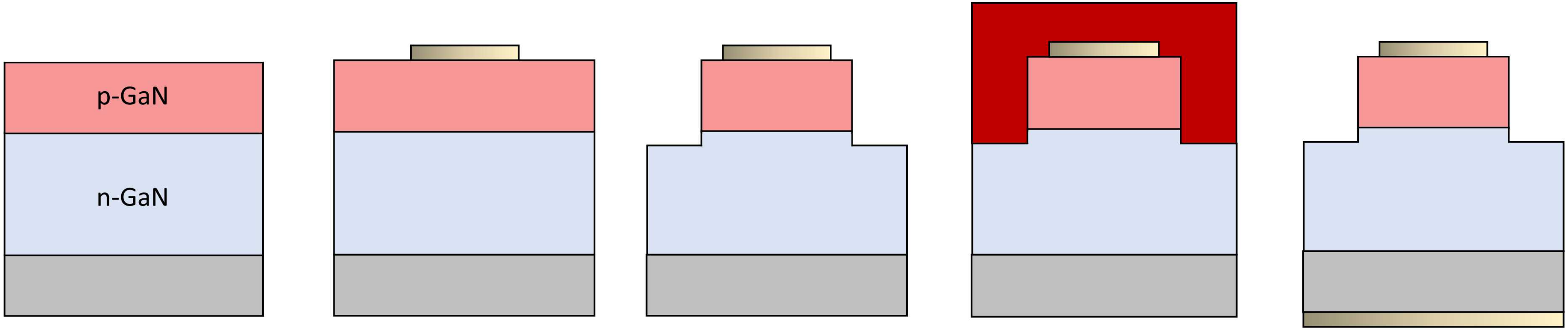


i. **Continuously grown p-n junction**

ii. **p-GaN grown after in-chamber interruption lasting 10 minutes**

iii. **p-GaN regrown after sample sitting outside chamber for one week**

Experiment 2 - Effect of interfacial impurities on p-n diodes



1) Epitaxial Growth

- Grown using MOCVD
- p-GaN layer activated

2) p-Contact Deposition

- Pd/Au (30nm/300nm)
- E-beam evaporation

3) Mesa Etch

- Inductively coupled plasma etching
- Ar/Cl
- RF Power = 20 W
- ICP Power =150 W

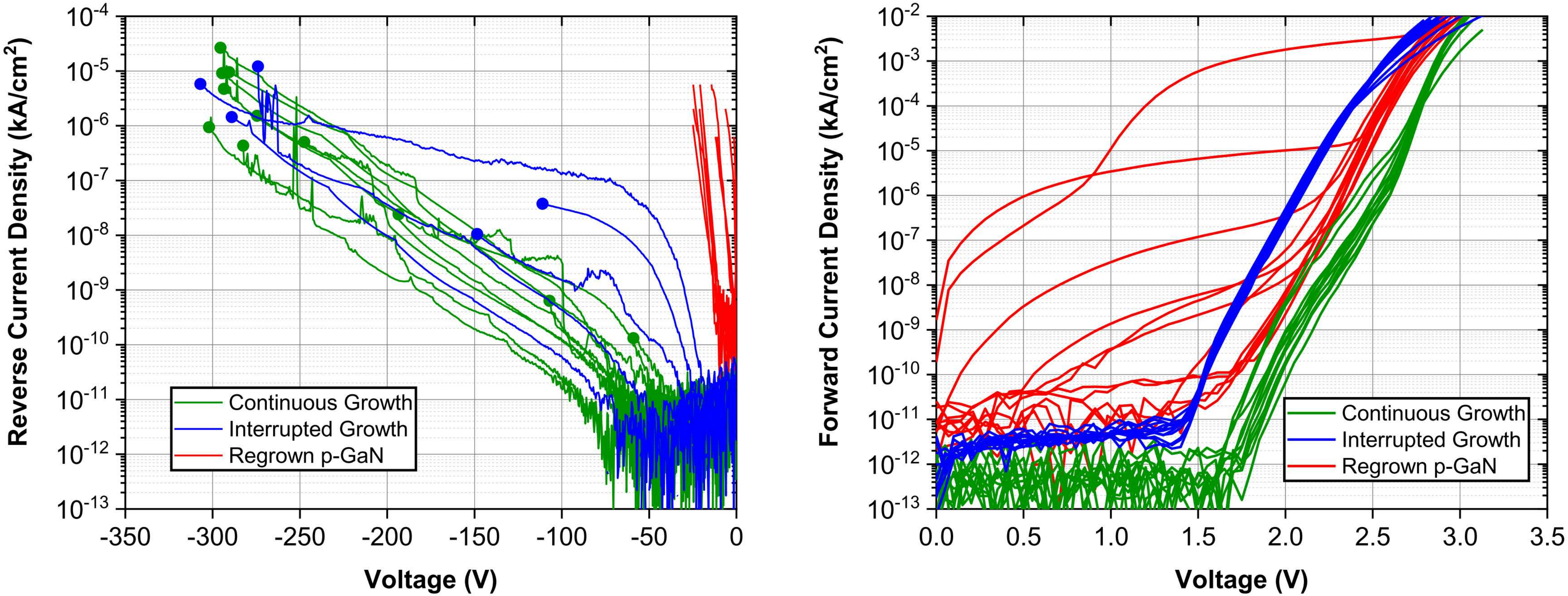
4) Protective Photoresist

- Protects topside during backside contact deposition

5) n-Contact Deposition

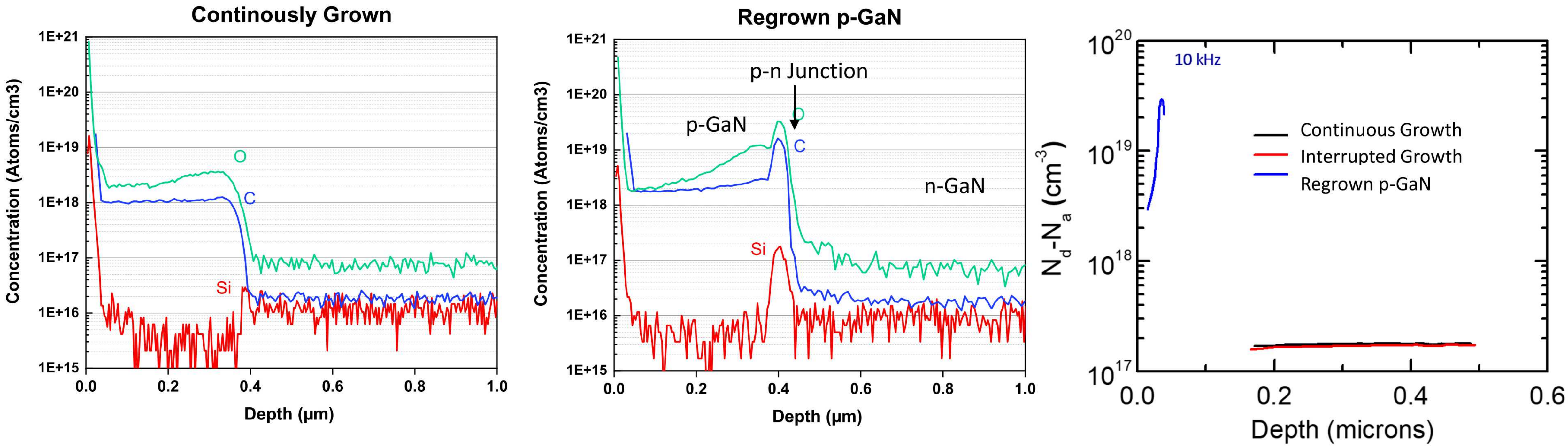
- Ti/Al/Ni/Au (20/100/50/300nm)
- E-beam evaporation
- Photoresist then removed

Experiment 2 – Effect of interfacial impurities on p-n diodes



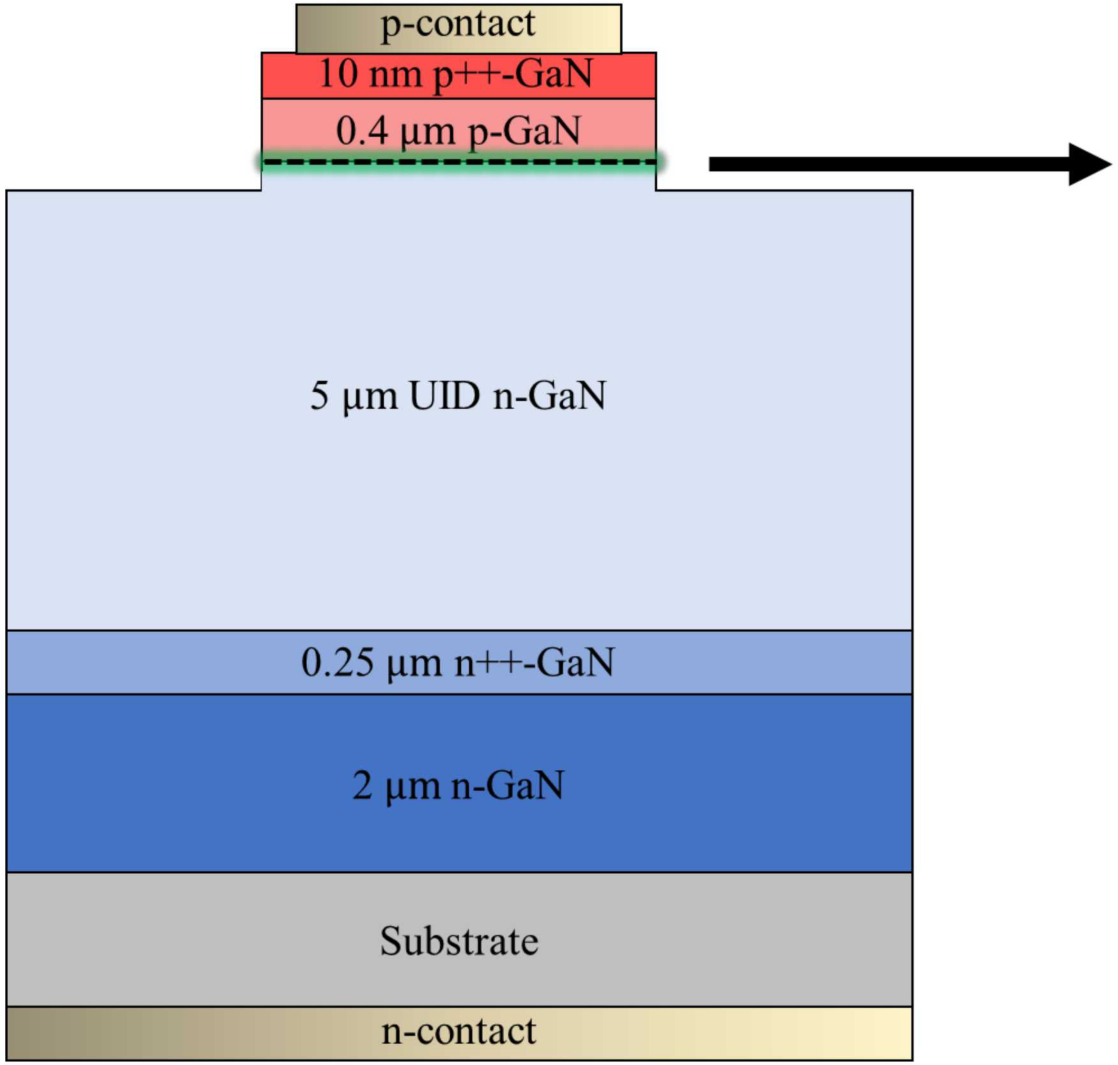
- ❑ The p-n diodes featuring continuous growth and interrupted growths performed relatively similarly.
- ❑ The p-n diodes featuring a regrown p-GaN layer experienced high leakage currents both in reverse bias and forward bias before turn on.
- ❑ Continuous p-n diodes are the first on m-plane to achieve 300 V.

Experiment 2 – Effect of interfacial impurities on p-n diodes



- SIMS profile analysis showed the presence of large impurity spike at the p-n junction of the sample with a regrown p-GaN layer.
- C-V measurements revealed a net carrier spike in the sample featuring a regrown p-GaN layer. This suggests the oxygen acting as dopants have created the spike. We believe the C-V measurements are artificially high due to stray capacitances and are representative of trends rather than absolute carrier concentrations.
- The main difference between the SIMS profiles is the presence of the impurity spikes in the regrown sample. It could be possible that the large impurity spikes have a role in the I-V characteristics of the regrown sample.

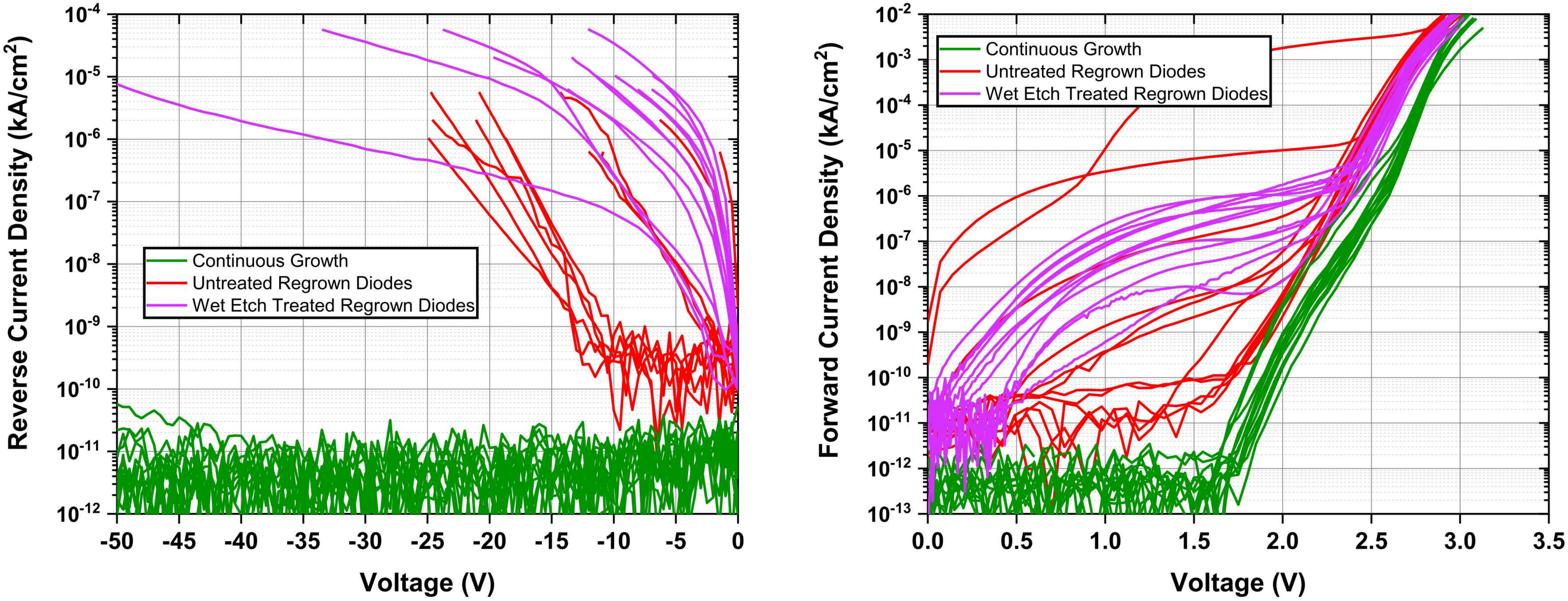
Experiment 3 – Effect of wet etch treatment on interfacial impurities and p-n diodes



i. **Sample regrown after 1 week in nitrogen box without treatment**

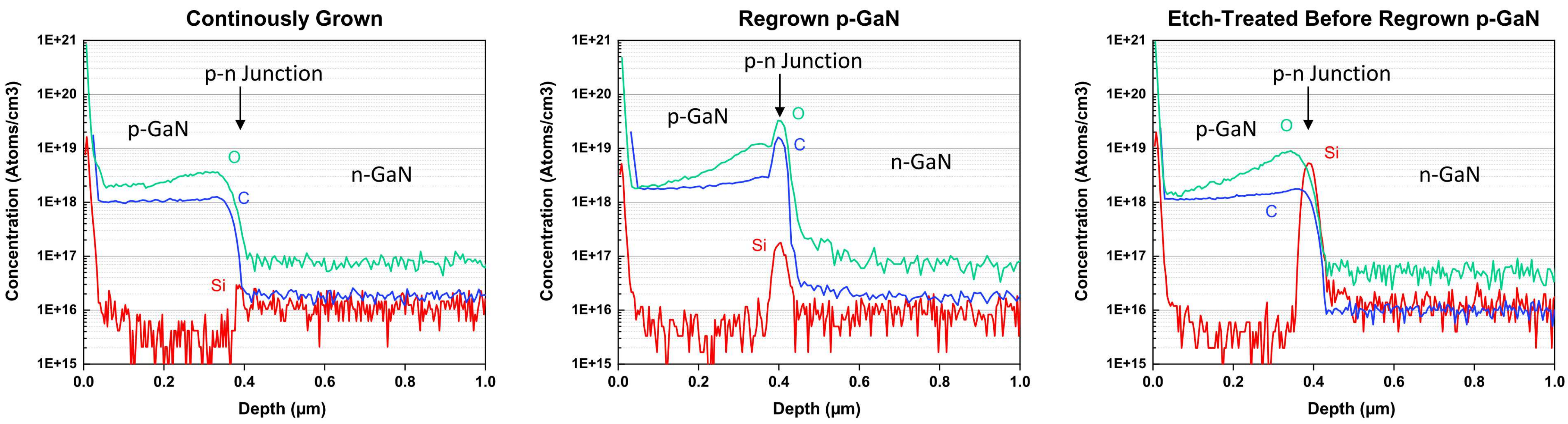
ii. **Sample regrown after 1 week in nitrogen box and treatment with 1 min acid dip into buffered oxide etchant**

Experiment 3 – Effect of wet etch treatment on interfacial impurities and p-n diodes



- The wet etch treated diodes performed slightly worse than the untreated diodes.
- The wet etch treated diodes all showed high leakage currents before turn-on in forward bias. However, some untreated diodes show much less leakage current before turn-on
- The wet etch treated diodes generally demonstrated higher leakage current in reverse bias than the untreated diodes.

Experiment 3 – Effect of wet etch treatment on interfacial impurities and p-n diodes



- The SIMS profile analysis between p-n diodes that were continuously grown, possessed an untreated regrown p-region, and possessed a wet etch treated regrown p-region as shown.

- The analysis comparing the three suggests that the wet etch treatment removed the oxygen and carbon impurity spikes

Conclusion

- In the first experiment, we observed that inducing growth interruptions in which the sample was removed from the chamber and kept in a nitrogen box for a week produced impurity spikes of concentrations ($2.71 \times 10^{17}\text{cm}^{-3} - 5.19 \times 10^{17}\text{ cm}^{-3}$) that were 5 to 20 times the concentration ($2.5 \times 10^{16}\text{ cm}^{-3} - 5.38 \times 10^{16}\text{ cm}^{-3}$) of an in-chamber growth interruption lasting 10 minutes depending on growth conditions.

- In the second experiment, the impurity levels of continuously grown, interrupted, and regrown p-n junctions of diodes were linked to current-voltage characteristics demonstrating that impurities associated with interrupted growths did not severely impact performance while the $\geq 1 \times 10^{19}\text{ cm}^{-3}$ oxygen and carbon impurity levels associated with regrowth caused p-n diodes to experience elevated leakage currents.

- The third experiment showed that buffered oxide etch treating a sample before a regrown p-GaN layer had removed much of the carbon and oxygen impurities while adding silicon impurities and was unsuccessful in preventing high leakage currents.

- While a correlation between carbon, oxygen, and silicon impurities and diode performance cannot be uniquely established, we infer that such impurities might play a role in the higher leakage current of p-n diodes featuring regrown layers.

- Growth and processing techniques for mitigating the negative effects of impurities in regrown junctions will need to be further developed to realize GaN power devices with embedded p-n junctions.

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