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Sandia National Laboratories

Fabrication of SiGe Quantum Dot Nanostructures and Device Construction Zones

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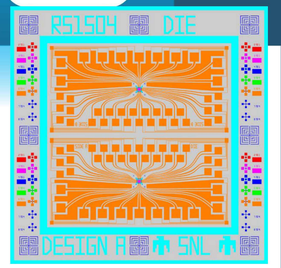


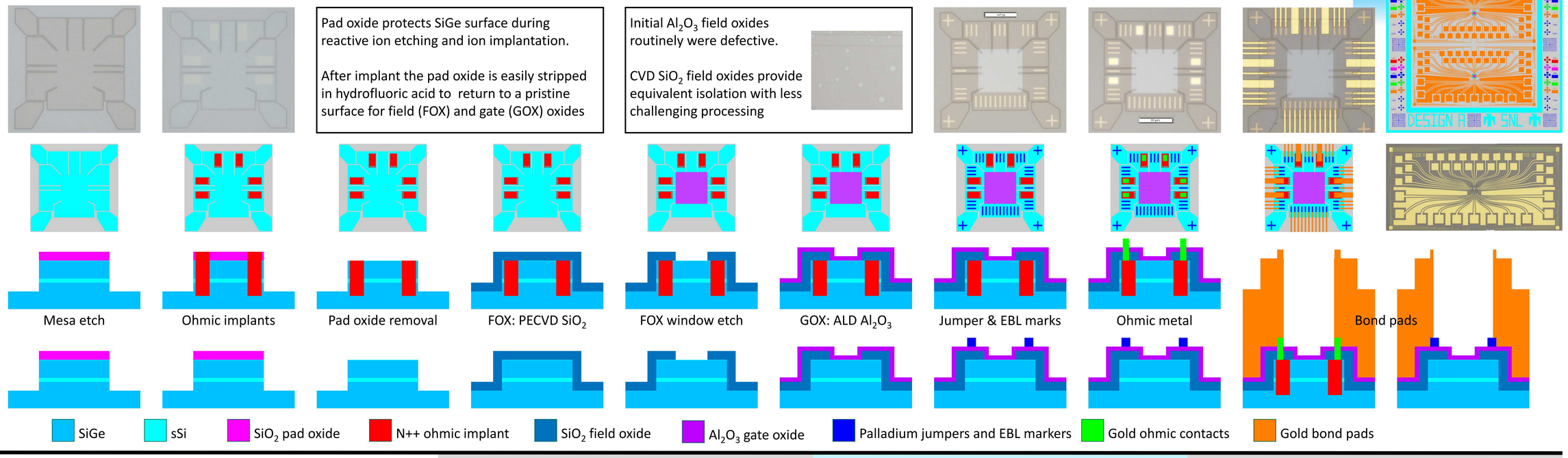
Wafer level fabrication
of qubit construction zones
- High yield
- High throughput
- All photolithography process
- 52 die per 3” wafer

Pad oxide protects SiGe surface during reactive ion etching and ion implantation.

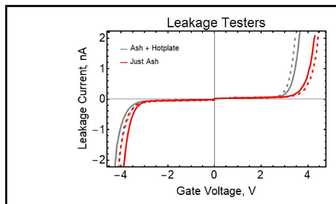
After implant the pad oxide is easily stripped in hydrofluoric acid to return to a pristine surface for field (FOX) and gate (GOX) oxides

Initial Al_2O_3 field oxides routinely were defective.

CVD SiO_2 field oxides provide equivalent isolation with less challenging processing



Die level nanostructure fabrication
of qubits with electron beam lithography
- Design adapted from on D. M. Zajac, *et. al.* Phys. Rev. Applied **6**, 054013 (2016).
- Aluminum gates isolated by native oxide enhanced through downstream ozone plasma clean
- Die level fabrication enables efficient *fabrication → measurement → fabrication* feedback loop



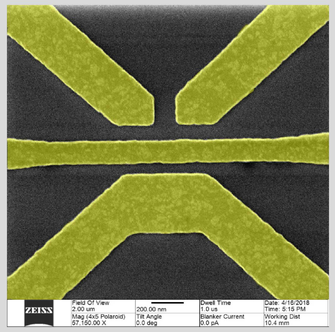
Leakage measurements show 3V of gate range between overlapping gates. A plasma ashing between evaporation provides enhancement of the native oxide.

MESA complex:
Class 1 Si cleanroom (CMOS)
Class 10 Mixed materials (III-V R&D)
Capabilities:
Up to 6” wafer processing, novel integration, small volume production.

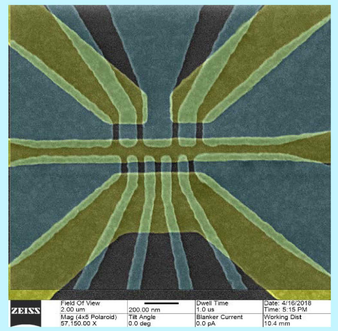
CINT complex:
Class 100 cleanroom
Capabilities:
Up to 4” wafer processing, user facility for visiting collaborators.

Special thanks to Evan MacQuarrie (UW-Madison) for oxide leakage measurements

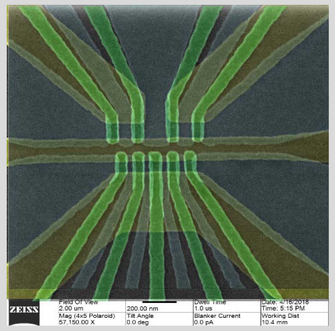
Level 1: Isolation
Define channels charge sensor and QD transport

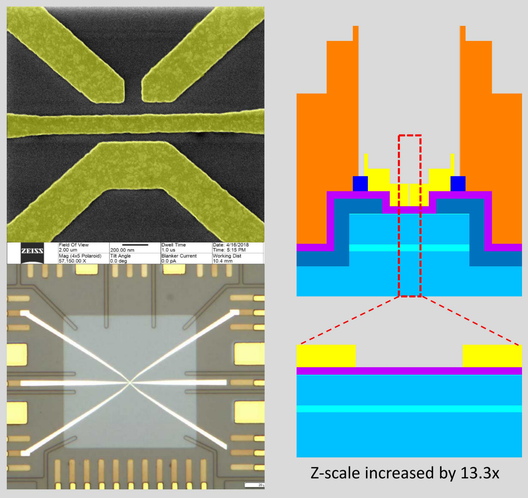


Level 2: Accumulation
Reservoirs and QD occupation control gates

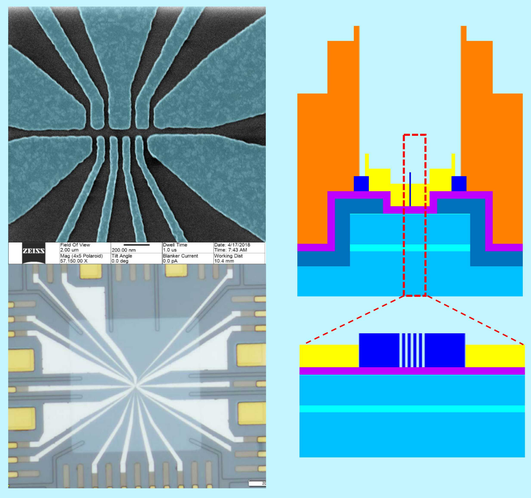


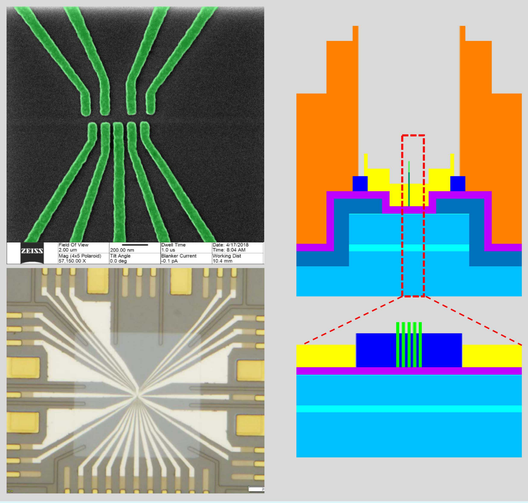
Level 3: Tunnel Barrier Control
Tuning for reservoir-QD and QD-QD tunnel rates





Z-scale increased by 13.3x





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