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Optimal Design of MHz LLC Converter for 48V Bus Converter Application

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***Abstract*— Intermediate bus architecture employing 48V bus converters is widely used in power supply applications. With the rapid increase of demanded power by these loads, higher efficiency and power density are driving better performance power management solutions. In this paper, a Gallium Nitride (GaN) based design of a two-stage solution is proposed. The first stage is a multi-phase Buck for regulation. The second stage is an LLC converter with fixed switching frequency for isolation. The detailed design and optimization of the LLC converter are studied. To achieve high power density and high efficiency, the transformer design becomes critical at MHz frequency. The matrix transformer concept is applied and a merged winding structure is used for flux cancellation, which effectively reduces the AC winding losses. A novel primary termination and via structure is proposed, resulting in great loss reduction. In addition, to study the current sharing of parallel winding layers, a 1-Dimensional analytic model is proposed, and a symmetrical winding layer scheme is used to balance the current distribution. Finally, the prototype for the two-stage bus converter is developed, with the peak efficiency of 96% and power density of 615W/in^3.**

***Index Terms*— bus converter, integrated magnetic**

I. Introduction

With the fast development of digital systems, their power management has become a big challenge. To achieve higher power delivery efficiency and to reduce the power module size, the 48V intermediate bus architecture (IBA) power supply is widely used in telecom, data centers, and aerospace applications [1], [2]. Fig. 1 shows one example of IBA used in a network switch. In the IBA solution, only one, or a small number of isolated DC-DC bus converters, are employed for the isolation requirement to supply an intermediate bus voltage, which is typically 12V. The intermediate bus is followed by a number of non-isolated point-of-load (niPOL) converters for the final regulation to various electronic loads [3], [4]. Currently, the IBA approach is widely adopted in all kinds of distributed power systems [4], [5]. The isolated bus converter plays a very important role in IBA implementation. A high-power, highly-efficient, small solution for the intermediate bus converter (IBC) is desired. In different applications, isolation is required at IBC level for different reasons. Generally speaking, there are safety requirements in

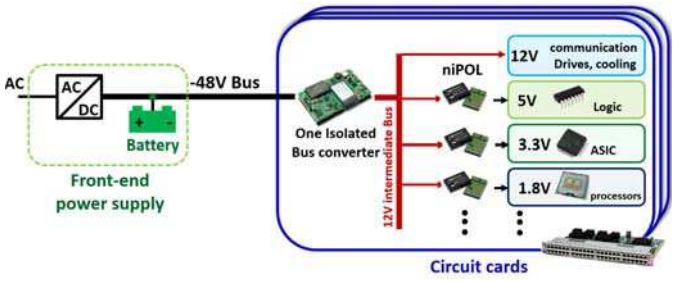

Fig. 1. Intermediate Bus Architecture in a network switch.

information technology equipment and medical equipment. And the output of an isolated converter can be configured to be either positive or negative. Moreover, isolation eliminates or reduces noises of the system bus from appearing on the output. It also eliminates ground loop noise. The isolated bus converter can be regulated or unregulated, depending on the requirements of the system [6]. For systems with a well-regulated 48V bus, such as enterprise equipment specified with Server System Infrastructure initiative [4], an unregulated DC transformer (DCX) can be used for the IBC. For other applications, such as telecom equipment that has a wide input voltage range (35V to 72V), regulation is necessary for the IBC [7]. This paper will focus on the design of regulated IBC.

The state-of-the-art IBCs fall into two categories: the single-stage solution [8]–[10] and two-stage solution [11]. In [8], a phase-shift-full-bridge converter (PSFB) is used as a single stage. The first problem with this solution is that PSFB is not a complete soft-switching topology. The high switching loss limits the switching frequency to 150kHz, which leads to bulky magnetics. To handle the large amount of output current, four synchronous rectifiers (SRs) are connected in parallel. The current sharing between these SRs is critical. Also, the transformer suffers from high termination loss and conduction loss on the secondary side. To improve this solution, an LLC converter can be used instead of the PSFB, which can achieve zero to full load ZVS, and ZCS for the SRs. It also has very low turn-off current for primary side devices [12], [13]. With these benefits, the switching frequency can be pushed higher to reduce the magnetic size. However, due to the nature of the resonant converter, LLC converter needs variable frequency control. This is acceptable in some applications, but in other applications where there is a stringent Electromagnetic Interference (EMI) specification, the fixed-frequency solution is preferred. With the two-stage architecture, it is easier to design a fixed-frequency IBC with high efficiency and power

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density. The basic idea is to design one regulation stage and one isolation stage. The regulation stage is implemented with fixed-frequency control. The isolation stage is an unregulated fixed ratio converter, which can be highly efficient.

In this paper, a two-stage fully regulated bus converter is proposed. The first regulation stage is a multi-phase Buck converter. The bus voltage will be regulated at 36V. The second isolation stage is a fixed-frequency LLC DC transformer (DCX) with integrated matrix transformer. The two-stage solution operates at 1MHz fixed switching frequency, which provides predictable EMI performance. The first-stage Buck is still a hard switching topology and hence the switching frequency is not high (500kHz per phase). But the second stage is free from regulation requirement and the soft-switched and highly efficient LLC-DCX is used. Compared with the best state of the art in [8], the switching frequency can be pushed to 1MHz to reduce the transformer size, which is the first advantage. To handle the high output current, three elemental transformers are connected in parallel on the secondary side. The first benefit is the reduction of secondary conduction and termination loss due to the three parallel outputs sharing current. The second benefit is that because of the series connection of the primary side, the current in the parallel SRs in each output is naturally distributed evenly. This is the second advantage. In this paper, the focus is on the design of the second stage LLC-DCX. Due to its full soft-switching property, it is implemented with Gallium Nitride (GaN) devices to achieve MHz high-frequency operation; thus, shrinking the passive size and increasing the power density. In terms of the LLC design, a great amount of work has been done to improve the high-frequency PCB-winding transformer.

In [6], the matrix transformer concept is applied [14]. The matrix transformer can significantly reduce leakage inductance, winding resistance, and termination loss by splitting the secondary side current. Also, due to the primary series, secondary parallel connection, it naturally achieves good current sharing for the SRs, which used to be a major limitation for the secondary SR implementation. However, by using multiple transformers, it suffers from large core volume and core loss. In [5], the flux cancellation method was proposed to integrate two transformers into one core. Later, the secondary termination loss is re-examined in [15]. The goal is to minimize the secondary termination loop to minimize the leakage flux and related AC losses. The secondary windings are placed on the top and bottom layer and directly integrate the SRs and output caps into the windings. As a result, the winding and termination loss are greatly reduced. In [16], an optimization procedure for the transformer was proposed which utilizes the 3D FEA simulation as the correction factor. There works are followed in [17], which further integrates two cores into one core with four legs, which is more robust against variations and tolerance and better for manufacture. In [18], the optimization procedure is further improved by introducing another non-uniform parameter in windings, which results in higher power density and light load efficiency.

However, none of the works mentioned above carefully studied the primary termination design and current sharing issues of parallel windings in multiple layers. In their applications, these issues should not be a problem. The output current can be high, but the primary side current is small (usually smaller than 15A RMS). However, in the 1kW bus converter design, with 36V bus voltage, the primary current is much higher, which can cause great AC termination and via loss at 1MHz frequency. Moreover, to handle the large current, more parallel windings are used. The current sharing between these windings becomes another new challenge that must be solved. All of the above issues are discussed and addressed in this paper.

The paper is organized as follows: Section II discusses the LLC design and transformer structure. A novel merged winding structure is proposed to achieve better interleaving and reduce AC losses. Section III proposes an interleaved termination and via structure achieving great loss reduction and better via utilization. Section IV discusses the current sharing issue of parallel windings in multiple layers. The analytic model is built and verified by 3D FEA simulation. A new symmetrical winding layer arrangement is proposed to address the current sharing issue. Section V demonstrates the transformer optimization process and experimental result. Section VI concludes the proposed design.

II. Matrix Transformer and Merged Winding Design of LLC-DCX

The circuit diagram of the LLC-DCX with the matrix transformer and PCB windings is presented in Fig. 2. For each elemental transformer output, four windings are paralleled on secondary sides to handle the large output current and the same number of parallel windings are used on the primary side to achieve good interleaving. The three elemental transformers are integrated into the one-core structure. The 3D view of cores is shown in Fig. 2. The integration helps achieve symmetrical air-gaps across the three transformers and is also better for manufacture. The front view of the transformer is shown in Fig. 3. The paralleled SRs and output capacitors are placed on both the top and bottom layers and integrated with the PCB windings to minimize the termination loops and hence reduce the loss [19]. The middle 12 layers are for windings. They are separated into four identical groups. Each group has secondary layer #1, primary layer, and secondary layer #2. The top view of one group of windings is shown in Fig. 4(a). In this manner, all of the primary and secondary windings are interleaved. As mentioned earlier, the primary current is large; thus, we minimize the primary current path by a novel simple primary winding structure so that the primary winding loss can be reduced. The yellow arrows on the winding indicate the current flow in the positive half cycle. Note that the impact of parasitic capacitance of the primary and secondary windings is usually small in low voltage applications.

Nevertheless, there is a price one pays for this special primary winding structure. Now, the primary winding is not in a similar shape as the secondary winding, there are some non-interleaved areas, as spotted in the shading areas in both top view and cross-section view in Fig. 4. Here we use the first elemental transformer as an example, the other two transformers have similar problems. In the shading areas, the

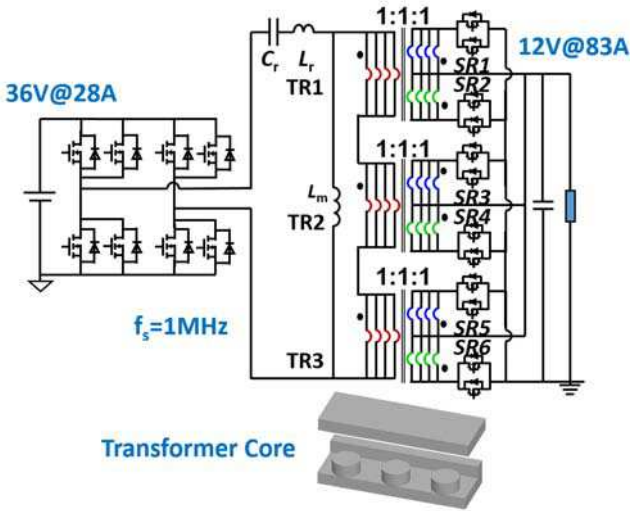


Fig. 2. Circuit diagram of proposed LLC-DCX and integrated transformer core.

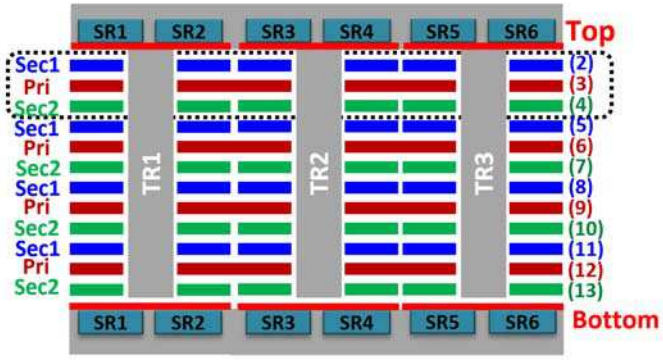
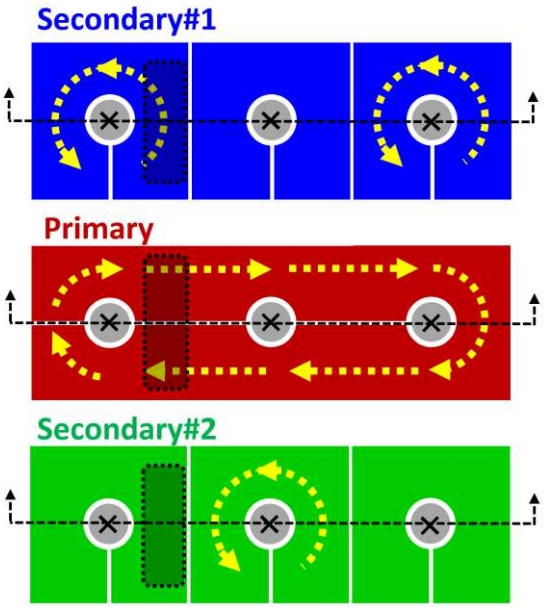


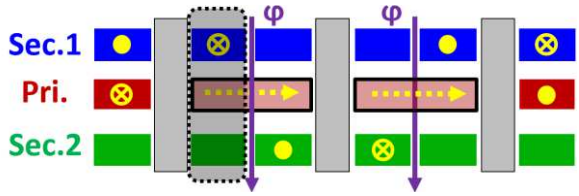
Fig. 3. Front view of the proposed PCB-winding transformer.

current which are supposed to flow in opposite direction in the conventional interleaved design, now flow in the perpendicular direction. Based on Faraday's law and Lentz's law, the AC current always tries to attract or induce AC current on nearby conductors oppositely to cancel the flux. So both current try to affect each other. As a result, eddy current appears on both secondary 1 and primary windings and the current crowding zones are observed in the simulation results in Fig. 5. This uneven current distribution creates very high conduction loss. Another effect of the non-interleaving of secondary 1 and primary is that the flux cannot be canceled, as shown by the purple arrows in Fig. 4(b). The leakage flux from these two windings will create eddy current on the nearby winding, which is the non-conductive winding secondary 2. Even though it is not supposed to conduct current in the positive half cycle, current is observed in the secondary 2 shading area in Fig. 5. This is the eddy current created by the leakage flux.

To solve this problem, two windings of secondary winding #1 are merged into one, and the same is done for secondary #2, as shown in Fig. 6. The merged parts are both connected to the output terminal Vo; therefore, it will not affect the circuit



(a) Top view of the original winding structure.



(b) Cross section view of the original winding structure.

Fig. 4. One winding group of the original winding structure.

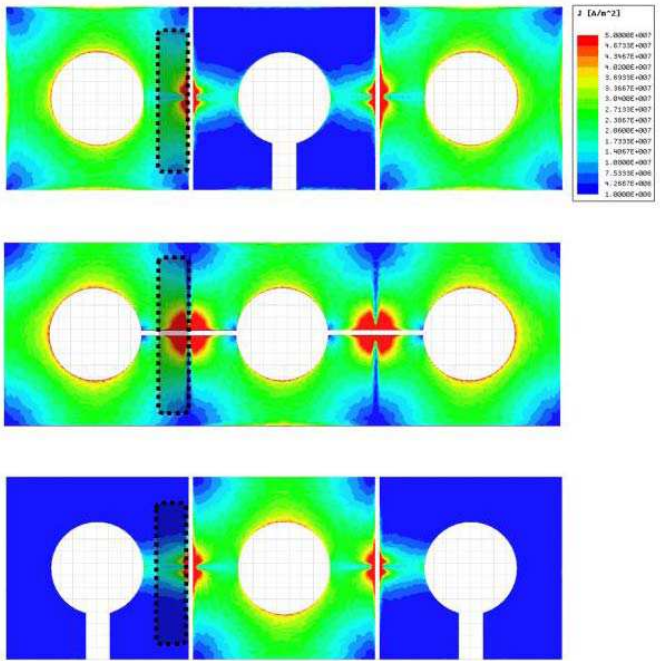
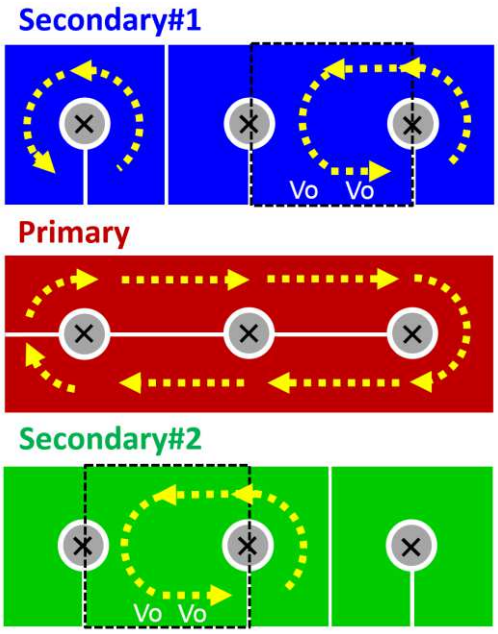
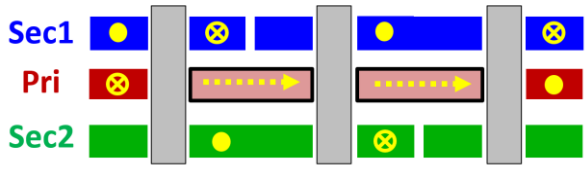


Fig. 5. Winding current distribution of the original structure.

operation. Now, in the junctional area, instead of interleaving the primary and secondary, two secondary currents flowing in opposite directions are "interleaved", and the leakage flux



(a) Top view of the proposed merged-winding structure.



(b) Cross section view of the proposed merged winding structure.

Fig. 6. Proposed merged-winding structure.

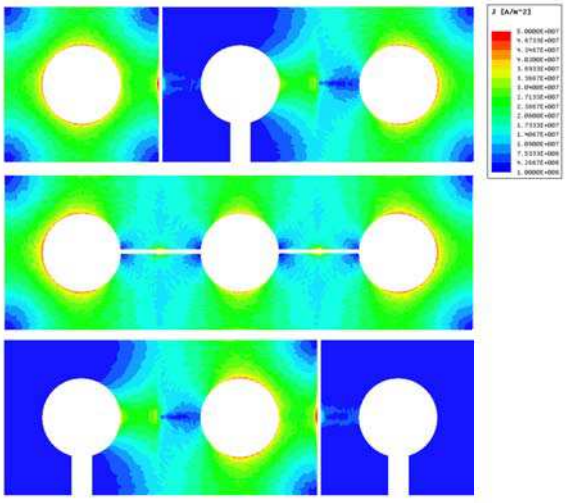
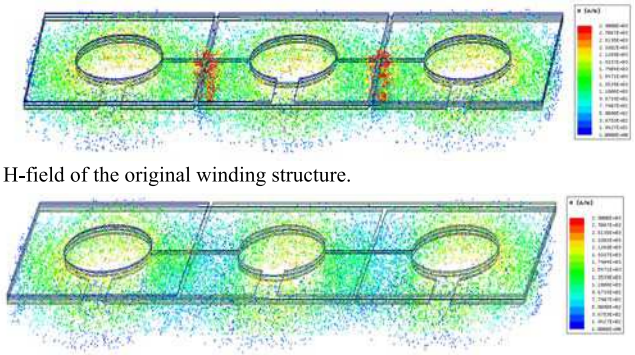


Fig. 7. Winding current distribution of the proposed structure.

are cancelled, as shown in Fig. 6. The simulation results of the improved structure are presented in Fig. 7. The H field comparison of the two structures is shown in Fig. 8. The current crowding is greatly reduced. 40% loss reduction and 40% leakage inductance reduction are achieved by this improvement.

As a summary, in applications of matrix transformer with high turns ratio and multiple primary windings, conventional interleaved winding design still applies. In other applications where 1:1 turns ratio and one-turn primary windings are used, the proposed simple primary winding structure with merged winding design can be performed to minimize the winding loss.



(a) H-field of the original winding structure.

(b) H-field of the proposed merged-winding structure.

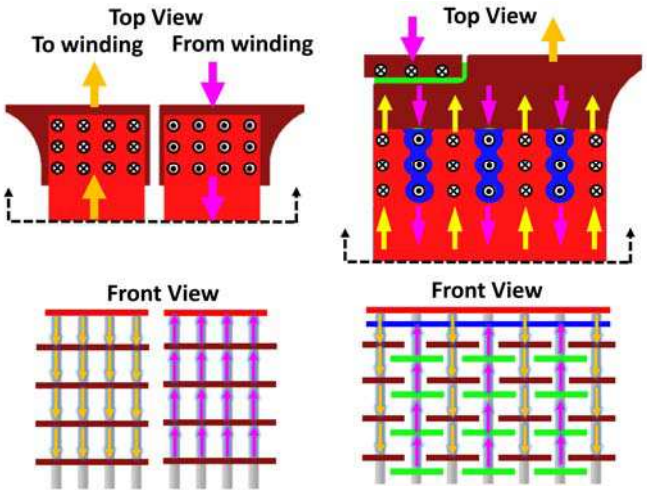
Fig. 8. H-field comparison of the original and proposed winding structure.

III. Termination and Via Design of Transformer Primary Windings

Termination and via design of transformers are critical in high current applications. In [5], [15], [19], efforts are made to minimize the secondary termination loop. As a result, the secondary termination loss is reduced. A similar SR integration technique has been applied in this work to minimize the secondary termination loss. However, for applications where the output power can be as high as 1kW, the LLC-DCX primary RMS current can also be high. In this application, because the bus voltage is 36V, the primary RMS current is above 30A. Such high current must go through termination and vias to enter the primary windings in each layer. This creates a significant amount of losses, which is a new challenge for the transformer design.

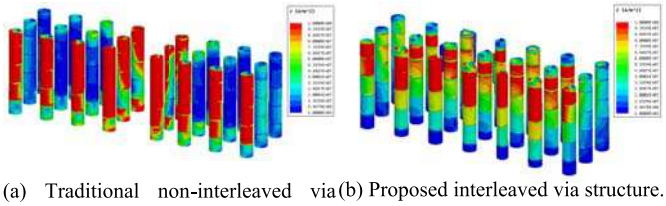
To address this problem, the interleaving concept is applied. First, the traditional non-interleaved via design and the current density of FEA simulation are shown in Fig. 9(a) and Fig. 10(a). In the traditional design, current flowing up (indicated by orange arrows) is on one side and current flowing down (indicated by pink arrows) is on the other side. This structure suffers from large leakage flux, eddy current, and proximity effect. As a result, the current is crowded to only half of the total vias. Also, the current within one via is not distributed evenly. This results in poor via utilization and high via loss. In the proposed interleaved structure shown in Fig. 9(b), the vias are interleaved in the vertical direction. By placing vias in the finger-shape manner, the currents flowing up and down are split and interleaved. The same number of vias are used for both designs as a fair comparison. The results are shown in Fig. 10(b). The vias are now well utilized.

Second, the traditional non-interleaved termination design and current density results are shown in Fig. 11(a) and Fig. 12(a). A large current crowding hot spot is observed. In the proposed structure, the terminations are also interleaved. The



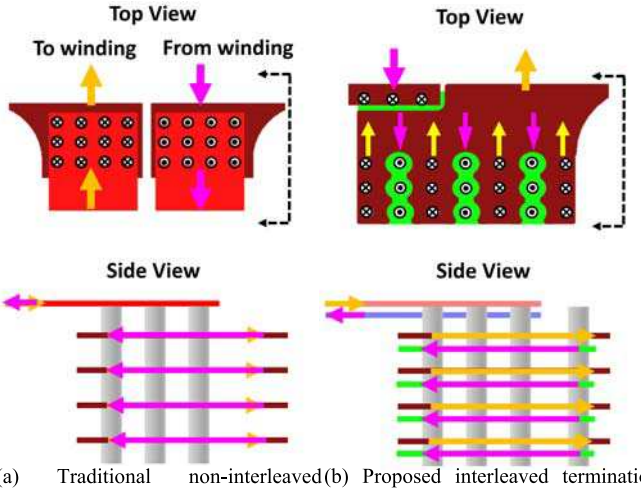
(a) Traditional non-interleaved via structure. (b) Proposed interleaved via structure.

Fig. 9. Top view and front view comparison of non-interleaved and interleaved via structure.



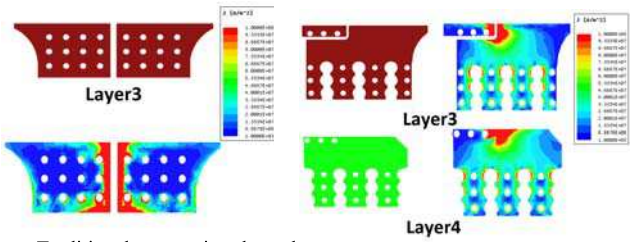
(a) Traditional non-interleaved via structure. (b) Proposed interleaved via structure.

Fig. 10. Current distribution comparison of non-interleaved and interleaved via structure.



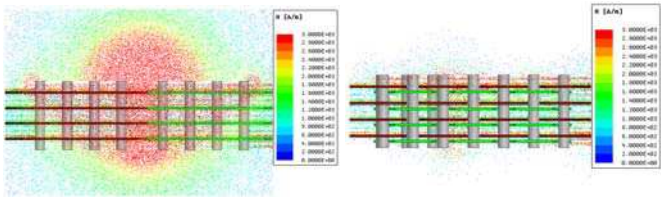
(a) Traditional non-interleaved termination structure. (b) Proposed interleaved termination structure.

Fig. 11. Top view and side view comparison of non-interleaved and interleaved termination structure.



(a) Traditional non-interleaved termination structure. (b) Proposed interleaved termination structure.

Fig. 12. Current distribution comparison of non-interleaved and interleaved termination structure.



(a) Traditional non-interleaved termination and via structure. (b) Proposed interleaved termination and via structure.

Fig. 13. H-field comparison of non-interleaved and interleaved termination and via structure.

proposed structure is compared with the conventional structure in Fig. 11(b). The current flows in (indicated by orange arrows) through one group of layers into windings, and it flows out (indicated by pink arrows) through the other group of layers which are right on the bottom of the first group of layers. As a result, the terminations are interleaved in a similar manner as of transformer windings. In the proposed structure, the crowding is greatly reduced, as shown in Fig. 12(b). A great reduction of leakage flux can be observed for the improved design, as shown in Fig. 13. As a summary, the proposed design achieves interleaving for both vias and terminations in both vertical and lateral directions, which minimizes the leakage flux and AC losses. Before the improvement, the primary termination and via loss was almost as large as the primary or secondary winding loss. After the improvement, this loss is reduced by 50%.

With the interleaved structure, the via arrangement is optimized based on the tradeoff from via size, number and distance. Generally speaking, for the given termination footprint, if a larger via size is used, the total via number is reduced, so the total via loss could increase or reduce. At the same time, since the via is basically a hole on the termination, the termination area is cut by the via and the termination resistance is also affected. Via distance is a very important factor for the termination conduction loss. The tradeoff here is between AC and DC loss. If the distance is too small, the termination is cut too much and the DC conduction loss becomes very high. If the distance is too long, the termination is too large and skin and proximity effect induces high AC loss. With the help of simulation, we can propose a basic procedure to optimize the via design. First, in the given terminal footprint, for each given via size, the via distance can be optimized by sweeping the distance with simulation results. Each via size has its best design and loss result. After that, the results of different via size are compared to obtain optimal via design.

In conclusion, the termination and via design concept can be widely applied. They are not restricted to the primary or secondary side respectively. In effect, when the circuit and connections outside the transformer windings are simple, for

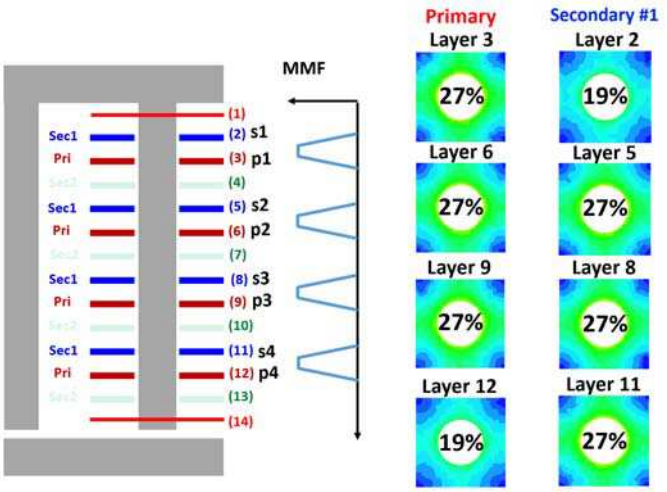


Fig. 14. Original layer scheme of the paralleled PCB windings and the current distribution in positive half cycle.

example, the center-tapped rectifier structure, the integrated termination design can be applied [15], [19]. When the circuit and connections outside the transformer windings are complex, where integrated design is no longer possible, the proposed termination and via interleaving concept can be applied. As a result, a complete solution is provided for the transformer winding termination design. It could be applied based on different external circuits.

IV. Current Sharing of Parallel Winding Layers

A. Analytic Model for Parallel-Winding Transformer

Another major challenge comes from the current sharing of the paralleled winding layers. As discussed earlier, each primary or secondary winding has four paralleled layers. To fully utilize these layers and prevent any hot spot, good current sharing is critical. In the parallel winding design, the layer scheme is found to have a significant impact on current sharing and losses. In the original design presented in Fig.14 left, with a fully interleaved layer arrangement, the current distribution is not uniform. The 3D simulation results are presented on the right in Fig.14. In the simulation, all of the parallel windings are connected using the external circuit, which means the impacts of non-ideal vias and terminations are ignored. The percentage on each winding indicates the current share of that winding. The non-uniform current distribution causes higher conduction loss and uneven thermal stress. Here only the positive half cycle of current is shown when secondary winding #1 conducts. The distribution of the negative half cycle is also uneven in a similar manner.

Basic analysis was performed on this issue and some guidelines are summarized in [20], [21]. However, they are completely simulation based, which is time-consuming and non-convenient for iterative design and analysis. It also lacks physical intuitions. In [22], application of the extremum co-energy principle was proposed for prediction of the current distribution and AC resistance. However, it neglects the frequency effect. In [23], an analytic model was proposed based on Faraday's law and voltage balance. This model effectively predicts the AC winding resistance of a wide frequency range. An example of 8:1 transformer with primary windings in series and two secondary windings in parallel is illustrated. However, the problem with this approach is that the equations become very complicated when applied to a transformer structure with a greater number of parallel layers. For example, to solve for the four parallel primary windings and secondary windings in our case, it needs to build 32 differential equations with double integrals and then solve for 32 unknowns. The complexity continues to grow for more parallel layer designs. In [23], Visual-Basic codes are built to solve this problem.

To simplify the previous model, reduce the calculation burden, and gain some physical intuitions, a simplified model using the superposition method is proposed. First, two simple structures are studied. Then based on the superposition concept, these two structures serve as the building blocks for multi-layer parallel winding structures. When analyzing the structures, the magneto-quasi-static (MQS) and 1-D assumptions are still used. The first building block structure and circuit connection are shown in Fig. 15. It has one primary winding and two parallel secondary windings. A similar concept proposed in [23] is still used to calculate the current distribution of this block. Based on Ohm's law, the resistive voltage drop and induced voltage of the loop should balance. Combine Ampere's law and Faraday's law and solve the equation and the current distribution is as follows:

$$\frac{I_1}{I} = \frac{I_1}{I_1 + I_2} = \frac{\frac{coth\alpha h}{\alpha} + \frac{tanh\frac{\alpha h}{2}}{\alpha} + r2}{2\left(\frac{coth\alpha h}{\alpha} + \frac{tanh\frac{\alpha h}{2}}{\alpha}\right) + r\,1 + r2} \quad (1)$$

Where $\alpha = \sqrt{\frac{j\omega\mu_0}{\rho}}$. r_1, r_2 is the distance between secondary windings and primary winding, h is the copper thickness, ω is the switching frequency, and ρ is the resistivity. The distribution is related to the frequency and the distance between layers. The calculation and 3D simulation results are compared in Fig. 16. They match pretty well. The second building block is shown in Fig. 17. A similar calculation is done and the final current distribution is

$$\frac{I_1}{I} = \frac{I_1}{I_1 + I_2} = \frac{\frac{coth\alpha h}{\alpha} + \frac{tanh\frac{\alpha h}{2}}{\alpha} + r2}{2\left(\frac{coth\alpha h}{\alpha}\right) + r2} \quad (2)$$

The results also match with those from simulation, as shown in Fig. 18. Note that within certain r_2 and f_s range, all the current is on the secondary winding that is closer to the primary winding. This is also known as the "shielding effect".

The "shielding effect" concept can be further extended. If we are in the frequency range that the "shielding effect" holds for the basic primary-secondary-secondary layer arrangement, it can be extended to multiple layers. It means that on each side of the primary winding, no matter how many secondary layers there are, current will only distribute on the one secondary winding that is closest to the primary. It can be proved as follows. On one side of the primary winding, suppose there are n layers of secondary windings, as shown in Fig. 19. For the current distribution in winding s1 and s2, the same equations in

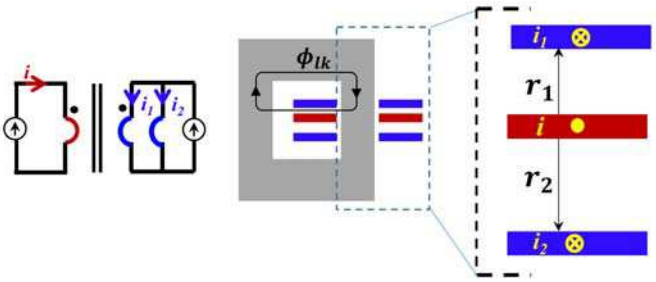
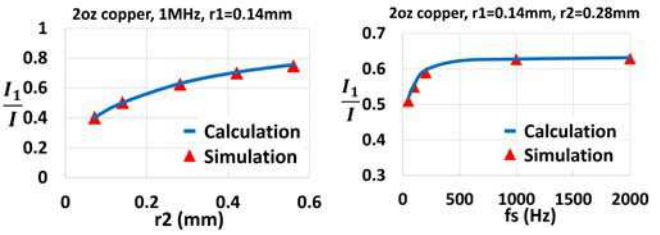


Fig. 15. First building block structure and circuit connection.



(a) Current distribution results of different r2 distances.

(b) Current distribution results of different frequencies.

Fig. 16. Comparison of current distribution results for building block #1 from calculation and simulation.

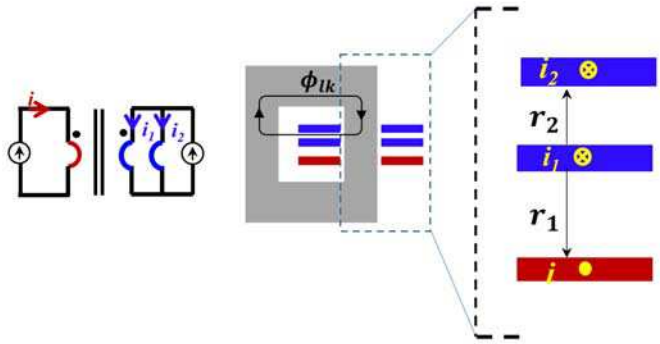
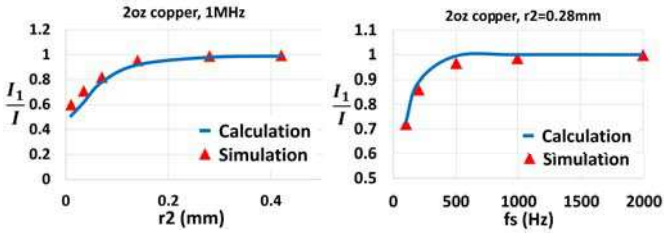


Fig. 17. Second building block structure and circuit connection.



(a) Current distribution results of different r2 distances.

(b) Current distribution results of different frequencies.

Fig. 18. Comparison of current distribution results for building block #2 from calculation and simulation.

the second building block are valid here. The only difference is just that the summation of i_1 and i_2 is not the primary current. But the current distribution expression on s1 and s2 are the same. Therefore, within the same frequency range, there is no current on s1, and it can be eliminated. The same derivation

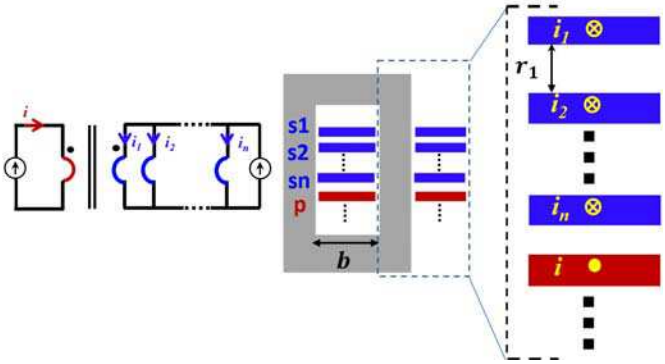


Fig. 19. Winding layer structure with n secondary layers on one side of the primary

can be processed on s2 and s3 and then s2 can be eliminated similarly. Following this sequence, we arrive at the end of the array, which is Sn, the secondary winding layer closest to the primary. Finally, we come to the conclusion that there will be no current on s1 to S(n-1). Note that it does not mean Sn has all the secondary current if there are secondary windings on the other side of the primary winding. This conclusion will be used later to simplify the winding structure.

Next, these two building blocks are combined for the object under study by the superposition method. For the layer scheme in Fig. 14, first assume there is only one excitation: primary winding p1. Based on the previous model, only the two secondary windings (s1, s2) next to p1 have current, while the other two secondary windings are blocked by the "shielding effect". And the current distribution on s1 and s2 can be calculated by the equation of building block #1. Define k equal to the current ratio between the first secondary current and the primary current. The k value can be obtained from (2), which is 2/3 in this case. Now the current on all secondary windings due to p1 is obtained. Following a similar manner, one can obtain the secondary winding current caused by p2, p3, p4, separately. For each secondary winding, according to superposition concept, the current is the summation of the current from four primary winding excitations individually. The final relationships are presented in (3)-(6).

$$s1 = k \cdot p1 \tag{3}$$

$$s2 = (1-k) \cdot p1 + k \cdot p2 \tag{4}$$

$$s3 = (1-k) \cdot p2 + k \cdot p3 \tag{5}$$

$$s4 = (1-k) \cdot p3 + p4 \tag{6}$$

Where p_i and s_i (i=1, 2, 3, 4) represent the current on that winding layer. After this, secondary windings can be used as excitation, and the same method is used to obtain the four primary currents. Finally, the eight relationships can be written

TABLE I
CURRENT DISTRIBUTION OF ORIGINAL LAYER SCHEME BY ANALYTIC MODEL

Current Distribution	First Layer	Second Layer	Third Layer	Fourth Layer
Primary	27.2%	27.2%	27.2%	18.4%
Secondary	18.4%	27.2%	27.2%	27.2%

in matrix form (7).

$$\begin{bmatrix} 1 & 0 & 0 & 0 & -1 & k-1 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & -k & k-1 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & -k & k-1 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & -k \\ -k & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ k-1 & -k & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & k-1 & -k & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & k-1 & -1 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} p1 \\ p2 \\ p3 \\ p4 \\ s1 \\ s2 \\ s3 \\ s4 \end{bmatrix} = 0 \tag{7}$$

The only thing left is to solve this simple homogeneous linear equation set. Note that due to the "shielding effect", the matrix is always highly sparse, which gives an immediate solution for current distribution. For this matrix equation, it has a non-zero one-dimensional solution space (8).

$$\begin{bmatrix} p1 \\ p2 \\ p3 \\ p4 \\ s1 \\ s2 \\ s3 \\ s4 \end{bmatrix} = a \begin{bmatrix} 1/k \\ 1/k \\ 1/k \\ 1 \\ 1 \\ 1/k \\ 1/k \\ 1/k \end{bmatrix} \tag{8}$$

Where $a \in R$. The distribution results of the analytic model are presented in Table I. They exactly match the simulation results (with some round-off error).

B. Symmetrical Layer Scheme

To improve the performance, a symmetrical layer arrangement is proposed and shown in Fig. 20. The model is built and from the equations, it is discovered with this structure, no matter what the distance is between layers, the current is always evenly distributed among all layers. This makes the solution more robust against FR4 thickness of PCB. In addition, because the current is evenly distributed, the AC resistance calculation in [24] still applies and will be directly used in the optimization process in the following section.

In the previous analysis, an ideal via structure is assumed. In the simulation, the termination and via structure proposed in Section III is applied on the new layer scheme. The simulation results of current distributions, in percentage, are presented in Fig. 21. With the via and termination impact, the current distribution of the symmetrical structure is no longer even. However, it still has much better current sharing performance than the unsymmetrical structure and the total winding loss is reduced by 10%. This impact is considered in the optimization procedure with a correction factor.

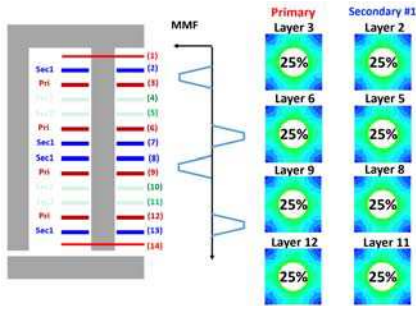


Fig. 20. Proposed layer scheme of the paralleled PCB windings and the current distribution in positive half cycle.

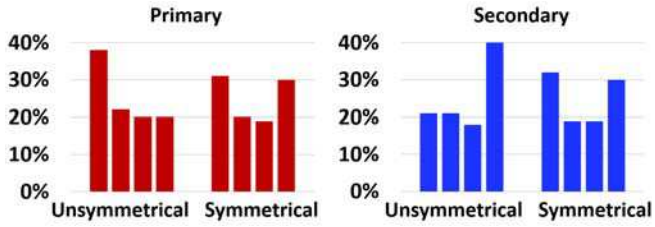


Fig. 21. Current distribution comparison of positive half cycle for transformer with via and termination design.

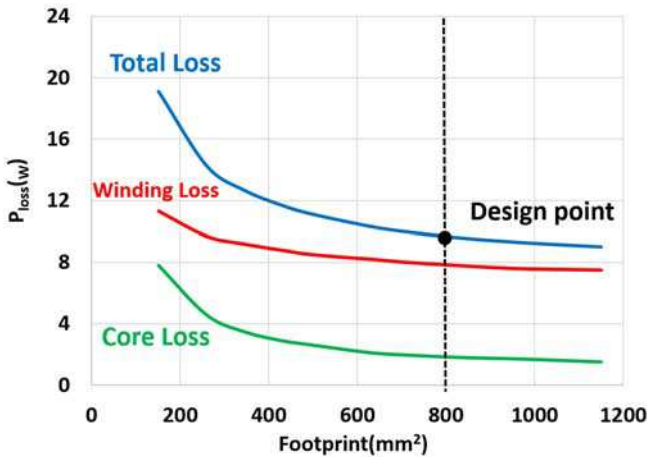


Fig. 22. Optimal transformer footprint vs. total loss.

V. DESIGN OPTIMIZATION AND EXPERIMENTAL RESULTS

After all of the above improvements, the transformer is optimized with the procedure demonstrated in [16]. The optimal copper thickness is selected to be 2oz. The winding loss is calculated based on [24] with the correction factor from the simulation. Combined with the rectangular voltage core loss model [25], the total transformer loss with the corresponding optimal footprint is calculated and shown in Fig. 22, where the design point is selected at the footprint of around 800mm^2, as a good trade-off between power density and efficiency. The loss breakdown of the converter is shown in Fig. 23. It is clear that the winding loss, which used to be a great portion, is minimized. (The shaded bar indicates the loss reduction by the improved transformer design.)

The proposed two-stage solution is designed and the hard-

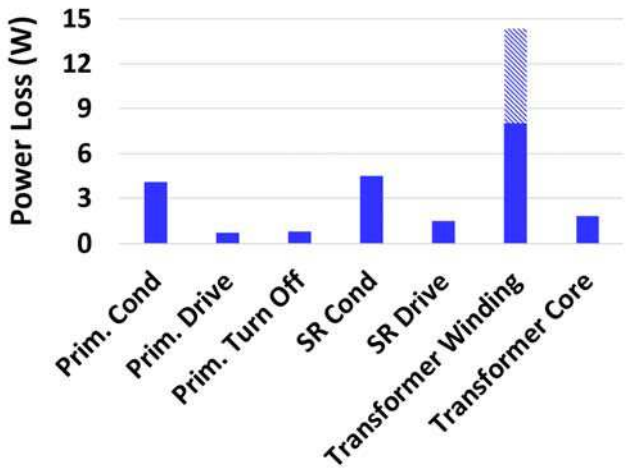


Fig. 23. LLC-DCX loss breakdown.

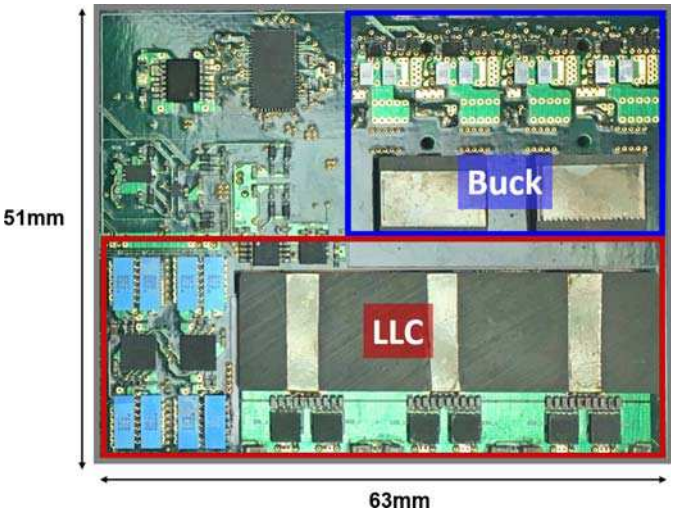


Fig. 24. Prototype of proposed two-stage regulated bus converter.

TABLE II
PROPOSED LLC-DCX CONVERTER PARAMETERS

Parameter	Value
Switching Frequency	1MHz
Input Voltage	36V
Output Voltage	12V
Output Power	1kW
Primary Devices	EPC2020
Secondary Devices	BSZ0500NSI
Primary Drivers	LM5113
Secondary Drivers	FAN3122
Magnetic Core	ML91 (Hitachi)

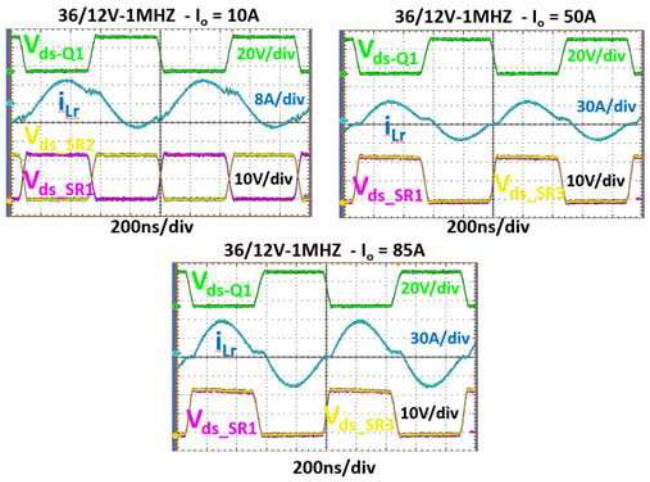


Fig. 25. Operation waveforms of LLC-DCX at light load (10A), half load (50A), and full load (85A).

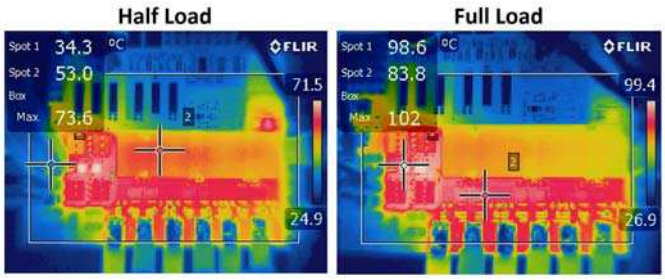


Fig. 26. Thermal images of LLC-DCX at half load (left) and full load (right).

ware prototype is built, as shown in Fig. 24. The design parameters are presented in Table II. The LLC operating waveforms with ZVS at light load, half load, and full load are shown in Fig. 25. Fig. 26 shows good thermal performance at half load and full load (wind speed 5m/s). The estimated and measured efficiency of LLC-DCX is shown in Fig. 27. Note that the first-stage Buck regulates the input of LLC at 36V, so the LLC always works at this optimal efficiency regardless of the 40V to 60V bus voltage variation. The efficiency of the two-stage converter is also shown in Fig. 27. With the LLC achieving 97.6% peak efficiency, the bus converter achieves 96% peak efficiency and 615W/in^3 power density. The control circuits, auxiliary power supply, and all the input/output and 36V dc-link capacitors are included in the power density calculation. The bus converter is compared with the state of the arts in Table III. With close peak efficiency, this design has the highest power rating and power density. Note that in the two-stage prototype, the connections between two stages are not optimized. It still has the potential to improve efficiency and reduce the footprint.

The manufacturing tolerance of the LLC converter is also considered. First, for Lr and Cr tolerance, the variance of resonant inductance and capacitance will influence the operating states of the LLC. However, since in our design Lr is much smaller than Lm the magnetizing inductance (Lr = 8nH, Lm=1.3uH), the gain curve of the LLC is very flat at switching frequency around resonant frequency. In this design, if we suppose +/−10% tolerance on both Lr and Cr, the switching frequency would be about +/−10% away from the resonant frequency. With the gain curve known, it is easily

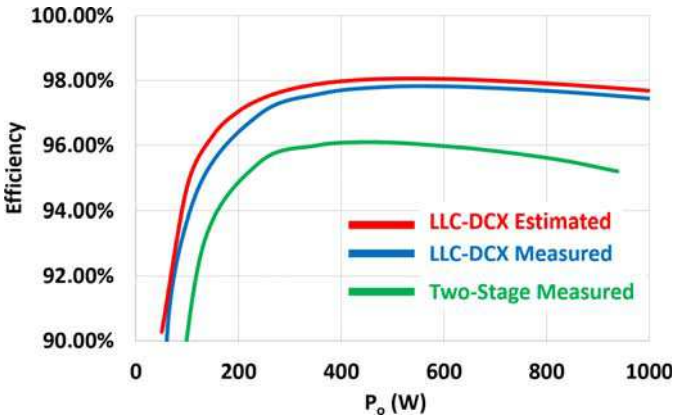


Fig. 27. Estimated and measured efficiency of LLC-DCX and two-stage bus converter at 48V input.

TABLE III
COMPARISON WITH THE STATE-OF-THE-ARTS

Prototype	Power Rating	Peak Efficiency	Full-Load Efficiency	Power Density
Proposed Converter	1000W	96%	95%	615 W/in^3
GE QBVE067A0B41	800W	96.3%	96%	480 W/in^3
Delta Q54SG	600W	96.5%	95.8%	360 W/in^3
SynQor PQ60120HZx50	600W	95.5%	94.9%	254 W/in^3

obtained that the output voltage is within $+/-1\%$. In terms of the efficiency, two extreme cases where Lr and Cr are both $+10\%$ and -10% from the nominal values are tested. It is found out that the efficiency variation is also very small (less than 0.2% efficiency drop). Second, for the Lm tolerance, the manufacture errors of air gaps and core dimensions cause the variation of the magnetizing inductance value. Since we do not use controller for the DCX design, we can consider this tolerance in the first place by extending the dead time to ensure ZVS in the worst-case scenario when the Lm is the maximum and the magnetizing current is minimal. Theoretically, longer dead time means higher circulating energy and higher conduction loss. But when reflected to final efficiency, the impact of this small amount of change in dead time is very small, which is less than 0.1% peak efficiency in this case. Based on the analysis above, the LLC-DCX is very robust against the manufacturing tolerance in terms of voltage ratio and efficiency.

VI. CONCLUSION

This paper studies the design and optimization of a high frequency, high current LLC converter for the 48V bus converter. First, a GaN-based LLC circuit is proposed with matrix transformer. A merged winding structure is created to achieve better flux cancellation and lower AC winding loss. Second, a novel interleaved termination and via structure is proposed resulting in great loss reduction. Third, a 1-D analytic model is proposed to estimate the current distribution of parallel winding layers in the PCB-winding transformer. And a symmetrical winding layer arrangement is used to improve the current sharing and further reduce the losses. Finally, the prototype for the 1kW two-stage bus converter is developed, with the high peak efficiency of 96% and a power density of 615W/in^3.

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