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Hybrid MEMS-CMOS ion traps for NISQ computing

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Abstract. Surging interest in engineering quantum computers has stimulated significant and focused research on technologies needed to make them manufacturable and scalable. In the ion trap realm this has led to a transition from bulk three-dimensional macro-scale traps to chip-based ion traps and included important demonstrations of passive and active electronics, waveguides, detectors, and other integrated components. At the same time as these technologies are being developed the system sizes are demanding more ions to run noisy intermediate scale quantum (NISQ) algorithms, growing from around ten ions today to potentially a hundred or more in the near future. To realize the size and features needed for this growth, the geometric and material design space of microfabricated ion traps must expand. In this paper we describe present limitations and the approaches needed to overcome them, including how geometric complexity drives the number of metal levels, why routing congestion affects the size and location of shunting capacitors, and how RF power dissipation can limit the size of the trap array. We also give recommendations for future research needed to accommodate the demands of NISQ scale ion traps that are integrated with additional technologies.

1. Background

Since the demonstration of surface ion traps in 2005 [1, 2], dozens of different designs have been fabricated and their quality, robustness, and consistency has steadily improved. Surface ion traps have supported experiments requiring quantum coherent operations by multiple research groups, and in many cases the surface traps offered performance and functionality not achievable with a non-lithographic trap. Some of the advances during the last decade include: fabricating a diverse range of trap architectures (e.g. linear, junction [3, 4], ring [5], and two dimensional nodal traps [6]); improving the design to maximize trap strength and lower power dissipation; reducing exposed dielectric surfaces that support unpinned charges; reducing motional heating with surface treatments [7] and cryogenic operation [8]; incorporating on-chip microwave [9, 10] and optical [11, 12, 13] waveguides; fabricating active and passive electrical

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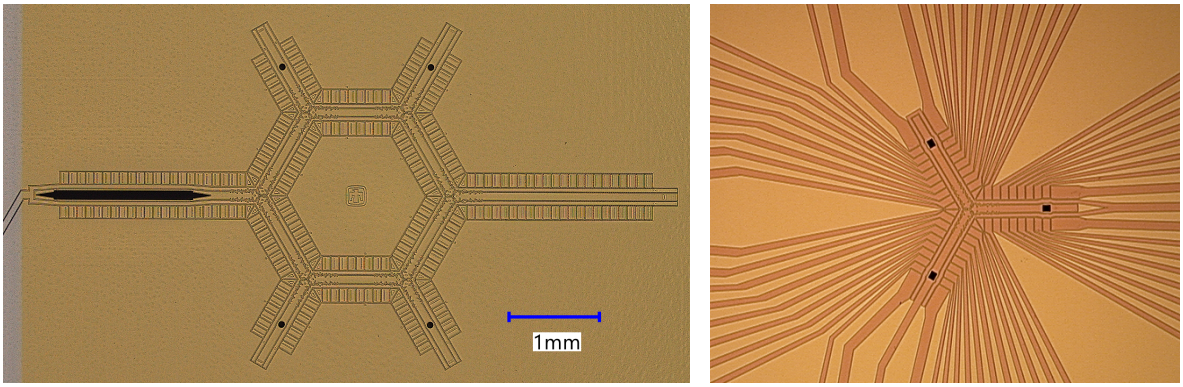
[14] and thermal components [15]; and advancing fabrication and packaging to increase device yield and ease of integration with the experiment.

The last decade has also brought additional clarity about the attributes required for ion traps as they evolve in size and complexity. These features depend on whether the architecture primarily relies on individual, localized gate operations and ion transport [16], or a reduced amount of shuttling but additional photonic interconnects [17]. The NISQ regime [18] is not quantitatively defined, but in this article we consider it to involve about 50 to 100 ions and more importantly employ the transport or remote entanglement features needed to connect those ions. For both architectures, a modest number of ions (tens) can be addressed with laser beams that cross the surface of the trap, provided the lateral dimensions of the trap substrate do not interfere with tightly focused laser beams; this has been the primary method for building a multi-ion system to date [19, 20]. For larger NISQ scale devices the trap array will extend from a linear to a planar layout, necessitating a signal delivery scheme employing on-chip optical or microwave waveguides to achieve the desired addressability and avoid crosstalk. Integrated light modulators [21] and photon detectors [22] at UV wavelengths may also be required for increased functionality and individual qubit addressing.

Several variants of microfabricated surface ion traps exist, differentiated by whether the substrate is a semiconductor (typically silicon) or insulator (e.g. sapphire), as well as the number of metal layers (one versus multiple). The devices discussed in this article are fabricated using silicon substrates and have four or more metal levels. While alternative materials such as fused silica and sapphire are appealing for their insulating properties and compatible with bulk and laser-based MEMS (micro-electro-mechanical-systems) processing techniques, the implementation of active CMOS devices and multiple BEOL (back-end-of-line) metal levels is challenging, at best, for these substrates. Consequently, silicon substrates are the most promising substrate material for scaling to the NISQ regime. Physical properties like capacitance, ohmic loss, dielectric loss, voltage breakdown, inductance, and thermal conductivity have been engineered to operate within acceptable performance values (like total power dissipation) for current numbers of ions. However, scaling to NISQ sizes will require substantive fabrication and design changes that employ both CMOS and MEMS processing techniques. These necessary advances and other trap fabrication considerations are the focus of this paper.

2. Topology, geometry, fabrication, and surface effects of silicon-based microtraps

The use of silicon (Si) as the substrate for fabricating an ion trap allows for device processing that combines VLSI (very large-scale integration) circuit approaches and MEMS techniques, employing thin-film deposition, subtractive etching, and bulk and surface micromachining methods. CMOS-inspired BEOL techniques enable lead routing and electrode definition in multiple metal levels separated by inter-metal dielectric (IMD) layers, capacitating nearly arbitrary surface trap geometries by virtue of the sub-



(a) (b)

Figure 1: Optical microscope images of a (a) hexagonal circulator trap and (b) Y junction trap. The hexagonal ion trap array shows islanded electrodes which are inside the ring and only accessible using multiple metal levels with subsurface lead routing. An ion was successfully shuttled around this trap using the same voltages at each junction (some of which were co-wired), demonstrating that their geometric consistency leads to repeatable behavior. In contrast the Y junction trap has top metal leads; due to the fixed locations of perimeter bond pads these leads are not symmetric relative to the electrodes and therefore the voltage solution is orientation specific.

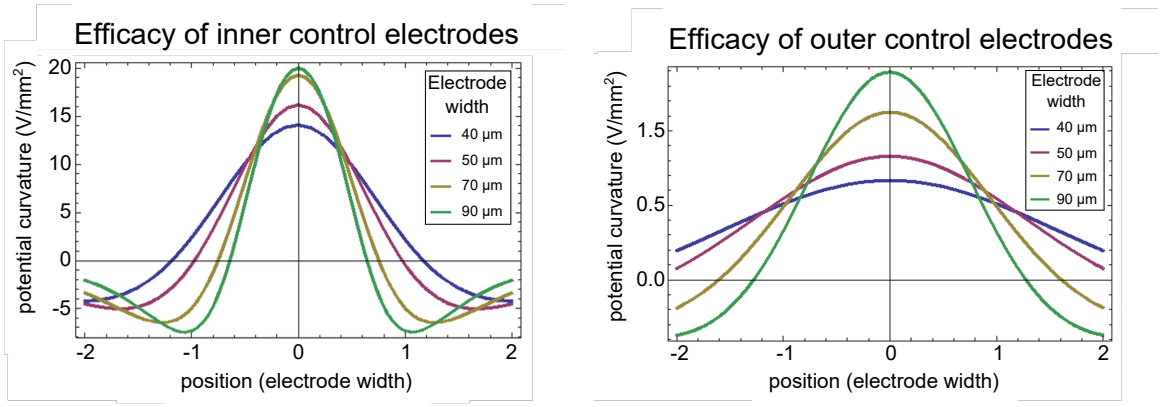
surface routing of electrical leads in the planarized layers of conductors and insulators. Trap electrodes built using CMOS BEOL processing, including the RF electrode, are most commonly in the top metal layer for a 2D, planar surface trap [23], but certain topologies benefit from having control and/or ground electrodes in layers below or above the RF electrode to render a 2.5D trap. 2.5D refers to the concept of 3D features at the scale of the thin films defining metal and dielectric layers, though they encompass only a fraction of the total thickness of the chip or substrate.

The magnitude of voltage (100 V to 300 V RF amplitudes) applied to ion traps constitutes a defining difference compared to CMOS integrated circuits (typically <3.5 V for CMOS transistors). This difference requires significantly thicker dielectric films to prevent RF breakdown [24], as well as thicker metals to lower resistance and capacitance and therefore ohmic power dissipation. These factors drive an interdependence between electrode geometry, topology, and processing that is relatively unique to ion traps.

2.1. Electrode topology and geometry

The relative positions of trap electrodes determine routing and in turn integration parameters like lead widths and numbers of metal layers. Islanded electrodes, like those inside the hexagon in figure 1a, are those which do not have a direct top metal path from the electrode to perimeter bond pad and therefore require subsurface lead routing. Interior control electrodes between RF rails also require subsurface routing. While it is easier to fabricate inner electrodes that are not axially segmented (e.g. both traps in figure 1), and they can still be transversally split to provide significant

principal axis rotation, axially segmented inner electrodes are much more efficient at generating an axial electric field as shown in figure 2. This example is based on the "High Optical Access" (HOA) trap fabricated at Sandia and shown in figure 5a. The potential curvatures were calculated with a boundary element model simulation but are qualitatively similar to those shown for the analytic calculation in figure 3 of [25]. In this trap with a 70 μm ion height, the inner electrodes have an ion-electrode distance of 85 μm and the maximum efficacy (potential curvature per volt applied) is found for widths of around 90 μm ; this is consistent with the rule of thumb that the maximum efficacy occurs for an electrode width close to the ion-electrode distance. For the segmented outer electrodes, where the ion-electrode distance is 165 μm, the generated curvature is about 9× smaller for the same electrode width-to-distance ratio. For electrode widths considerably larger than the ion-electrode distance, the efficacy is reduced and a local minimum is found at the center of the electrode. The curvature at the end of an electrode segment (±0.5 in this figure) becomes small in the limit of large electrode width; in this case large voltages would be needed to create sufficient curvature for an ion at the gap between two neighboring electrodes.



(a) (b)

Figure 2: This figure compares the efficacy (parameterized by the potential curvature) of (a) axial electrodes inside the RF electrodes to (b) axial electrodes outside of the RF electrodes for the HOA trap. These plots show the potential curvature at the ion for a unit voltage applied to a single axial electrode while grounding the rest. For the inner electrodes with an ion-electrode distance of 85 μm a maximum efficacy is found for widths around 90 μm; smaller electrodes that are significantly below the ion-electrode distance have more fine-grained control but less potential curvature. For segmented outer electrodes with an ion-electrode distance of 165 μm the highest achievable curvature is about 9× smaller for the same electrode width-to-distance ratio and the most effective electrode width exceeds 90 μm in this example.

Efficiency is important given the limited voltage output of control electronics and the high field gradients sometimes required to shape the potential well, correct for high spatially variant background fields, or aid in splitting, reordering, and joining ions. Finally, even electrodes which are not islanded benefit from subsurface routing to provide a uniform electrode geometry and therefore consistent transport solutions.

These arguments only grow stronger as the trap array expands to accommodate NISQ algorithms. A consequence of axially segmented inner electrodes is that a minimum of four metal layers are needed to leave the bottom ground plane unbroken and limit RF dissipation into the substrate while also screening the control electrode leads that cross under the RF electrode with intermediary grounded metal.

NISQ systems will weight performance characteristics differently than smaller trap arrays. For instance, although trap depth may be treated as one of many parameters to optimize (e.g. secular frequency, ion height), it is reasonable to weight it more heavily in an experiment with more ions that requires a longer ensemble lifetime. Full ion flight simulations can quantify this tradeoff; for example the simulations in figure 3 reveal the optimal voltage and frequency to maximize trap depth, accounting for decreasing depth due to regions of the nominal trapping volume that become unstable as the adiabaticity parameter becomes too large.

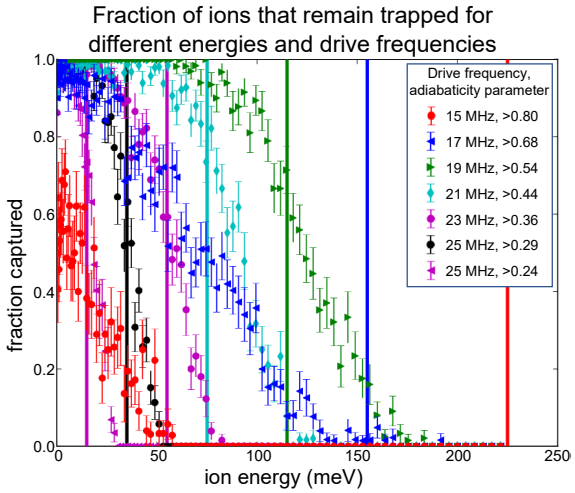
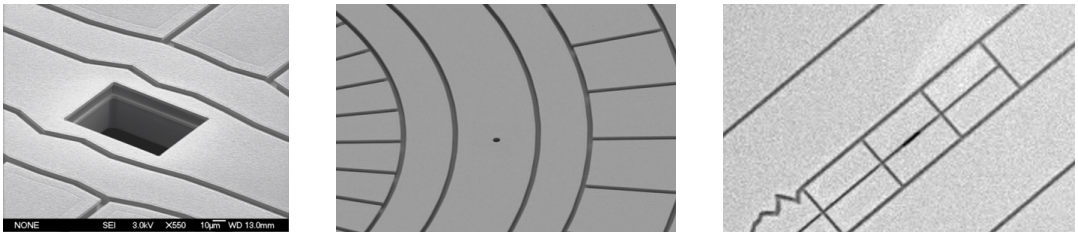


Figure 3: Flight simulations of ions in a microfabricated surface trap that record the fraction trapped as a function of initial vertical velocity for different RF drive frequencies with the same voltage. The vertical lines are the trap depths calculated based on the pseudopotential, ignoring the stability parameter. At low drive frequency (15 MHz) the trap is unstable and even very slow ions are not trapped reliably. The maximum velocity an ion can have and still remain trapped is highest for 19 MHz; increasing beyond 19 MHz does not improve the stability but reduces the pseudopotential and simulated depth.

2.2. Chip definition and through-hole perforations for loading and optical access

Small and precisely defined holes that pierce the silicon die are useful for loading neutral atoms from an atomic source below the chip. While top-side loading is also possible, backside loading is advantageous for screening the top metal and already trapped ions from the hot vapor. Since loading is a stochastic process this latter benefit is particularly valuable for NISQ applications; current ion numbers may operate efficiently by dumping and reloading all ions when one is lost, but a larger system will have less downtime if

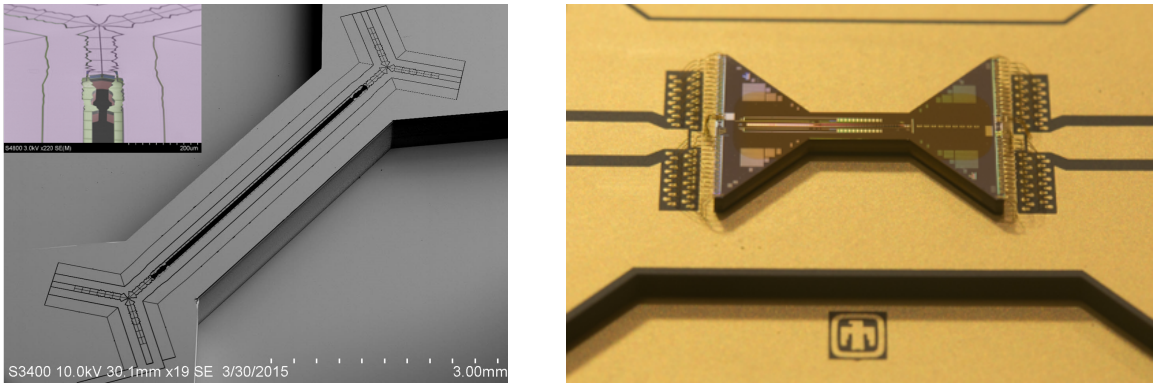


(a) (b) (c)

Figure 4: SEM images of loading holes in different traps, including (a) a $50\,\mu\text{m} \times 80\,\mu\text{m}$ loading hole which required a perturbation to the surrounding RF electrodes to limit the axial pseudopotential, (b) a $10\,\mu\text{m}$ diameter loading hole which still perturbed the axial pseudopotential [5], and (c) a narrow loading slot in and under the $3\,\mu\text{m}$ gap between the center pair of rectangular electrodes with no electrode perturbation. All were successfully loaded from a backside oven.

only lost ions are replaced. Loading holes have become less intrusive over time; early loading holes with lateral dimensions of tens of microns have been reduced to several microns, allowing their placement in electrode gaps such that there is no deviation of the top electrodes (figure 4), and more importantly minimal pseudopotential perturbation.

An HOA linear surface trap, shown in figure 5a, is lithographically defined to accommodate tightly focused laser beams from the side and through the chip. The bowtie shape and through-chip slot are fabricated in the same way as loading holes. This platform has been used for multiple traps and provides a maximum numerical aperture of 0.11 from the side (perpendicular to the isthmus) and 0.25 through the slot. The 1.2 mm isthmus width could be narrowed further but was chosen to balance the competing needs of routing many low resistance leads to control electrodes against accommodating tightly focused laser beams across the surface, with priority to the latter. What is not visible in the image is the lead routing congestion, with hidden electrical leads in the underlying five metal layers filling the isthmus width. While reducing isthmus width may be an option in the case of a single linear trap with few electrodes, a NISQ-scale trap utilizing bulk optics but with more control channels will likely require either a wider isthmus, additional metal levels for routing, or narrower electrical leads (resulting in higher resistance and self-inductance). In this case, maintaining the same width isthmus and adding metal levels is the most practical approach. There are, however, limits to the number of metal levels that can be added because the thick IMD and metal thin films needed to accommodate high voltage RF and achieve low lead resistance causes increased stresses, and consequently thermal management and yield issues. The use of through substrate vias (TSVs) [26] may relieve routing congestion and the demand for more metal layers, depending on the electrode size, pad pitch on the interposer, and available real estate in that region of the trap.



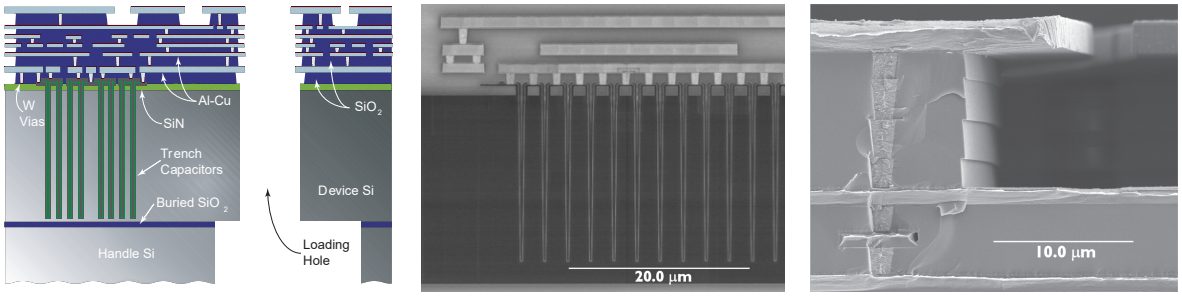
(a) (b)

Figure 5: (a) SEM image of an "HOA" trap on the high optical access platform, with an inset false color SEM image looking down the slot. The inner control electrodes are highlighted in green, while the outer control electrodes are shown on the outside of the RF electrodes and have a diagonal segmentation near the junction. (b) The "Phoenix" trap is a linear trap fabricated at Sandia on the same high optical access platform and is shown here in a custom aluminum nitride package.

2.3. Fabrication: materials, processes, feature sizes, and design rules

The multi-level metal surface traps fabricated here are realized by adapting a 350 nm, 3.5 V CMOS BEOL process to route and build trap electrodes. This process uses an alloy of aluminum and copper (Al-½%Cu) for all metal layers, planarized silicon dioxide (SiO_2) IMD, and vertical electrical connections with tungsten (W) vias. The metal layer thicknesses are typically 2.45 μm for the layer(s) with RF leads and 1.35 μm for the other metal layers. Chemical mechanical polishing of the plasma enhanced chemical vapor deposited (PE-CVD) SiO_2 results in planarized IMD layers typically 1-3 μm thick, or in some renderings as much as 10 μm thick for the top IMD just under the top metal RF electrode. Vertical electrical vias connecting adjacent metal levels are either 0.7 or 1.5 μm of CVD deposited W. The substrate is typically 20-25 μm of 2-20 ohm-cm top-Si separated from a 600 or 700 μm handle-Si wafer by a 1 μm buried SiO_2 layer (BOx).

These surface trap chips are shaped and perforated by applying MEMS processing techniques, employing deep reactive ion etching (DRIE) of both top- and handle- bulk Si to render lithographically aligned through-holes for ion loading and micro-optics integration [27]. Post-processing MEMS-type "release" etches remove SiO_2 from around and just under trap electrodes and singulate the chips from the Si wafer. DRIE Si processing enables the realization of arbitrary chip shapes, such as the bow-tie shaped HOA trap chip platform in figure 5 [28]. Deep Si etching also defines trenches used for high areal-density on-chip capacitors for RF voltage shunting, shown in figure 6b. These capacitors have nanofarad-scale capacitance values, breakdown voltages of ∼30 V, leakage currents of $< 1\mu A$ at 20 V, and an areal capacitance density of 94.3 fF/μm^2 [29], about 100× higher than on-chip metal-insulator-metal (MIM) capacitors. Both this density and monolithic integration with the trap are critical for NISQ devices, which



(a) (b) (c)

Figure 6: (a) Schematic cross-section of a six metal level trap, (b) a SEM cross-section of a three metal level ion trap routing and in situ trench capacitors, and (c) a SEM cross-section image of deterministic SiO_2 set-back underneath trap electrodes.

require more electrodes and longer leads connecting central electrodes to the perimeter.

To ensure acceptable device yield and account for variances in fabrication, design rules that dictate the geometric constraints and the range of values for thin films and electrical vias are employed. A schematic diagram (figure 6a) of a six-metal level trap shows some of these relevant dimensions. The trap RF rails are connected and routed in the top metal level, except where a cross-under is necessary (e.g. figure 1a); the different metal levels and are used as follows:

- bottom metal layer (M1); substrate ground plane and in rare cases for control electrode routing (not preferred);
- intermediate metal layers (M2, M3, . . .): control electrode routing, ground, possibly control or RF electrodes;
- penultimate metal layer: ground, possibly control or RF electrodes;
- top metal layer (M-Top): control and RF trap electrodes (including routing), ground.

The first metal layer (M1) provides a ground plane to electrically shield RF currents in the trapping structure from the lossy silicon, and even routing of control electrodes in M1 is usually avoided. The intermediate levels of metal are used for electrical lead routing from I/O pads to trap electrodes and allow leads to cross on separate layers. In the trapping region, however, the penultimate or an intermediate metal layer is frequently grounded underneath RF electrodes and leads to screen RF currents from the underlying control electrode leads. Metal covers the top of the entire trap chip area except at the gaps between RF leads, control electrodes, and grounded regions and also at the edges of the chip where I/O wirebond pads reside. The SiO_2 IMD between adjacent metal layers serves as an insulator and a mechanical support for M-Top, and is controllably etched back at the gaps of M-Top such that metal trap electrodes overhang the supporting SiO_2 pillars. This minimizes the line of sight from the ion to any dielectric that might support charge buildup and allows both evaporative coating of the trap electrodes with an arbitrary metal, typically gold (Au), and front-

side ablation loading without causing shorts (figure 6c). Any overhanging cantilever or suspended electrode will deflect in response to forces exerted by the applied RF voltage. The vibrational properties can be calculated using equations developed for MEMS; for overhang distances $<5\,\mu$m the resonant vibrational frequency is above 50 MHz with amplitudes less than 10 nm. While these vibrations would not couple with ion motional frequencies, the pull-in voltage should be simulated to ensure it is well above the planned applied voltage and resonant frequency; existing traps typically have pull-in voltages that exceed 1 kV.

Requirements for packaging trap chips include compatibility with ultra-high vacuum and cryogenic environments, line-of-sight access for atoms from the atomic source to the ion trapping site, laser access to the ion for atomic state manipulation and read-out, and electrical delivery of RF and DC signals. Additionally, overall cleanliness needs to be preserved and foreign contaminants (atmospheric particles and chemicals) avoided during the packaging process. Best practice is that all device assembly occurs in a Class 100 or better clean room and that traps are plasma cleaned to remove adventitious contaminants prior to wire bonding. While commercial off-the-shelf (COTS) packages have been readily adapted for ion trap chip packaging, we find that a custom, co-designed package can be optimized for best performance of hybrid MEMS-CMOS traps. For the traps here, custom packages consist of either high temperature co-fired ceramic (similar to alumina) or aluminum nitride (AlN), both of which meet the requirement for ultra-high vacuum and cryogenic operation. AlN provides a higher thermal conductivity than alumina (150 W/m·K versus 14 W/m·K) and a lower coefficient of thermal expansion (4.7 versus 7.1) that is closer to the thermal expansion coefficient of silicon (2.6). While these properties make AlN preferable for removing heat and reducing stress during a bake, alumina packages still perform acceptably well. Important geometric and electrical routing attributes of these packages are:

- a through-package loading hole, typically larger than and matching the position of the through-hole on the trap chip;
- a raised pedestal on which the ion trap chip rests that is high enough to limit the scatter of laser light delivered using bulk optics;
- electrical I/O pads for wirebonds at opposing ends of the trap chip such that optical access is not obstructed.

Custom packages have also been optimized to minimize the resistance of the RF signal grounds and include solder die attach pads for using gold-tin (AuSn) eutectic solder to mechanically, thermally, and electrically connect the trap chip to the package. This also allows for ready interconnection of through silicon vias (TSV) on the trap chip, which may be necessary for larger NISQ devices. The trap and package assembly process uses a flip chip bonder to align the chip to the package and solder it in place.

Since experimental installation and setup takes considerable time, trap and package assemblies are carefully selected prior to use. Each chip is checked for optical defects with

a high magnification and stereo-zoom optical microscope and then packaged. Electrical testing is performed between all electrodes to identify any shorts and test for continuity to ensure no electrodes are floating. All trench capacitances are measured, and their leakage current verified for both bias directions. Lastly, a laser scanning confocal microscope is used to measure the height between the top metal of the ion trap and the penultimate level, which is then used to model the electric fields and generate control solutions.

2.4. Surface effects and motional heating

The small ion-electrode distances inherent to surface traps amplify the effects of charge build-up on exposed dielectrics, defects in electrode geometry, surface roughness, and electric field noise associated with trap materials [30, 31]. The first three of these sources primarily impact trap stability, both in time (e.g. compensation field and motional frequency stability) and from device to device. For most surface traps we typically observe drifts in the compensation fields of less than 10 V/m over 24 hours, which can be corrected by applying less than 20 mV to an appropriate set of electrodes. The same consistency applies to separate but congeneric traps; in a recent set of experiments with different Phoenix traps [15], the same voltage solution successfully trapped and the correcting compensation fields were within 300 V/m of each other. We attribute this consistency to electrode geometry uniformity and overhung electrodes that screen ions from possible charges on the IMD SiO_2. Minimizing fluctuating electric fields from the trap will be even more important for NISQ scale devices with more ions per electrode and subsequently fewer degrees of freedom to correct for background fields.

Ion traps with slots for vertical beam access have typically displayed greater performance variation than their pure surface trap cousins (with no slot and minimal loading holes), and interestingly this variation is strongest in the measured heating rates. We attribute this to unintended exposed Si on the vertical sidewalls of the top Si in the slot. As an example, the heating rate measured on two separate Phoenix traps with complete sidewall metal coverage was substantially (about 5 times) lower than an HOA trap with incomplete sidewall coverage. Our treatment has ranged from oblique angle metal evaporation with a variable angle rotating substrate holder that can leave pockets of exposed silicon, to maximum angle deposition of thick titanium ($0.1\,\mu$m), platinum ($0.1\,\mu$m), and gold ($0.25\,\mu$m) using a high speed planetary substrate holder that completely and uniformly coats the sidewalls; the latter technique was used on the trap measured in figure 7.

Electrode geometry variations due to fabrication are minimal and typically can be ignored. The same is true of the surfaces of evaporated metals, which have multi-line arithmetic mean roughness (R_a) values less than 10 nm and maximum roughness values (R_z) less than 60 nm. Since both are much smaller than the typical ion height they do not noticeably influence the trapping potential, though surface roughness may play a role in anomalous heating, a correlation which is still being investigated [31, 32]. Voltage noise

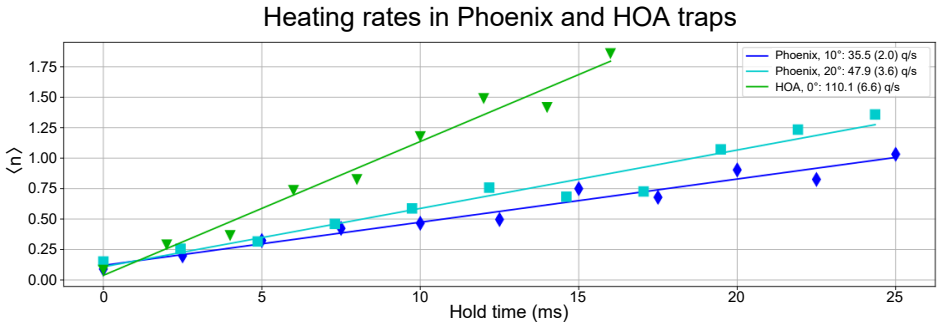


Figure 7: Heating rate measurements using the sideband thermometry technique for a $^{171}Yb^{+}$ion in the Phoenix-2 and the HOA-2.1 trap [15]. Using the Phoenix-2, the measurements were made on a radial mode at 2.3 MHz for two different rotations of the principal axis, 10 and 20 degrees from horizontal. On the HOA-2.1, the measurements were made on the 2.4 MHz radial mode for a principle axis rotation of 0 degrees.

sources which are correlated across the electrode (like technical noise on the DAC) have a d^{-2} distance dependence with ion height d. Once those sources are eliminated, the more pernicious "anomalous" source dominates with a d^{-4} dependence. This unfavorable scaling is blunted by the increased trap frequency that can be achieved for smaller values of d. In-situ surface treatments [7, 33] and cryogenic operating temperatures [34] have been effective at reducing electric field noise and therefore motional heating, but there are conflicting results regarding the decrease in heating rates and it may also be very dependent on the trap materials, manufacturing processes [32, 11], and surface treatment conditions.

The number of sequential entangling gates needed to take advantage of more ions depends on the algorithm [35], but can scale rapidly with system size (e.g. $\mathcal{O}(N^4)$ for unitary coupled cluster algorithms [36]). Current trapped-ion QC demonstrations can already be limited by motional heating [37] that accumulates during the algorithm, and even the best rates measured thus far when operating at cryogenic temperatures may not be low enough to perform hundreds of gates at sufficiently high-fidelity. NISQ scale algorithms will therefore likely require sympathetic cooling with another species or isotope. Even with sympathetic cooling, lower heating rates are extremely beneficial for reducing the infrastructure and time cost associated with cooling. Therefore continued work in understanding heating rates and how they vary with frequency, trap temperature, and surface proximity is essential for making surface traps that can achieve high fidelity gates. To enable compatibility with future heating rate advances, it is important for NISQ-scale traps to remain operable at cryogenic temperatures and accommodate new metals or surface treatments that might be discovered. For these reasons the surface traps described here emphasize low RF power dissipation (so as not to exceed the cryogenic cooling capacity) as well as maintain overhung electrodes that can accommodate evaporated metals and surface treatments while screening the dielectric sidewalls.

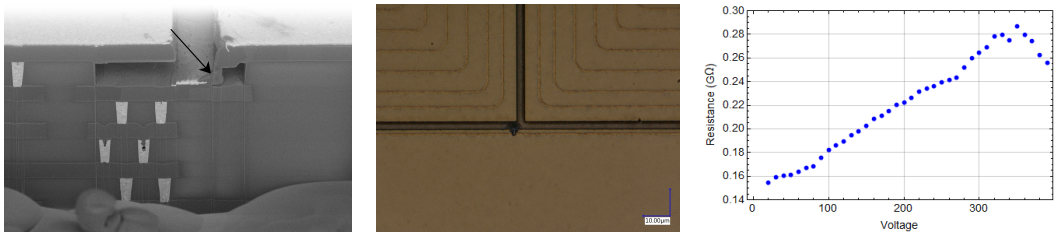
3. Electrical properties of microfabricated ion traps

The first surface ion traps consisted of electrodes defined in a single metal layer on an ideal low-loss substrate like sapphire or alumina [2]. This geometry has an inherently low RF to ground capacitance and subsequently low RF power dissipation, and the laterally defined electrode gaps can be easily designed to achieve a separation that prevents voltage breakdown. Traps fabricated on silicon wafers usually require a ground plane under the RF electrode and lead to limit losses into the silicon substrate [38], and is separated from the RF by 2 to 10 μm of SiO_2 [29]. Initial traps of this type focused on increasing dielectric thickness to prevent RF voltage breakdown; while that challenge is usually vincible (though sensitive to processing variables), the desire to reduce RF power dissipation has grown in importance. This can be achieved by increasing the oxide thickness to lower capacitance, a strategy that has been successful for the past decade because it was straightforward to achieve reasonable power dissipation for the trap sizes that were used.

NISQ scale devices will stress this approach to reducing power loss. For the same lateral RF electrode dimensions, ohmic power losses scale as the cube of the electrode length. In current traps the main contributor is the lead between the bond pad and the trap, but those roles will reverse for NISQ devices when the trap itself will contribute the majority of power dissipation. In the subsections below we describe these issues in greater detail and propose techniques to maintain acceptable power loss for NISQ scale trap arrays. Throughout this section we use parameters that are relevant for ytterbium ion trapping experiments, specifically a 300 V RF amplitude at 50 MHz. Some challenges are alleviated for lighter ions that require lower RF voltage, but the trends discussed below have general application.

3.1. RF breakdown

RF voltage breakdown can occur across the gap from an RF electrode to a ground or control electrode (which is capacitively RF grounded), along the dielectric surface from the RF electrode to the underlying ground plane, or through the dielectric bulk to the ground plane. The voltage at which breakdown occurs is affected by dielectric properties, surface/edge morphologies like field concentrating asperities, surface contamination, local pressure, and temperature increases resulting from power dissipation. These properties can be variable, hard to measure, and unpredictable, leading to a lower voltage breakdown than would be predicted based on ideal dielectric properties. Vacuum quality does not play a significant role; for distances exceeding 4 μm Paschen's law is applicable and the breakdown voltage through the empty gap exceeds several kV. For shorter distances, approaching 1 μm and below, a fixed breakdown field of 350 V/μm serves as a useful lower bound [39, 40], and since the gap between RF and ground generally does not fall below 2 μm the breakdown voltage exceeds the applied voltage by a factor of two or more. Breakdown is accompanied by a surge of current and subsequent metal heating and evaporation/sputtering, which can create a short between the RF



(a) (b) (c)

Figure 8: (a) Cross-section SEM image of a trap RF electrode at the location of a short to ground. The electrical vias are the light gray trapezoids and are surrounded by oxide. The metal layers are the slightly darker grey horizontal stripes. A short is indicated by the black arrow that points to metal that was liquefied and bridged the gap from the top RF electrode to the grounded layer beneath it. (b) An optical microscope image of the same short, before the trap was cross-sectioned. (c) The measured resistance of the RF trace as a function of applied DC voltage. There is a linear increase in resistance up to about 350 V, where the leakage current starts to increase disproportionally to the voltage and the resistance drops. This non-monotonic behavior is the first indication of dc breakdown prior to permanently damaging the device.

electrode and a ground or control electrode. Figure 8 shows post-mortem images of an ion trap that has suffered catastrophic voltage breakdown; we suspect the mechanism for this was field emission rather than surface flash-over because the molten metal is not present at the oxide surface.

Voltage breakdown can be non-destructively predicted with a DC voltage source and a low current ammeter, as show in figure 8c. Here the signs of breakdown about to occur are evident in the non-linear resistance measured. This type of test is not perfectly predictive, but subsequent RF tests (where the RF voltage amplitude is estimated rather than directly measured) show that RF voltage breakdown typically occurs at around 65% of the DC voltage breakdown value. As the trap array grows in size, it is reasonable to expect that breakdown due to defects in processing, contaminants on the surface, and temperature exacerbated conditions becomes more likely due to the greater volume and surface area available for it to occur. Fortunately, it is still unlikely and we have not observed a greater probability of RF breakdown for large versus small traps, so we do not anticipate this to be a dominant issue as NISQ scale traps are fabricated.

3.2. RF power dissipation

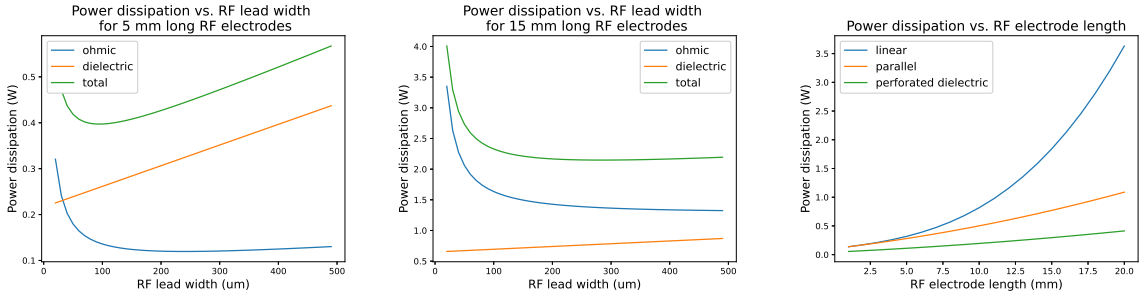
The length of the RF electrode in surface ion traps (∼1 cm) is smaller than the quarter wavelength of the RF signal being delivered (∼1 m). Because of this relative size the trap can be electrically treated as a lumped high impedance load at the end of a transmission line that delivers the RF voltage into the vacuum chamber. This load can be modelled as a two-part microstrip consisting of the trap electrodes and lead from the wirebond to the electrodes, both with distributed series resistance and inductance and parallel capacitance and conductance. At 50 MHz the skin depth in aluminum is 12 μm , so the

resistance can be calculated using the full cross-section of the aluminum electrode. The inductance and conductance can be ignored for purposes of calculating impedance but the latter is important for calculating dielectric losses.

In the following equations V is the amplitude of the applied RF voltage, $\Omega/2\pi$ is the drive frequency in Hz, C is the capacitance of the RF electrodes, R is the end-to-end resistance of the RF electrode, and $\tan\delta$ is the loss tangent of the SiO_2 between the RF electrode and ground plane. If $R \ll \frac{1}{\Omega C}$, the Thevenin equivalent circuit that accounts for its distributed nature would have resistance $R/3$ and capacitance C. The total RF current drawn by the trap is $\frac{V}{\Omega C}$, the ohmic power dissipation $P_{ohmic} = \frac{1}{6}V^2\Omega^2C^2R$, and the dielectric power dissipation $P_{dielectric} = \frac{1}{2}V^2\Omega C\tan\delta$. For standard geometries (e.g. [15]), the capacitance of a single RF electrode is 5 to 10 pF/cm of length and the resistance is $\sim 0.3\,\Omega$/cm. These estimates use an electrode width of $60\,\mu$m, a standard aluminum thickness of $2.4\,\mu$m, and a resistivity of 2.65 $\mu\Omega\cdot cm$ at room temperature. They also depend on the PE-CVD oxide between the RF electrode and ground plane; here we use a thickness of $2.4\,\mu$m under the RF electrode and $4.8\,\mu$m under the RF lead, and assume oxide with a loss tangent of 10^{-3}.

The designed RF lead width is primarily based on minimizing power dissipation. The lead must connect from the chip edge for wirebonding to the electrode and therefore its length is constrained. The RF lead uses the same metal layers as the trap so the capacitance density is similar, but the capacitance can be reduced by eliminating metal layers below the top lead, save the bottom ground layer. Both ohmic loss and dielectric loss are important considerations. In figure 9 the ohmic, dielectric, and total power dissipation is plotted for 5 mm and 15 mm long linear ion traps as a function of the lead width. Figure 9a shows a subtle minimum in the ohmic power dissipation; for very small widths the lead capacitance is low but the resistance high, and there is significant power dissipation due to the current that is delivered via the lead to the trap. For large widths the capacitance of the lead results in a significant current draw that causes growing ohmic power losses. The dielectric loss is a linear function of the capacitance and when added to the ohmic dissipation for short electrode lengths it establishes an optimal RF lead width, but for longer lengths the power is typically dominated by ohmic power losses. For small lead widths the current density of the lead can approach or exceed the electromigration limit of aluminum, conservatively assumed to be $10^5 A/cm^2$, though this is higher due to the 0.5% copper impurity in the aluminum metal layers.

Current devices operate well within the limits of electrode thickness, metal resistivity, oxide thickness, electrode length, and frequency, at least as it relates to delivering consistent RF voltage throughout the trap with manageable power dissipation. This margin will disappear for NISQ size traps if the electrode length is increased by an order of magnitude; in this case the ratio of resistance to capacitive impedance would drop by two orders of magnitude and the approximations above for power dissipation and the Thevenin equivalent circuit would no longer be valid. This would also be accompanied by a voltage drop from one end of the electrodes to the other and significantly larger power dissipations if all else were kept equal and the RF electrode



(a) (b) (c)

Figure 9: Electrical power dissipation for surface ion traps with electrode lengths of (a) 5 mm and (b) 15 mm to illustrate the relative impacts of ohmic power dissipation versus dielectric power dissipation. Power dissipation is compared in (c) for a linear RF topology (where the lead feeds a single pair of RF electrodes that wind throughout the trap), a parallel topology (where the lead fans out to multiple RF electrode sections), and a parallel topology with a perforated dielectric (0.37 fill factor) that reduces the capacitance by 46%. This fill factor is the optimal value for minimizing temperature.

was linearly meandered through the device. A much better RF delivery strategy is to use a lead that splits to serve multiple linear trap regions, as the electrode width of the lead can be optimized for the current draw, whereas a long linear trap would draw current through RF electrodes which are typically optimized for trap performance rather than power dissipation. However, especially as traps grow larger, care must be taken when splitting the lead to match the RF phase at points connected by two paths to the RF source.

Large stacks of oxide were used in early devices to reduce capacitance, with up to $10\,\mu$m oxide thickness. The cost of this approach is increased fabrication risk due to consequences of film stress. An alternative way to reduce capacitance is to partially remove underlying oxide; since SiO_2 has a dielectric constant $\epsilon_r = 3.7$, replacing it with vacuum gaps while leaving SiO_2 pillars to maintain the structural integrity of the metal layers can result in almost a $4\times$ reduction in capacitance for a low oxide fill factor. The ohmic power dissipation would drop quadratically and the dielectric power dissipation linearly with this capacitance reduction.

While related, temperature rise is not always directly proportional to power dissipation. The package is usually thermally sunk with two primary thermal pathways from the metal electrodes of the trap to the package, one through the bulk silicon of the chip (which is soldered to the package) and another through the electrodes and wirebonds to the package bond pads. At room temperature both aluminum and silicon have similar thermal conductivities between 150 and 200 $Wm^{-1}K^{-1}$, whereas silicon dioxide has a much lower thermal conductivity of 1.3 $Wm^{-1}K^{-1}$. However since the geometric pathway from the electrode to the silicon substrate has a large cross-section and small distance, and the pathway via the electrode has a small cross section and long distance, the lower resistance thermal path is through the oxide. For a trap with a 100%

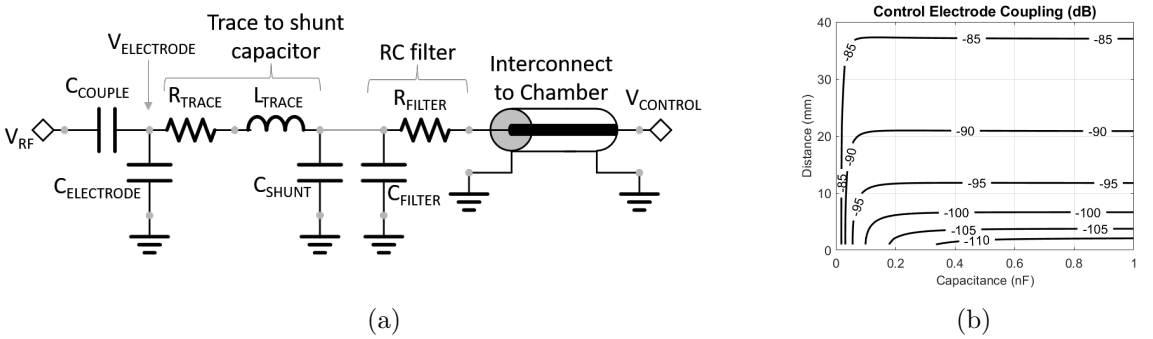
oxide fill factor beneath the RF electrode, consider power dissipation $P = \beta C^2 + \gamma C$, where the first term corresponds to ohmic power dissipation and the second to dielectric power dissipation. Using Fourier's law the temperature rise (from trap surface to the package) is $\Delta T \propto (\beta C + \gamma)/k$, where k is the thermal conductivity of the material stack. This shows that a lower capacitance achieved with thicker oxide layers reduces the temperature, even though the thermal resistance of the oxide increases (since the ohmic power dissipation decreases quadratically with a linear thermal resistance increase). The situation is more subtle for a perforated dielectric because the dielectric constant does not drop to zero by eliminating the oxide. If the oxide fill factor is α, the temperature increase on the trap is $\Delta T \propto -\left(\beta(\frac{\epsilon_\alpha A}{d})^2 + \gamma(\frac{\epsilon_r \alpha A}{d})\right)/k$, where $\epsilon_\alpha = 1 + \alpha(\epsilon_r - 1)$. For dielectric power dissipation the temperature increase does not depend on the fill factor because the power and thermal resistance both linearly depend on α. For ohmic power dissipation, an optimal fill factor of $\alpha = \frac{1}{\epsilon_r - 1}$ achieves the lowest temperature increase. Therefore the optimal fill factor for any geometry is the same as the one for the ohmic dissipation case, but the level of effectiveness will depend on the particular trap and lead geometries.

The calculations above show it is possible to fabricate NISQ scale traps with power dissipations similar to currently used devices but with up to 10× longer RF electrodes by employing both a parallel RF feed and perforating some or part of the dielectric between the RF and the ground plane. Operation at cryogenic temperatures would reduce ohmic power dissipation further by reducing the resistivity of the aluminum RF electrode by about 15× (limited by alloying Al and Cu).

3.3. Control electrodes

Surface traps have small but non-negligible parasitic capacitance between the RF and control electrodes and use shunt capacitors to limit RF pickup that would otherwise cause uncompensatable micromotion and other unpredictable behavior. The equivalent circuit of a typical control electrode is shown in figure 10a. We use typical values of the electrode capacitance to ground ($C_{ELECTRODE} \sim 50$ fF) and coupling capacitance to the RF electrode ($C_{COUPLE} \sim 1$ fF). The control voltage ($V_{CONTROL}$) is supplied from an external supply through a ∼1 meter-long cable. An added shunt capacitance ($C_{SHUNT} \sim 1$ nF) provides a low-impedance shunt path for any coupled RF voltage, and is connected by a trace with length-dependent resistance (R_{TRACE}) and inductance (L_{TRACE}). Finally, RC filtering (R_{FILTER}, C_{FILTER}) may also be used to reduce the injection of noise from external sources. While C_{FILTER} is shown adjacent to C_{SHUNT} it is generally physically located outside of the vacuum chamber, with control wires separating the two.

The location and the sizing of the shunt capacitance is critical for minimizing the RF voltage induced on the control electrode. If the shunt capacitor is too small or not included, the length of the connecting cable is too long to effectively shunt the RF signal, so the RF voltage induced on the control electrode could be as high as 2% of the RF voltage in the case of a 1 fF coupling capacitance and a 50 fF electrode capacitance;



(a) (b)

Figure 10: (a) Equivalent circuit of the control electrode considering trace resistance and inductance to the shunt capacitor. (b) shows the RF suppression on the control electrode vs the shunt capacitance and the length of the trace between the electrode and the shunt capacitor.

this RF voltage is on the same order as the control signal. Shunt capacitances also are constrained from above due to the area they consume and potentially excessive filtering and power draw of the control signals.

The shunt capacitor may either be an off-chip ceramic capacitor or an integrated on-chip capacitor, like a trench or metal-insulator-metal capacitor. Typical values are in the 0.1-1 nF range, but it is preferable to locate the capacitor close to the electrode because any trace resistance or inductance degrades the RF suppression provided by the capacitor. Figure 10b shows the RF suppression provided for capacitances with values of 0 to 1 nF, located at distances up to 50 mm from the control electrode. As an example, if a 1 nF capacitor is located off-chip and 10 mm away from the electrode, the trace resistance and inductance dominates the shunt impedance and degrades the RF suppression from 120 dB to <100 dB. In fact, similar performance can be realized with a 0.1 nF capacitor. To fully realize the benefit of large capacitors for RF suppression, they must be located as close as possible to the control electrode, which can be achieved with trench capacitors that are co-fabricated on the same chip. Higher lead congestion in NISQ devices will reduce the cross-sectional area and increase the length of leads, exacerbating both the resistance and inductance, and it may be important to put the trench caps not just on the trap die but much closer to the electrodes.

3.4. Built-in diagnostic elements

Diagnostic tools for measuring the on-chip temperature and RF amplitude [15] become more valuable as the trap array becomes larger and operates closer to performance bounds. Typical off-the-shelf thermistor devices have resistances on the order of kΩ's, which can be incorporated into the trap for reasonable size traces. For example, a thin aluminum trace that wraps around the perimeter of the device would have ∼1.5 kΩ resistance and is found to be accurate for measurements down to ∼30 K. In addition to verifying RF coupling to the trap based on the temperature increase, these probes are useful in cryogenic regimes where they can be calibrated as the cryostat cools down and

then used to measure the increase in temperature as the RF power is applied. Aluminum suffers from a relatively low electromigration limit and cannot exceed current densities of about 1 $\mathrm{mA}/\mu\mathrm{m}^2$, so a tungsten trace is preferred as an on-chip heating element capable of dissipating around 1 W of power. These are useful in cryogenic experiments for warming the trap temperature above its environment as the apparatus cools down, preventing outgassing contaminants from condensing on the trap.

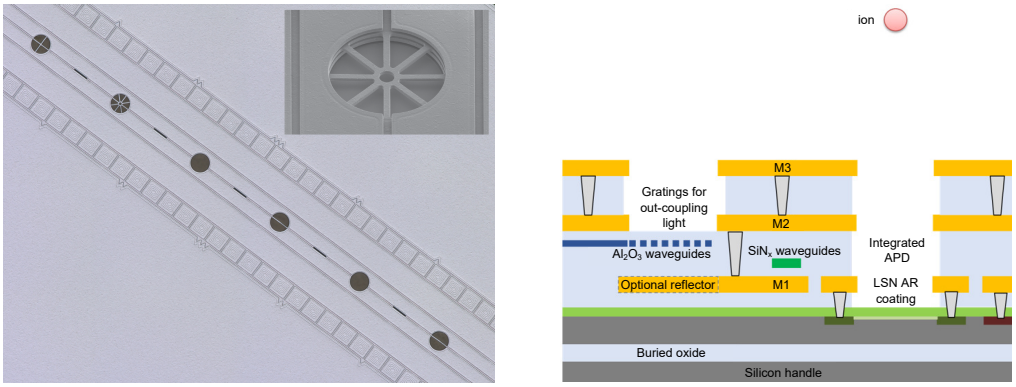
An RF pickup consisting of a capacitively coupled trace near the RF electrode, ideally opposite the launch side, can be used to estimate the RF voltage coupled to the trap. This is valuable both in the early parts of an experiment to estimate the voltage and during the experiment as a feedback signal for stabilizing the RF power. While this would be beneficial for a small ion trap as well as a large one, the more stringent performance requirements on radial mode stability needed to meet fidelity targets would make it especially useful for a NISQ scale device.

4. Future advances for hybrid MEMS-CMOS ion traps

While the preceding sections focused on advances needed to fabricate NISQ ion trap arrays, monolithic MEMS-CMOS integration renders a platform that can also support the added technical functionality that will be necessary for late- or post-NISQ systems. Advanced CMOS processing allows integration of active elements like single-photon detectors [41], waveguides [13], modulators [21], digital-to-analog converters [14] for electrode voltage control, and passive elements such as RF shunt capacitors [29], resistors [15], and RF capacitive pick-up sensors for RF stabilization.

As an example, we have employed hybrid MEMS-CMOS techniques to incorporate single photon avalanche photodiodes (SPADs) directly below trapping locations. SPADs are an alternative to other detectors that can be integrated and microfabricated, most notably superconducting nanowire single photon detectors (SNSPDs). SNSPDs have been demonstrated with excellent quantum efficiency and low dark counts in an ion trap [42], but face challenges with RF pickup and restrictive cryogenic operating requirements. SPADs have different but still critical challenges related to achieving fast high fidelity state detection, notably quantum efficiency and dark count rate. In recent research, a quantum efficiency of 24% and dark count rates as low as 1.2 kHz were measured. The optimal choice for integrated detectors may ultimately depend on the ion species used and the device temperature, and research on both of these integrated detector options will be useful for identifying relevant tradeoffs. Figure 11 shows these SPADs as well as a schematic of them alongside UV and visible waveguides and output grating couplers. In addition to monolithic integration of active and passive elements, heterogeneous integration techniques can interface other optical (fiber or diffractive optics), electrical (RF resonators, inductors), or thermal (heaters or cryogenic coolers) components to the trap.

NISQ-scale ion traps that can perform quantum computations or simulations on tens of ions will require new structures to minimize RF power dissipation and deliver



(a) (b)

Figure 11: (a) SEM image of SPADs integrated with a trap. Four of the locations have grids in metal 2 consisting of one, two, or four bars across the opening above the SPADs to screen the ion from voltages associated with the SPAD. (b) Schematic image of both SPADs and waveguides on the same device.

high fidelity electrical and optical signals to a 2D array of ions. These and other necessary advances will produce ion traps capable of supporting larger algorithms as well as providing insight into the challenges that will be encountered in the following stages of scaling. Even architectural trade-offs, such as using remote entanglement versus shuttling, may be influenced by the success or failure of managing RF power dissipation, delivering control signals, and achieving other performance requirements on NISQ-scale traps that are fabricated over the next few years. While many issues will be exacerbated by larger trap scales, employing some of the emerging technologies that have recently been successful at the small scale may provide paths to solving them.

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