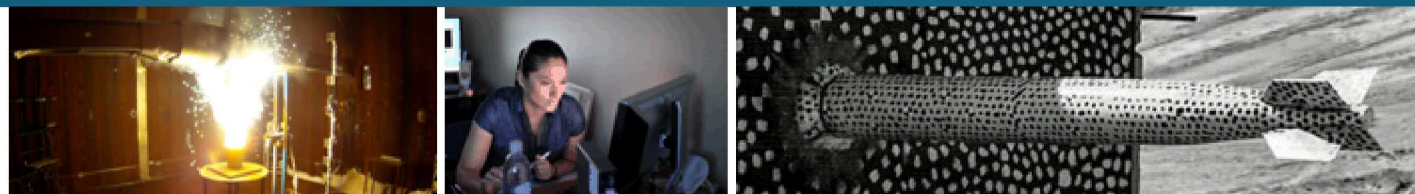


VTO/MOSFET Process Updates



PRESENTED BY

Caleb E Glaser – NSME PhD Student



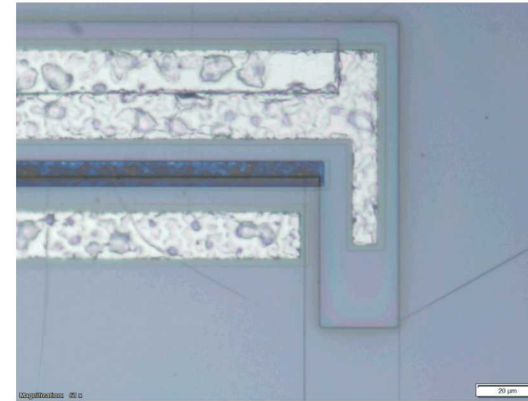
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Outline

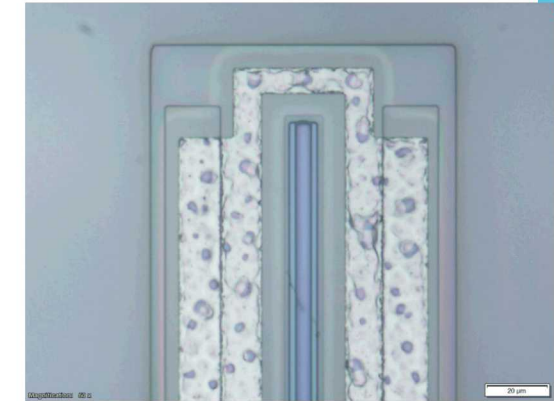
- Gate dielectric wet etch issues
- Gate metal sidewall coverage and liftoff
- GaICP microdots
- Next steps

3 Gate dielectric etch

- Problems with etch
 - Massive undercut of PR mask when in BOE 6:1
 - Difficult to determine when etch is complete
- Solutions
 - Find HF concentration to give 30-70 nm/min etch for SiO₂
 - Determine etch rate of other dielectrics in process



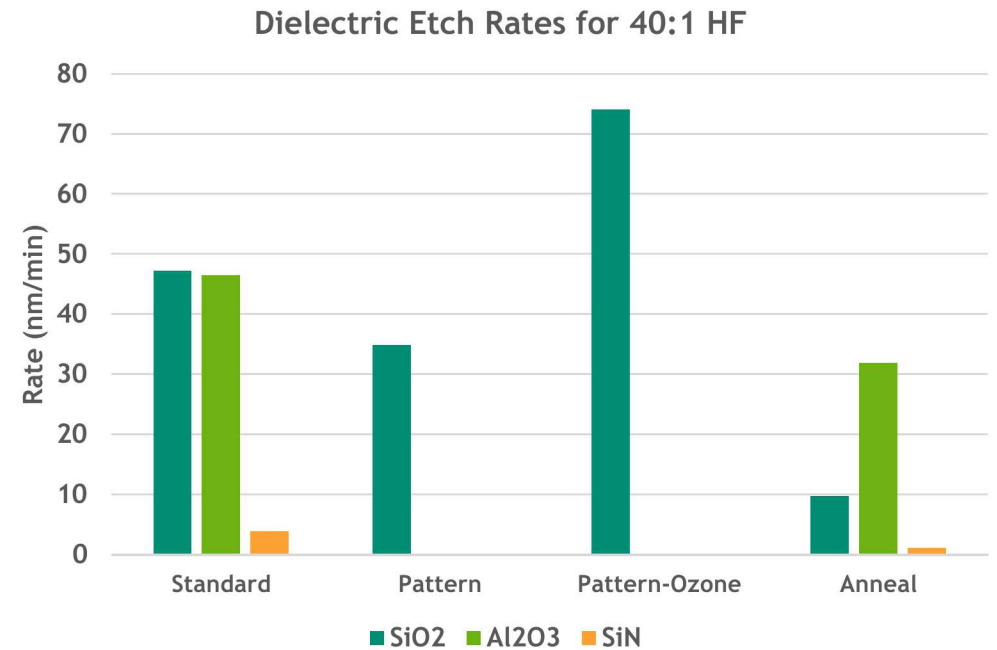
Incomplete etch



Completed etch with severe undercut

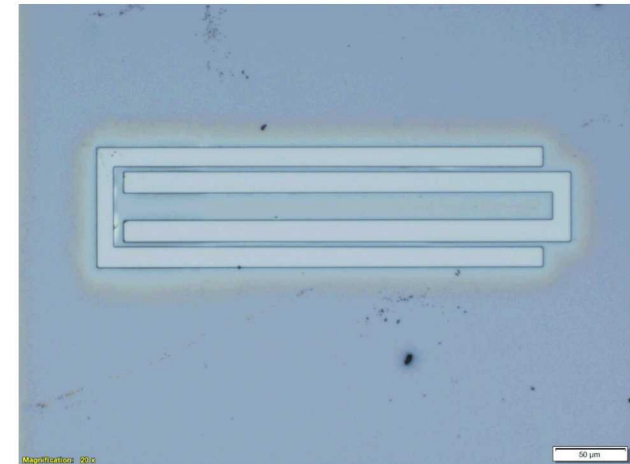
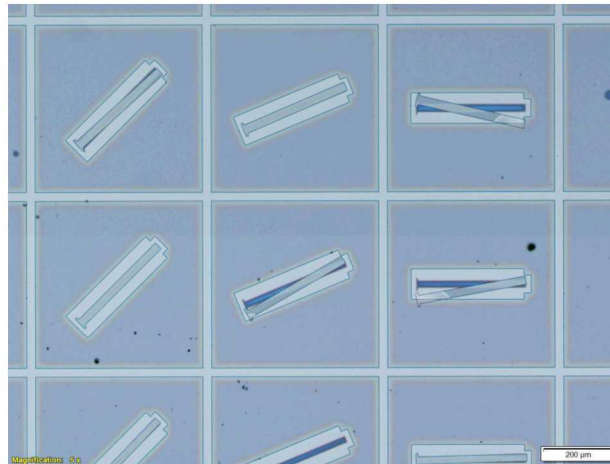
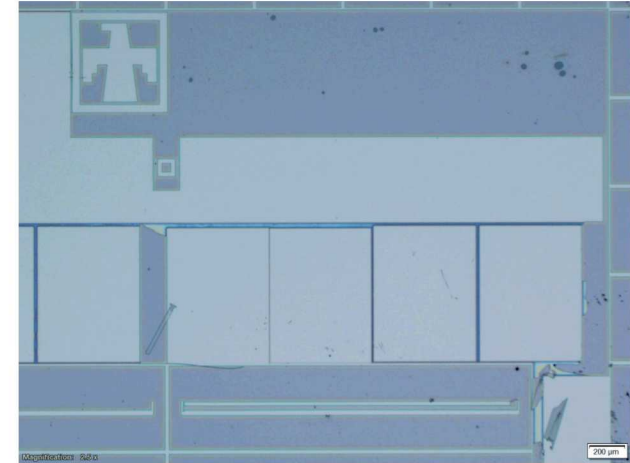
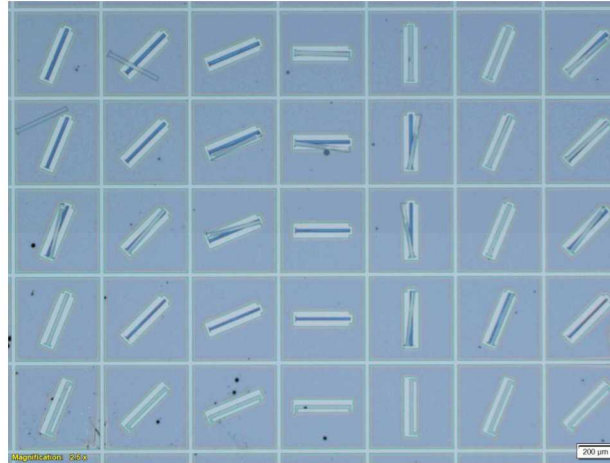
40:1 HF Raw Data (nm/min)

	SiO ₂	Al ₂ O ₃	SiN
Standard	47.2	46.5	3.9
Pattern	34.9	-	-
Pattern-Ozone	74.1	-	-
Anneal	9.8	31.9	1.1



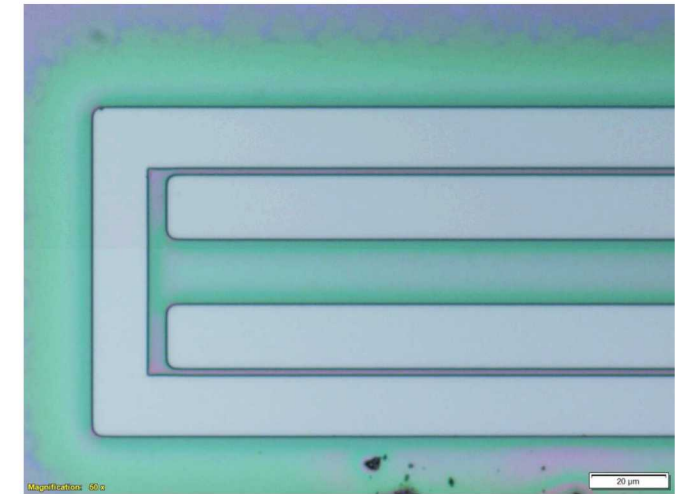
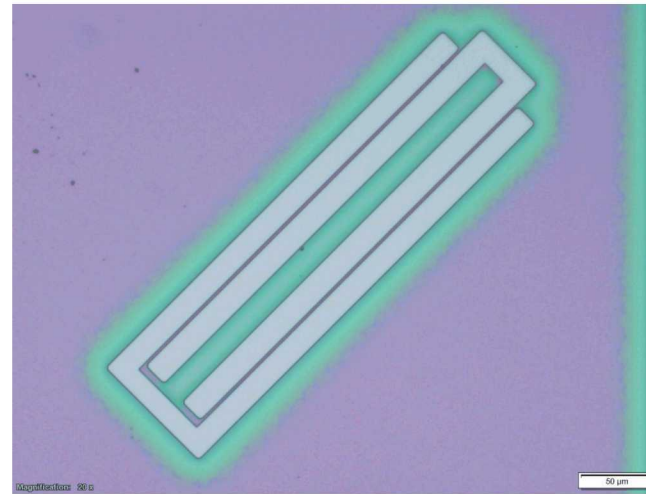
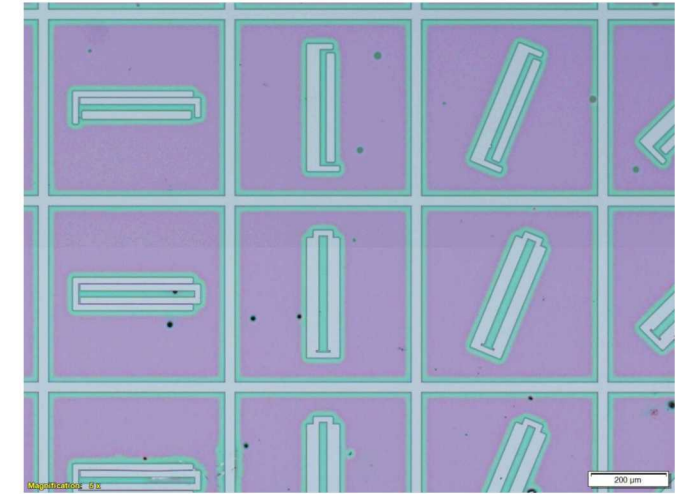
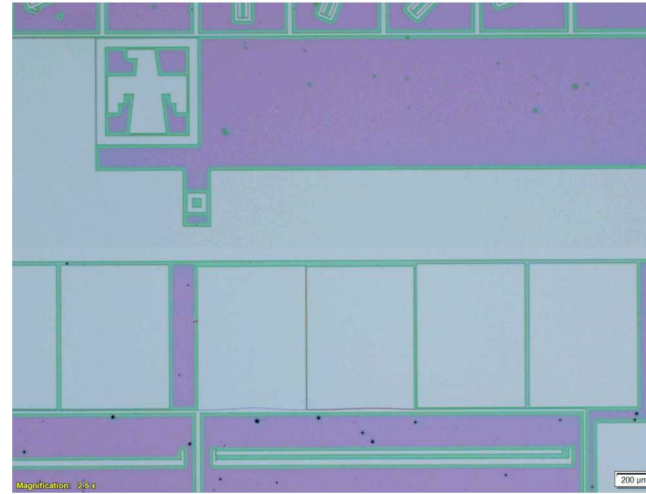
4 Patterned SiO₂ etch

- 200 nm of SiO₂ removed with 40:1 HF
- Liftoff and loss of mask to fully etch
- Undercut when SiO₂ is fully etched



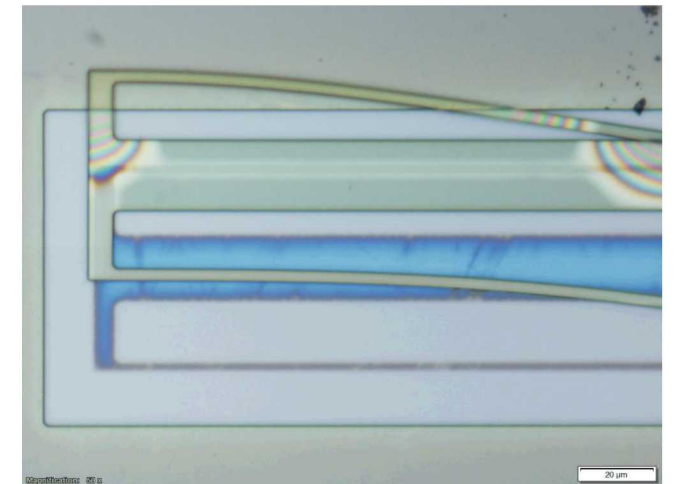
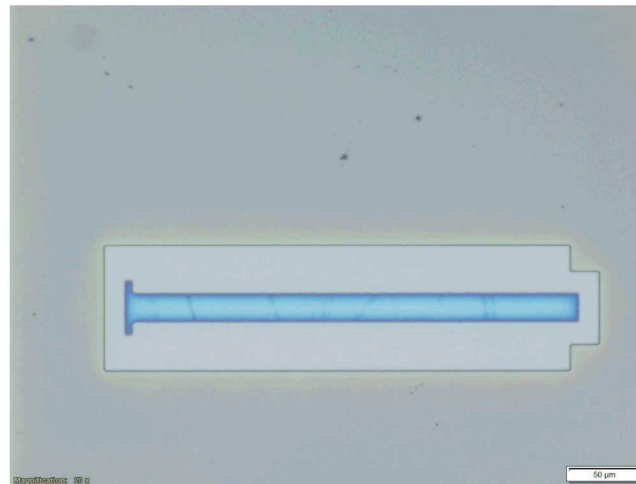
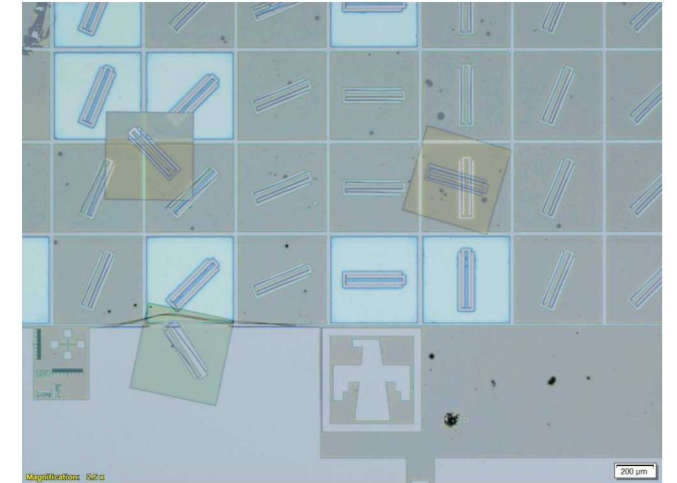
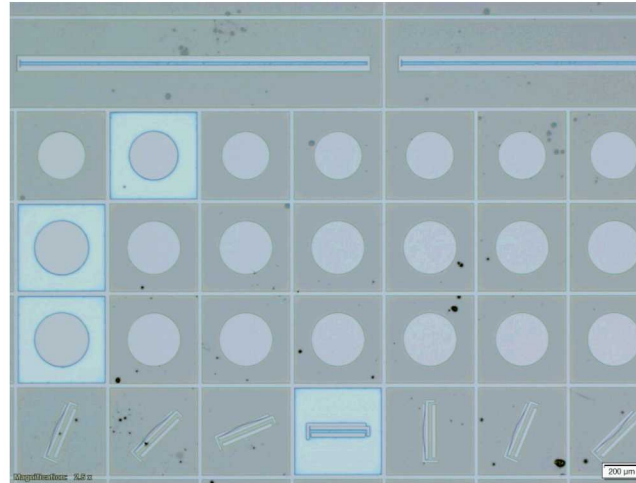
Patterned SiO₂ – 1 min O₂ Ash

- 200 nm of SiO₂ removed with 40:1 HF
- Add 1 min O₂ plasma Ash before etch
- Significant undercut
 - No pattern loss from etch



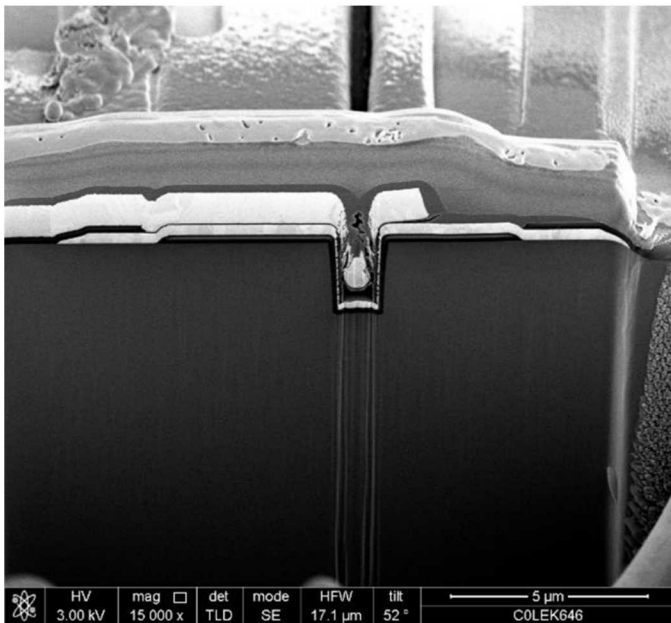
Patterned SiO₂ – 30 min Ozone

- 200 nm of SiO₂ removed with 40:1 HF
- 30 min chamber condition followed by 30 min ozone
 - Ozone after PR pattern
 - 1 min ASH after ozone treatment
- Sample cleared at 2.5 min
 - Undercut and total pattern loss
 - 30 min ozone appears too long
 - Vapor HF tool or ozone prior to patterning

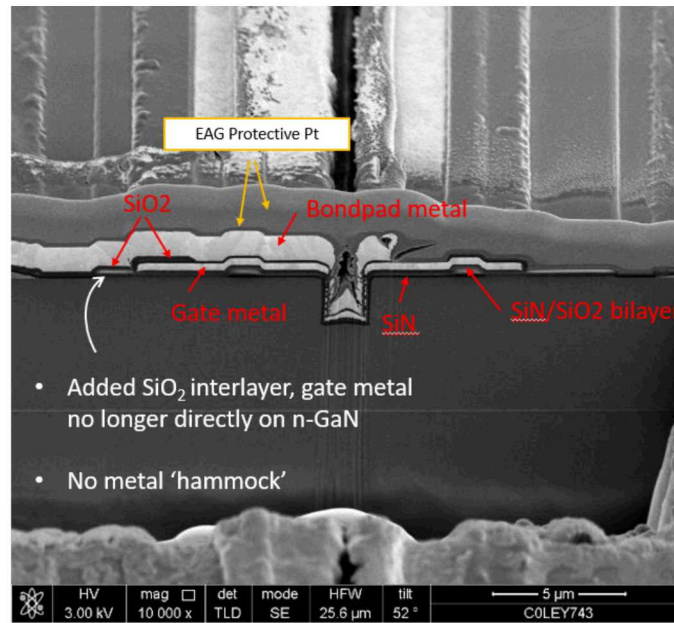


7 Gate metal sidewall coverage

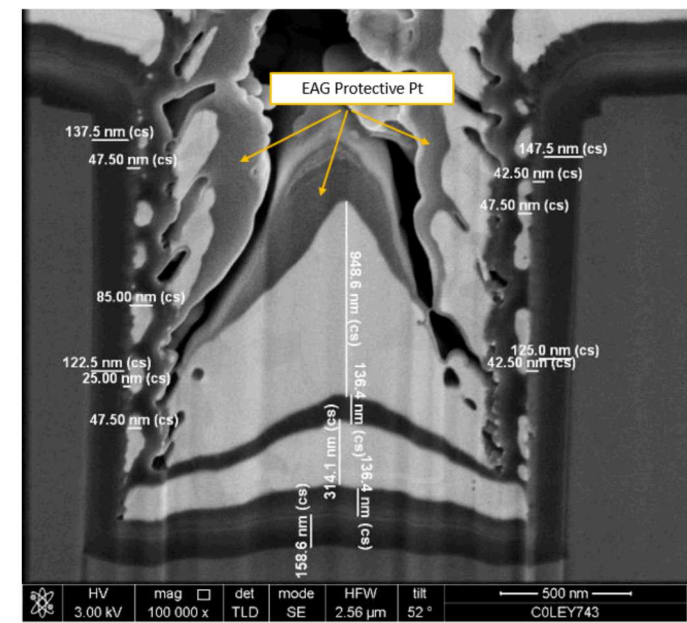
- Gate metal in trench
 - Increased Ti adhesion layer (10-100 nm) to improve sidewall coverage
 - Variable angle evaporation at 14°
- Previous process used high speed planetary and suffered from hammock effect
- Voids in sidewalls with poor Au adhesion
 - Gate metal - Ti-100 nm / Au-250 nm
 - Bondpad metal - Ti-100 nm / Au-1000 nm



Previous lot with hammock effect



Increased Ti to eliminate hammock

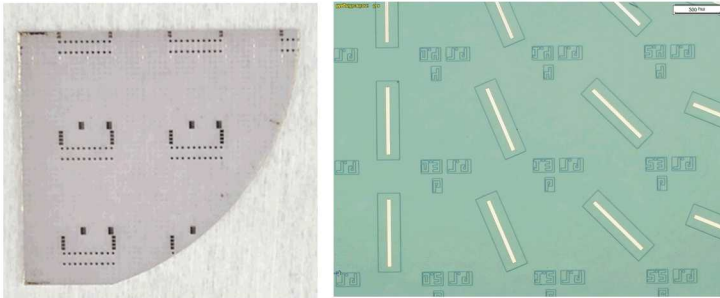


Voids in metal from Au adhesion

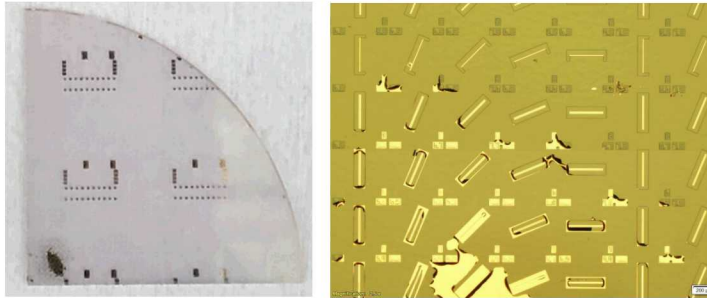
Gate metal PR mask selection

- Determine best resist for gate metal
 - 2020 - negative resist ~ 2.2 μm thick
 - 2035 - negative resist ~ 3.5 μm thick
 - 5214 - image reversal ~ 1.5 μm thick

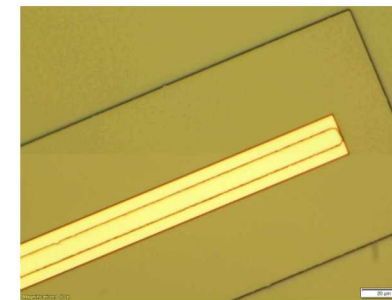
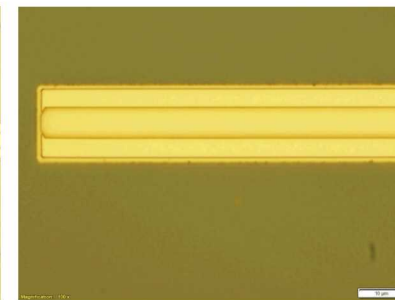
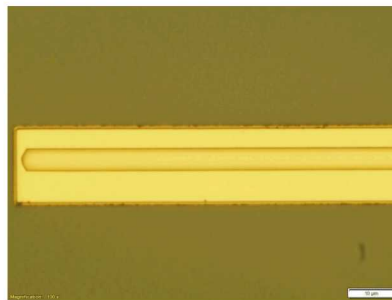
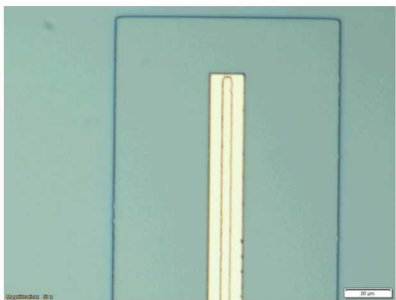
2020



2035

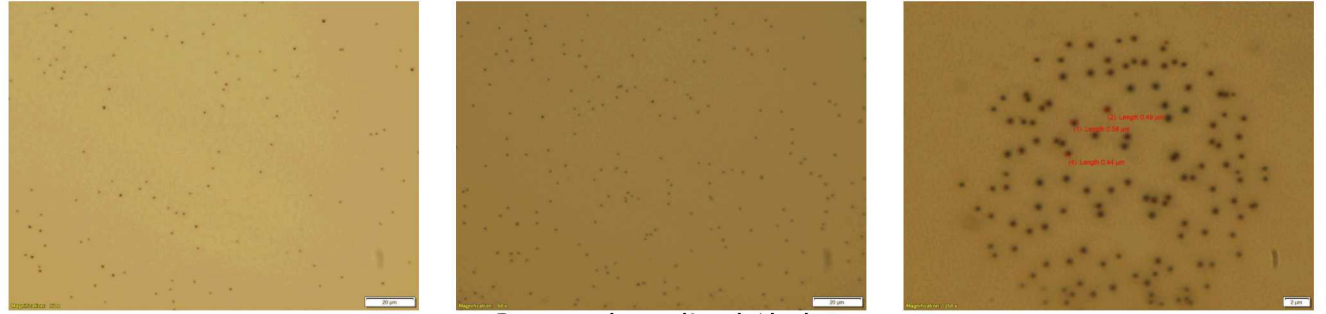


5214

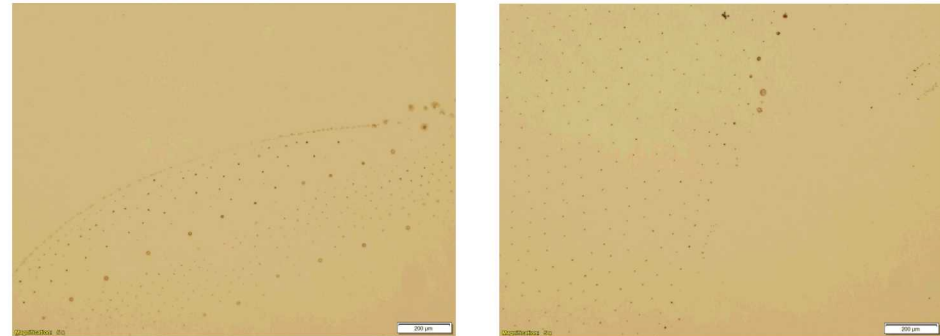


9 Microdots after GaICP trench etch

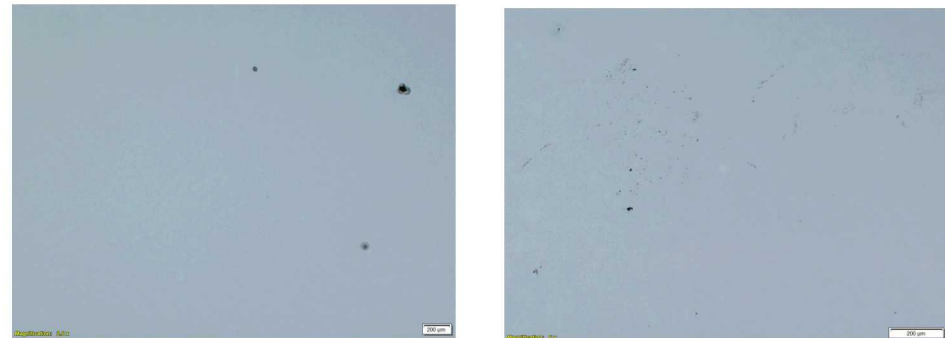
- Microdots appear on sample after 2 um trench etch
- Compare loading conditions to eliminate
 - Recessed anodized Al platen
 - Sample mounted on Si wafer
 - Sample mounted on sapphire



Recessed anodized Al platen



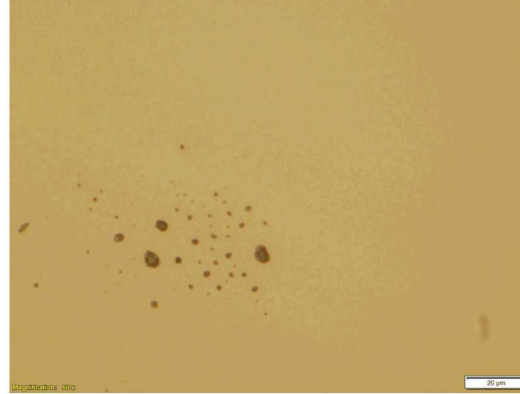
Si carrier wafer



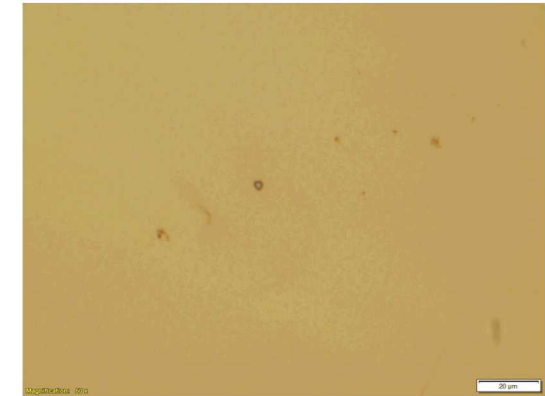
Sapphire carrier wafer

Microdots cont.

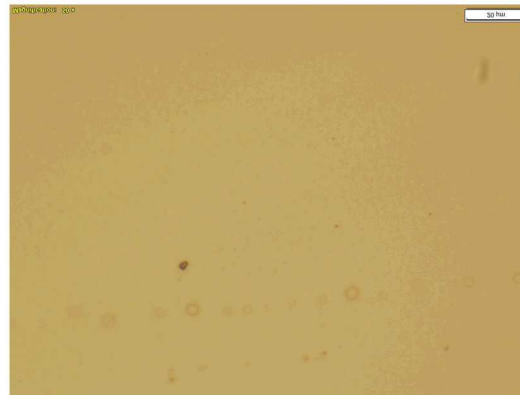
- Wet methods to remove microdots post etch
 - H_3PO_4
 - Acetone, Methanol, IPA
 - IPA with swab



Recessed post 5 min H_3PO_4



Recessed post 15 min H_3PO_4



Recessed post AMI clean



Sapphire mounted post IPA swab

Summary of semester work

- Determined 40:1 (DI:HF) best dilution for SiO₂ gate etch
 - Still need to find best method for ozone surface treatment
- Variable angle metal evaporation fixture at 14° best for conformal trench coverage
 - Voids from Au adhesion still an issue
- Evaluated several resists for gate metal pattern liftoff
 - Time for liftoff needs addressed
 - Thicker resists require longer soak time for liftoff
- Trench etch microdots and contamination
 - Cleaning methods including IPA swabs slightly improve

Next Steps

- Determine selectivity of PR mask
 - Calibrate other resists
- Find best way to determine when dielectric fully removed
 - Measured with Nanospec Reflectometer
- Understand trench microdot issue and how to mitigate
 - IPA swab
- Gate metal quick lot
 - Compare VAP, HSP, and sputtering
 - VAP with slower deposition rate
- Literature review for buried p-GaN activation
- Begin training for probe testing of completed devices



HSP fixture for metal evaporation



VAP fixture for metal evaporation