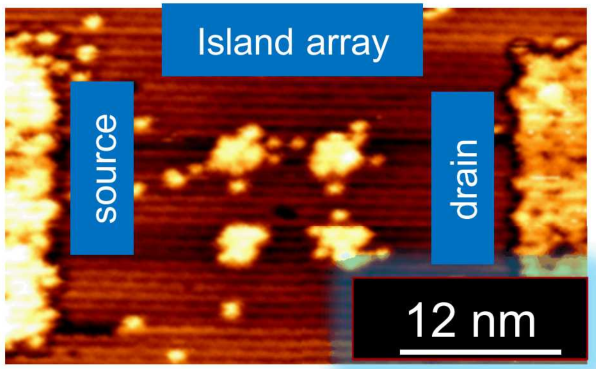
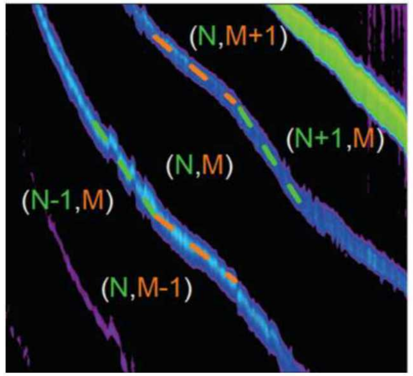
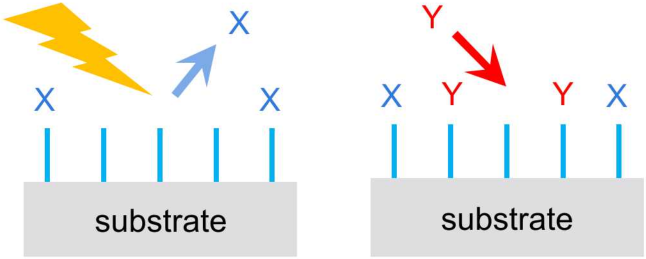
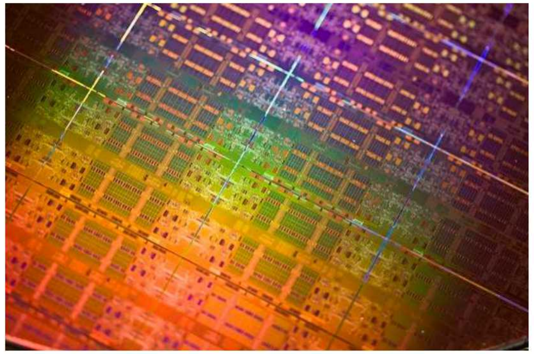
SAND2020-5187PE









Digital electronics at the atomic scale

Shashank Misra

U.S. DEPARTMENT OF ENERGY
NNSA National Nuclear Security Administration

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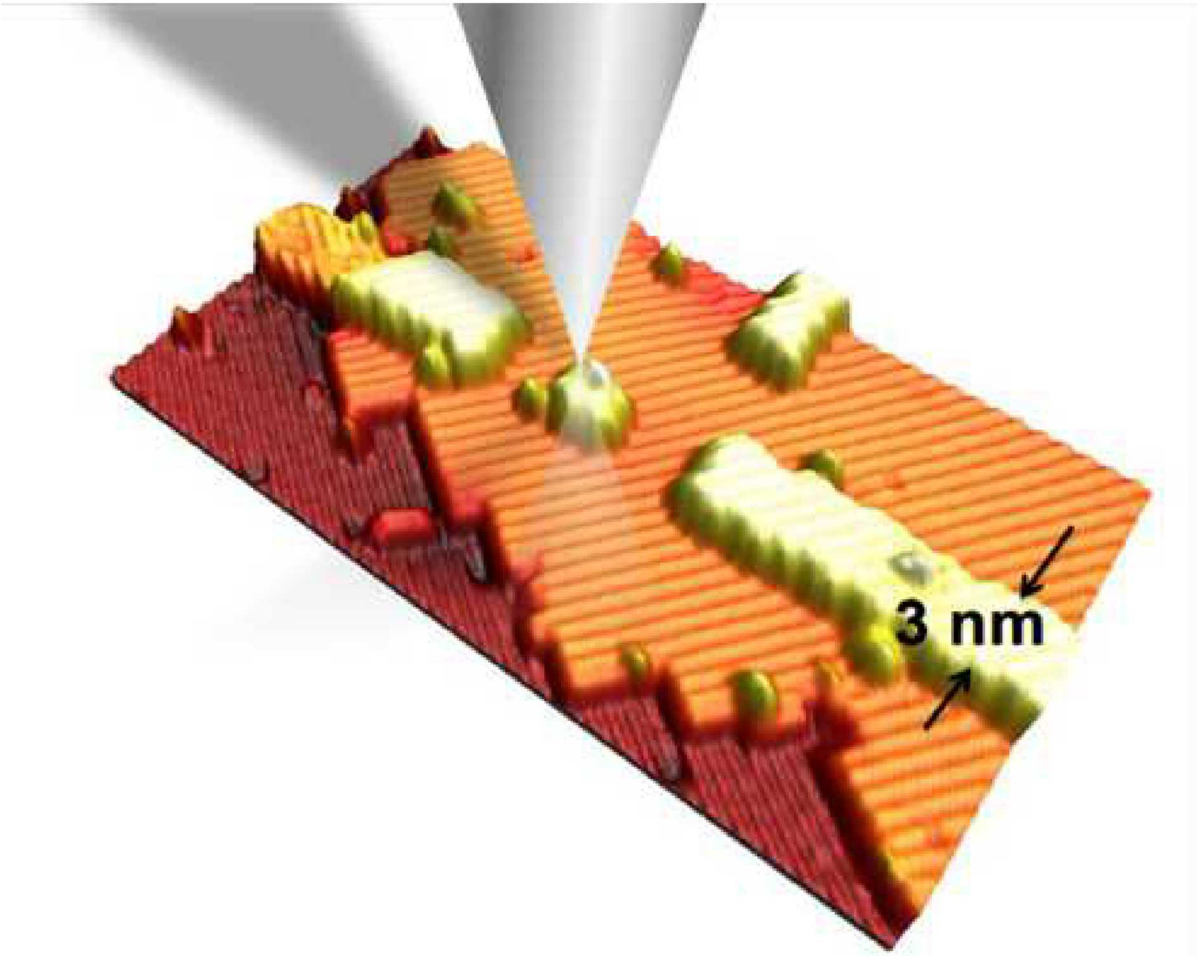
Atomic Precision Advanced Manufacturing



Assess the opportunities presented by having atomic-scale control over devices and processing for the digital microelectronics of the future

Where is microelectronics headed?

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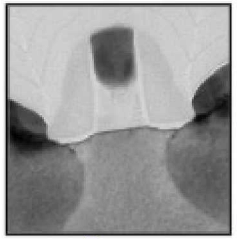
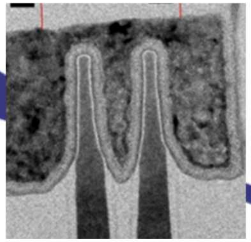
Historically, shrink transistor → more functionality and declining cost



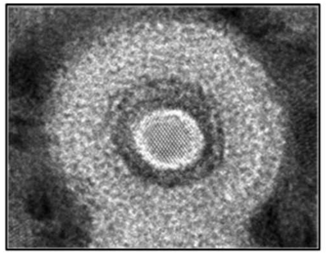
65 nm



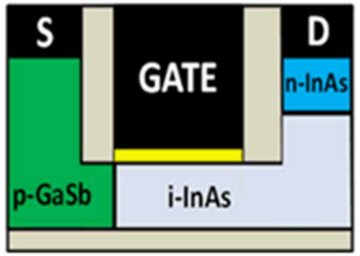
10 nm

5-7 nm

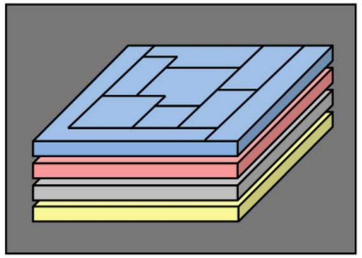
Unclear technology path.



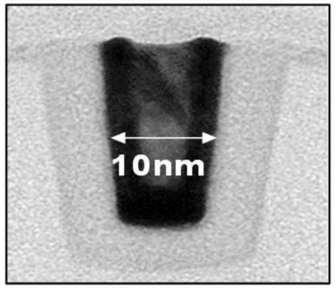
Nanowire Transistors



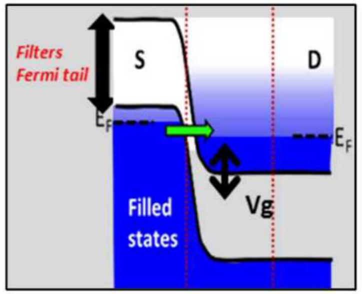
III-V Transistors



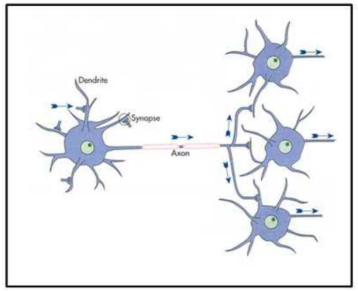
3D Stacking



Dense Interconnects

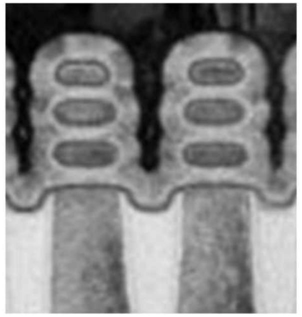


Tunnel FETs



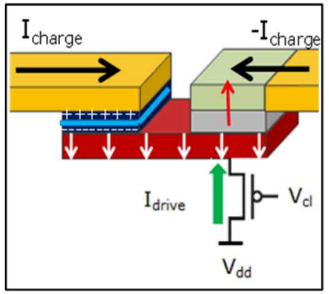
Neuromorphic Computing

Mark Bohr, Intel 2018

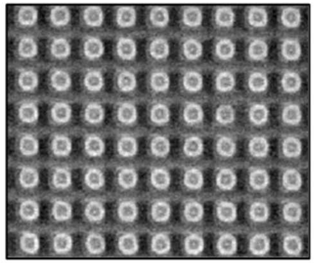


Nanosheets

Huiming Bu, IBM 2017



Spintronics



Dense Memory

Emerging risk in manufacturing-driven ecosystem

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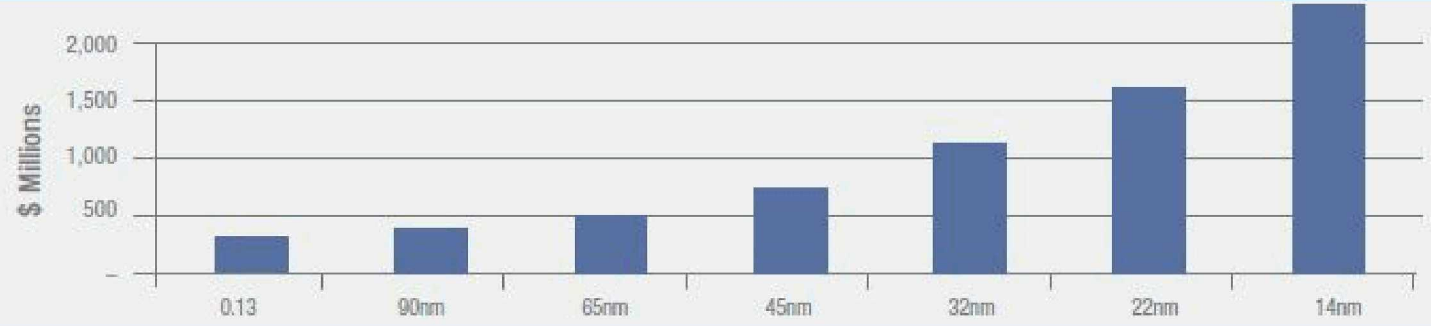
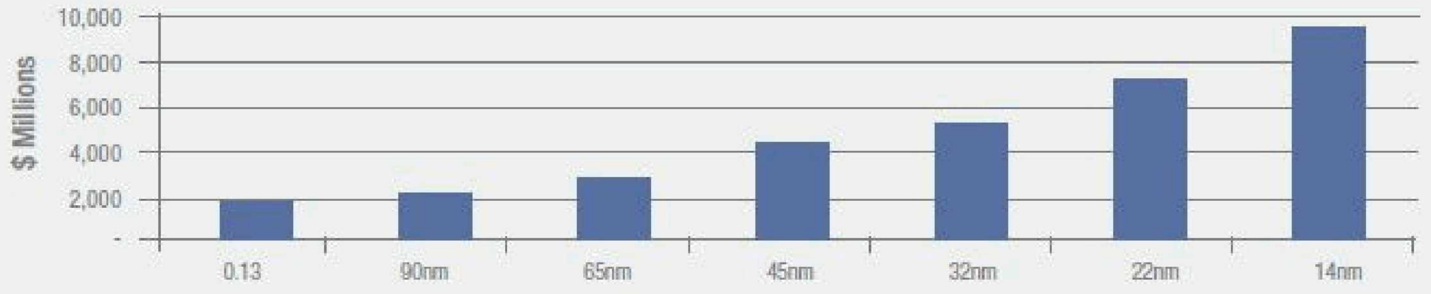
Process technology development cost by node



Fab costs by node



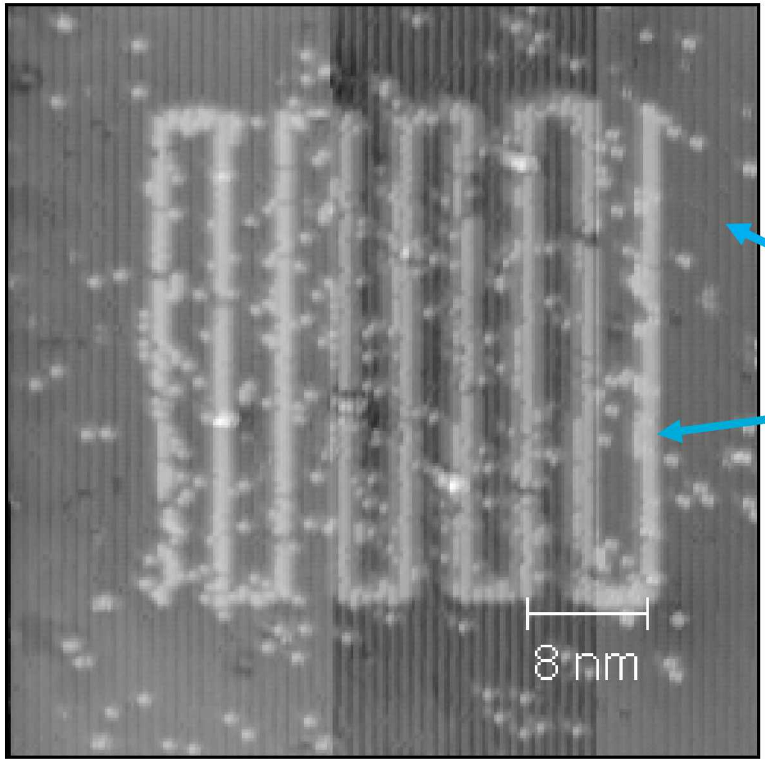
Source: Common Platform & AlixPartners Analysis

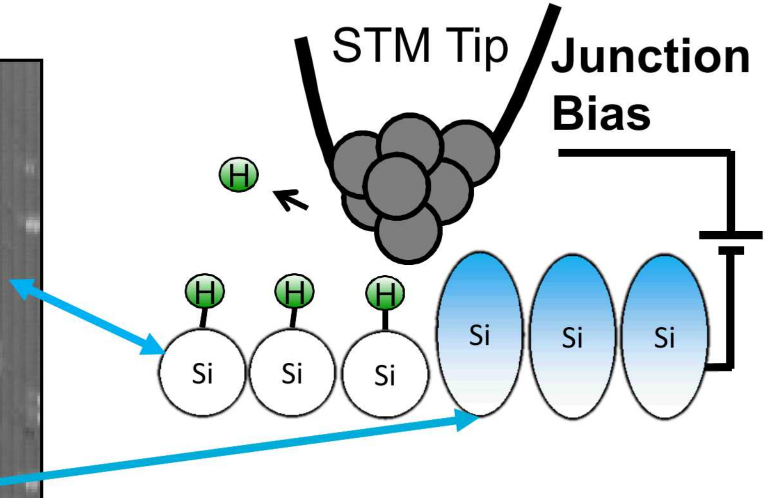
Ask what opportunities exist given atomic-scale control

How does Atomic Precision Advanced Manufacturing (APAM) work?

"Chemical contrast" at Si surface

- Unterminated Si: 1 reactive bond/ atom
- H-terminated Si: unreactive

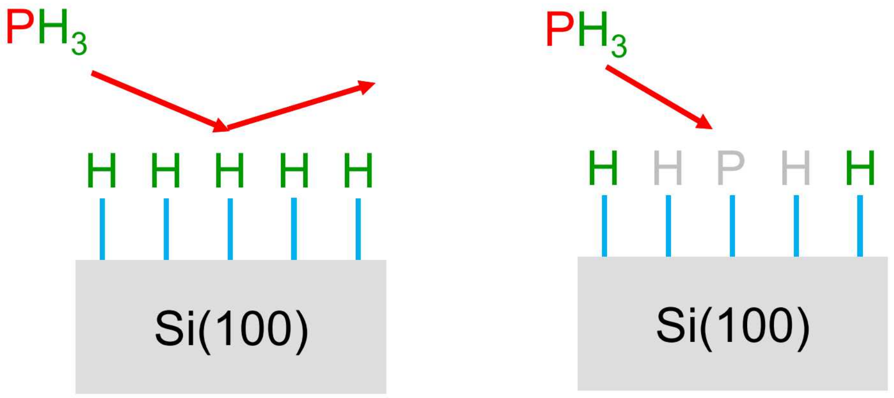




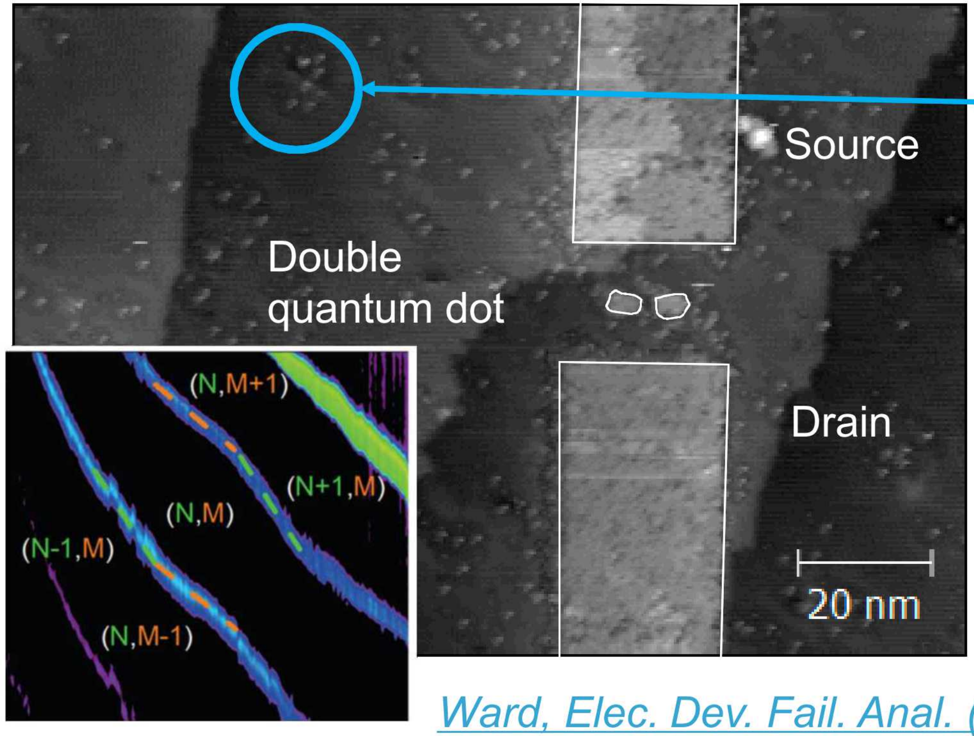
Scanning tunneling microscope (STM) can image and pattern the surface

Area-selective chemistry with phosphine

Phosphorus ‘donates’ an electron to silicon.



‘Artificial molecule’



Chemical error correction : need 3 open sites for phosphine

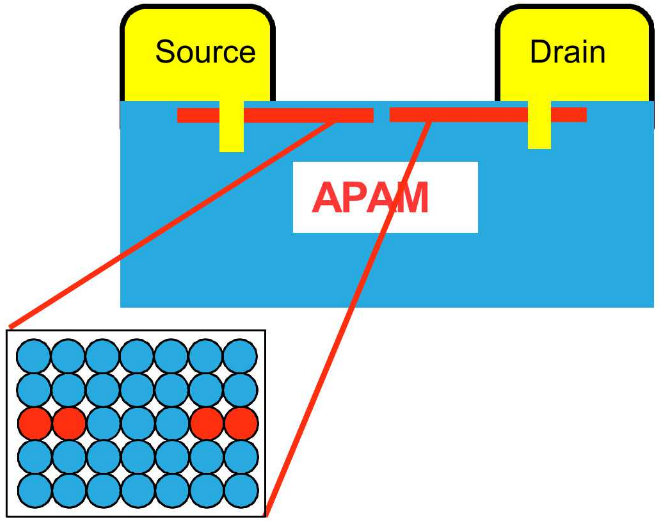
Ward, Elec. Dev. Fail. Anal. (2020)

Opportunities outside of quantum demonstrations

Opportunities outside of atomic-scale widgets

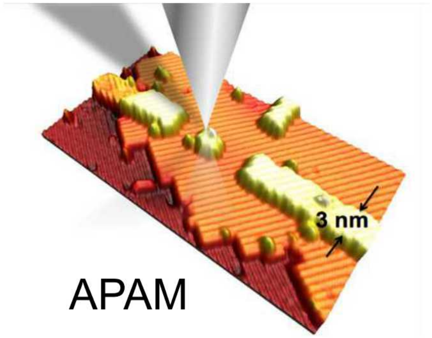
How to get to digital electronics at the atomic scale?

1. APAM devices



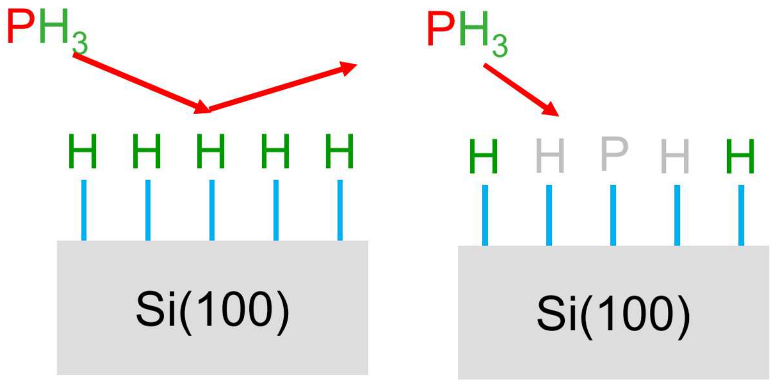
- Simple planar devices
- Only work at cryogenic temp.

2. CMOS integration



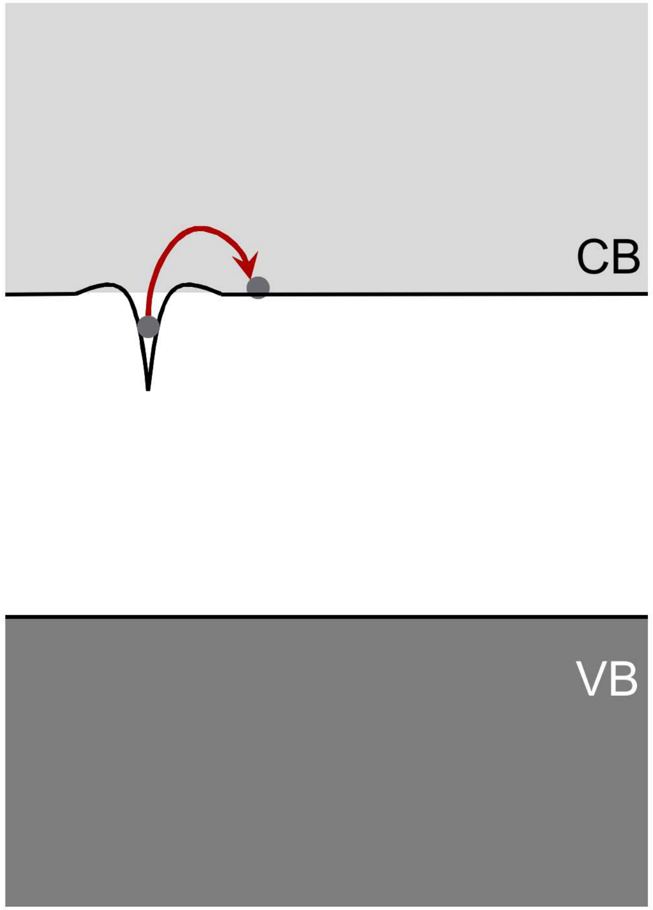
- Incompatible with CMOS workflows / parts

3. APAM toolkit

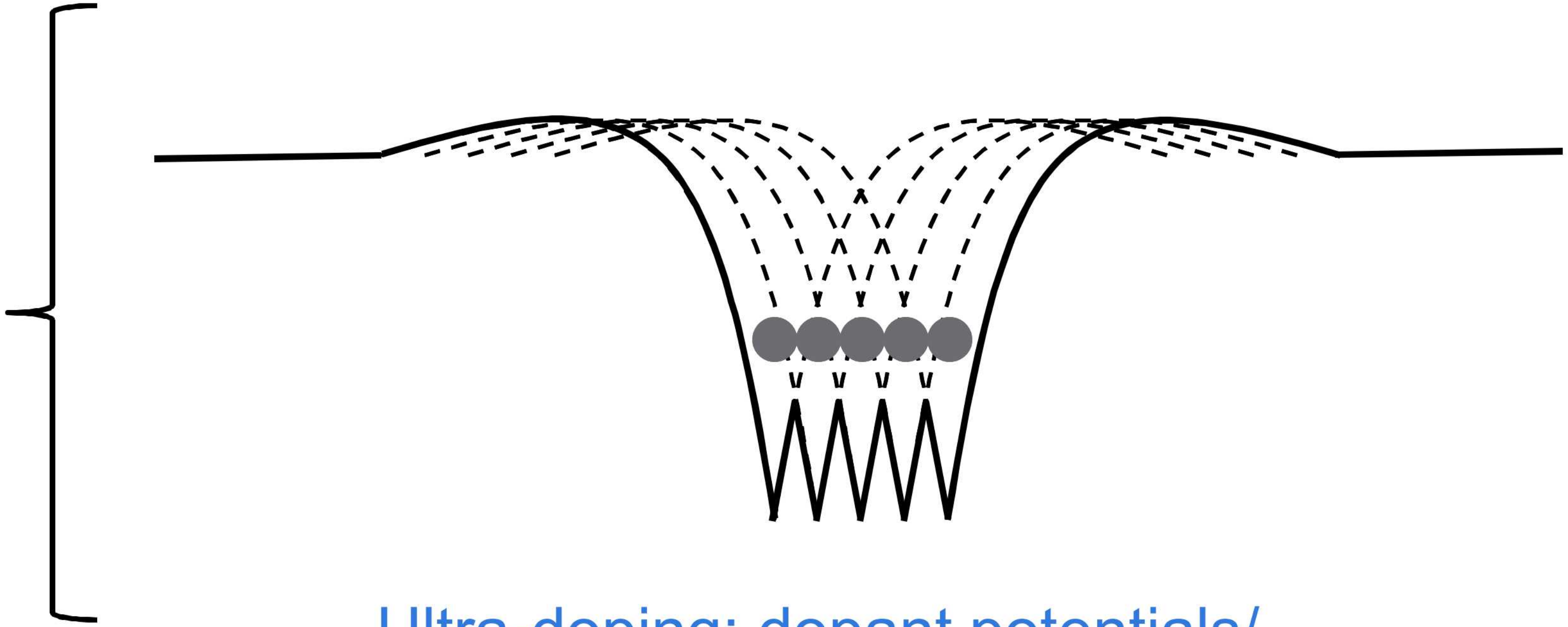


- One working chemistry

What does APAM do that's special? "Ultra-doping"



Normal doping



Ultra-doping: dopant potentials/ wavefunctions overlap significantly

APAM doping: 1 in 4 surface sites is a donor
Exceeds solid solubility for P in Si by 10x

Consequences: confinement

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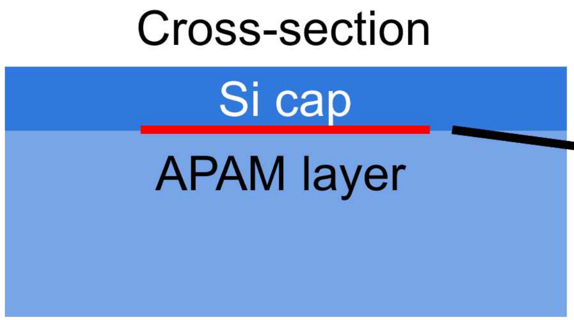
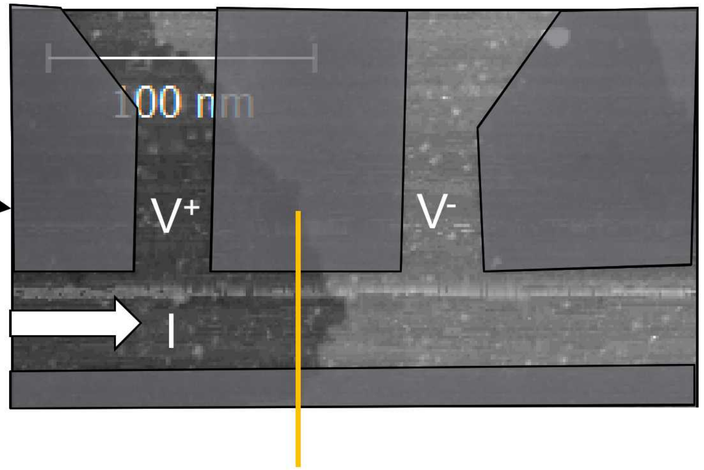
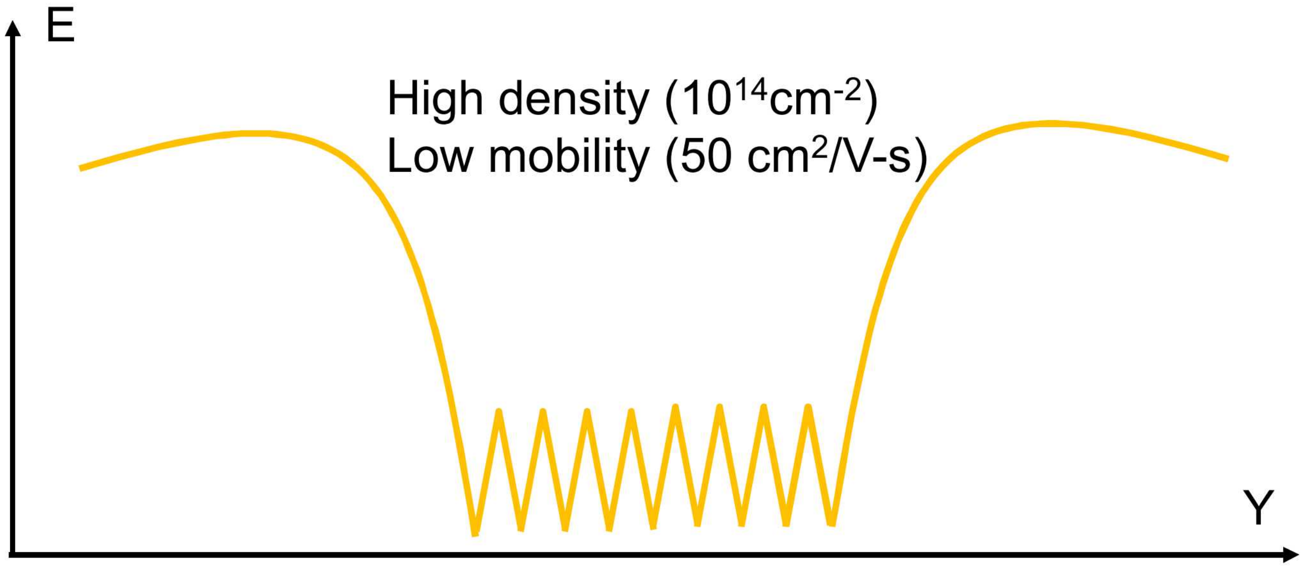
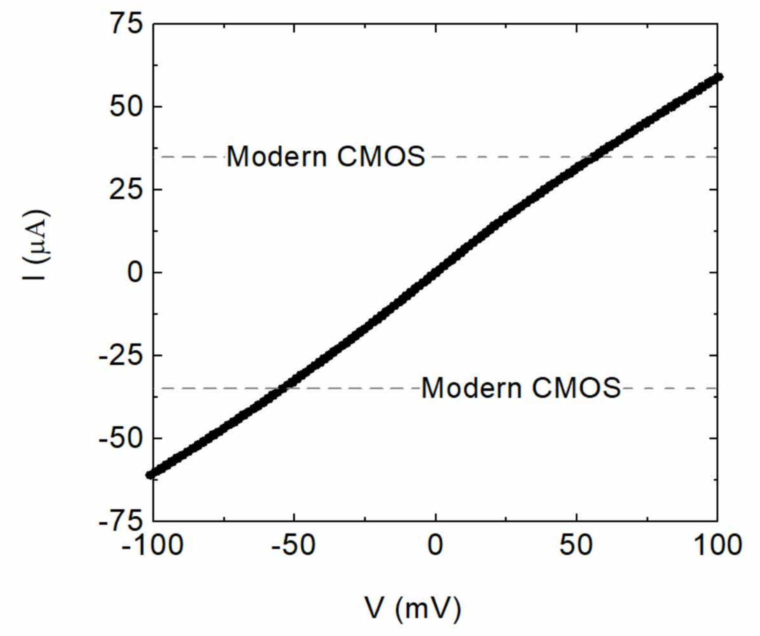




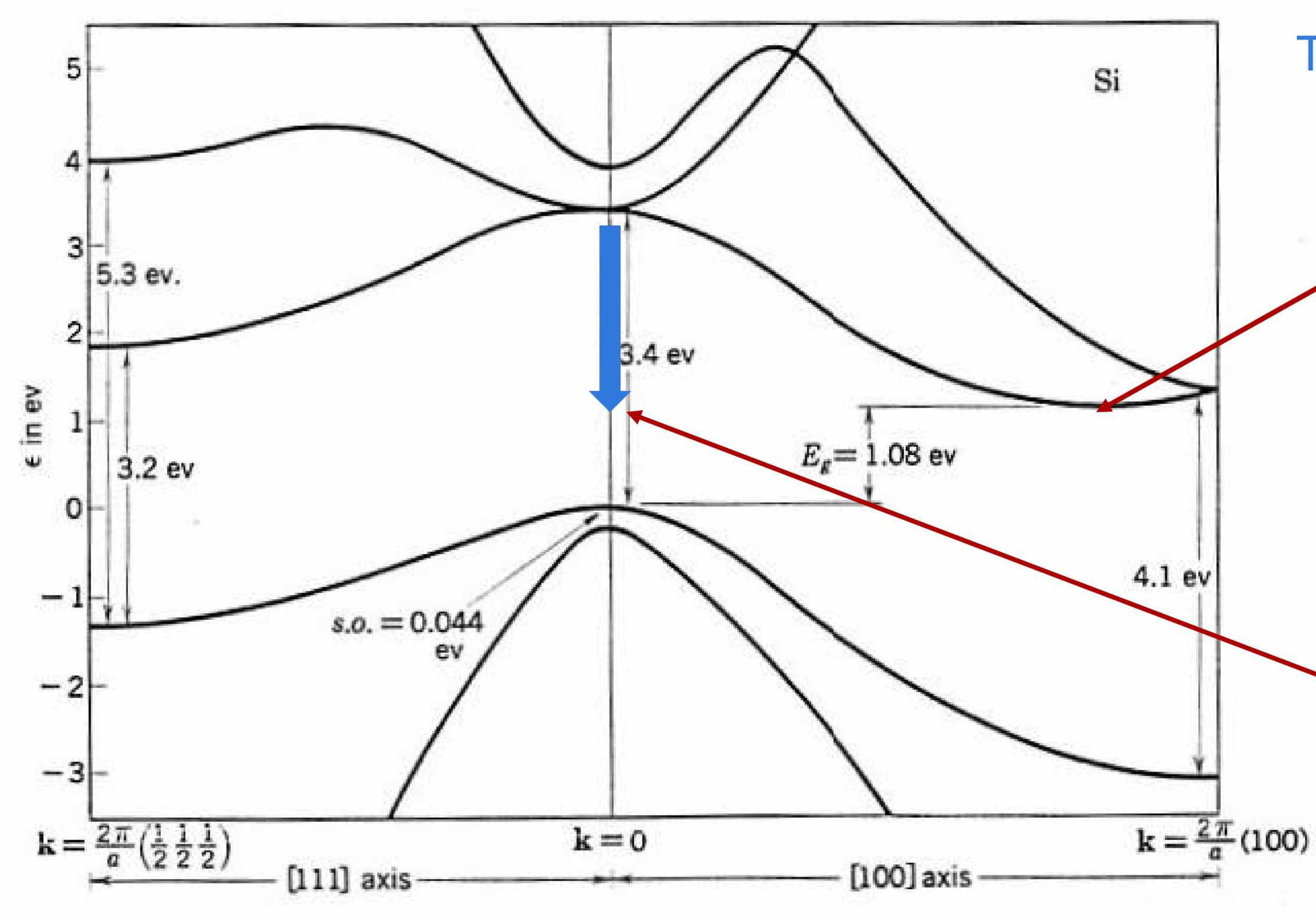


Ward, Elec. Dev. Fail. Anal. (2020)

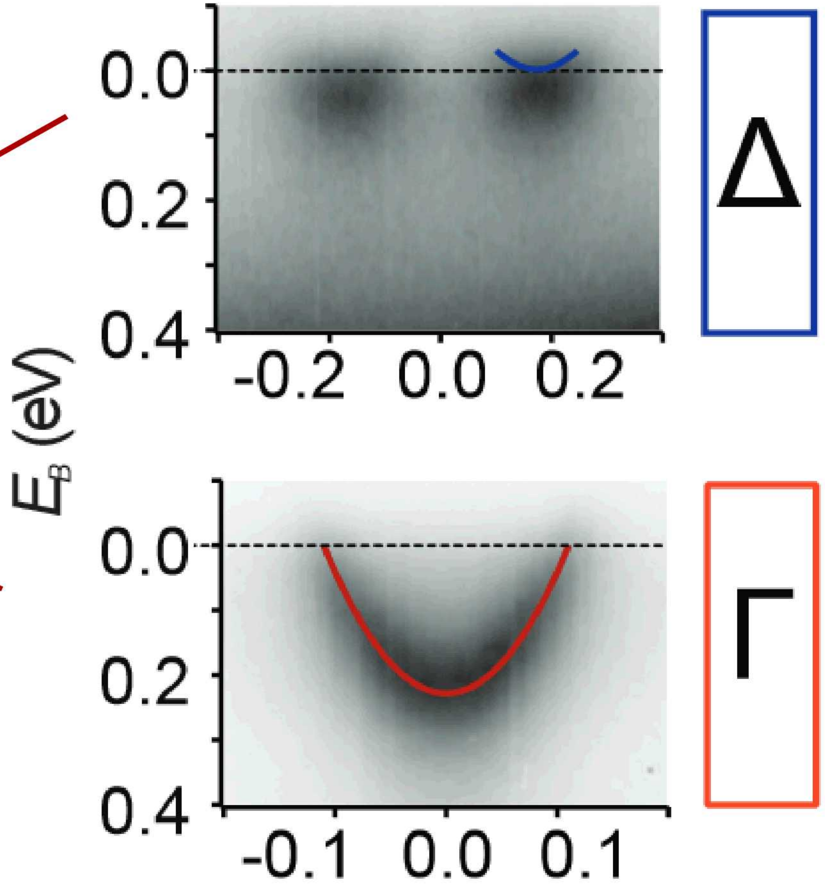


Dopants give you confinement
Extremely high current density.

Consequences: electronic structure

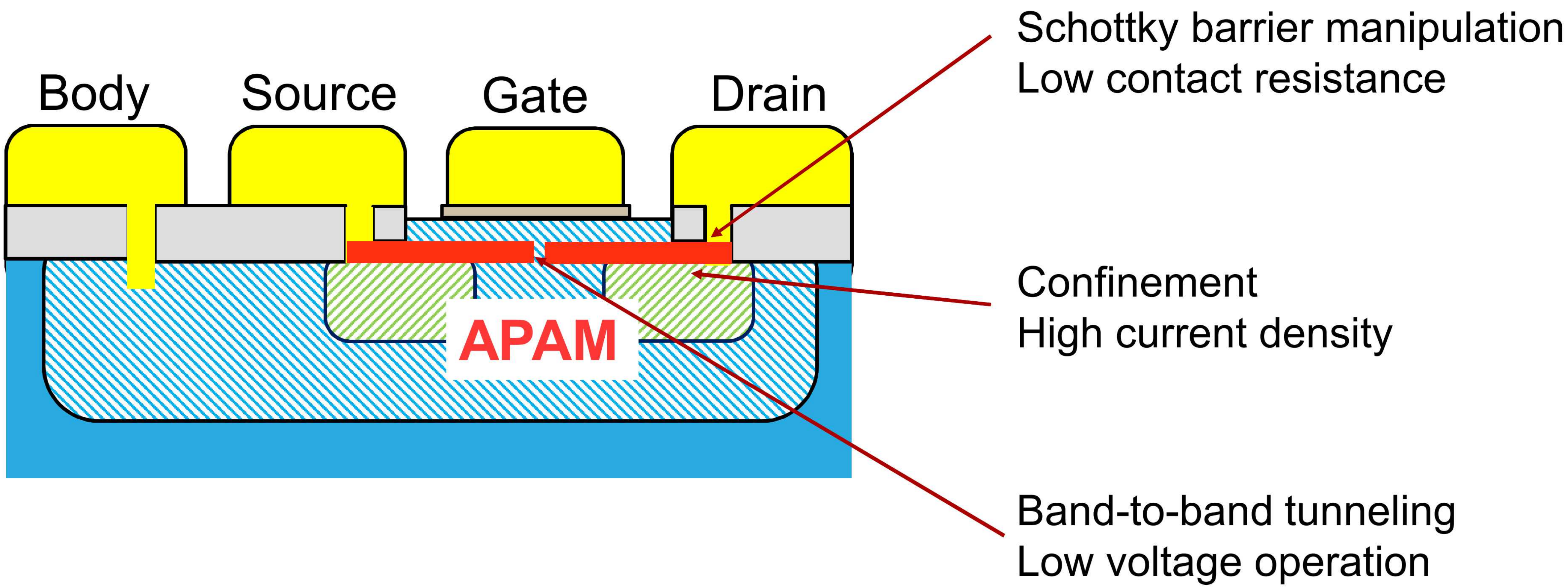


This isn't really silicon like you know it.



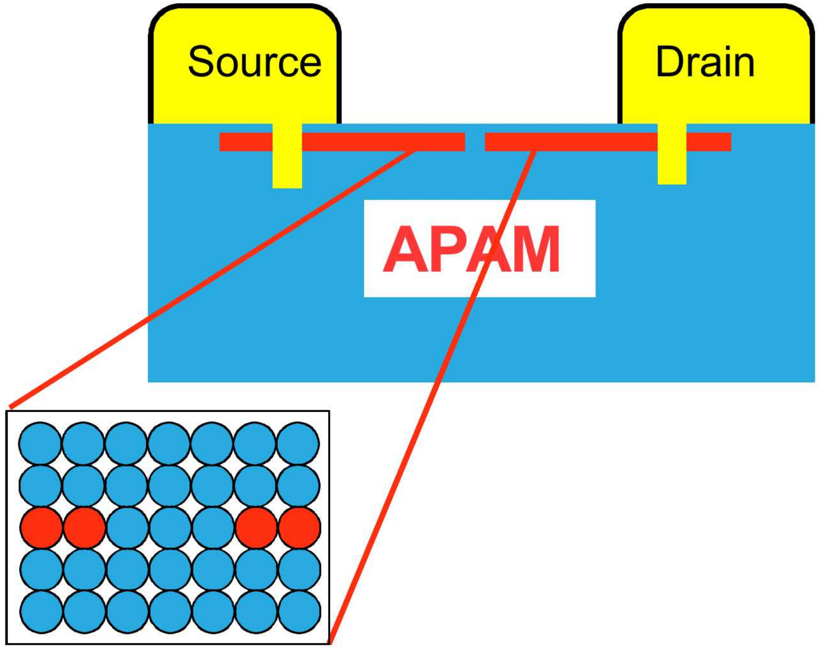
Holt, arXiv:1911.08274

APAM-inspired transistor



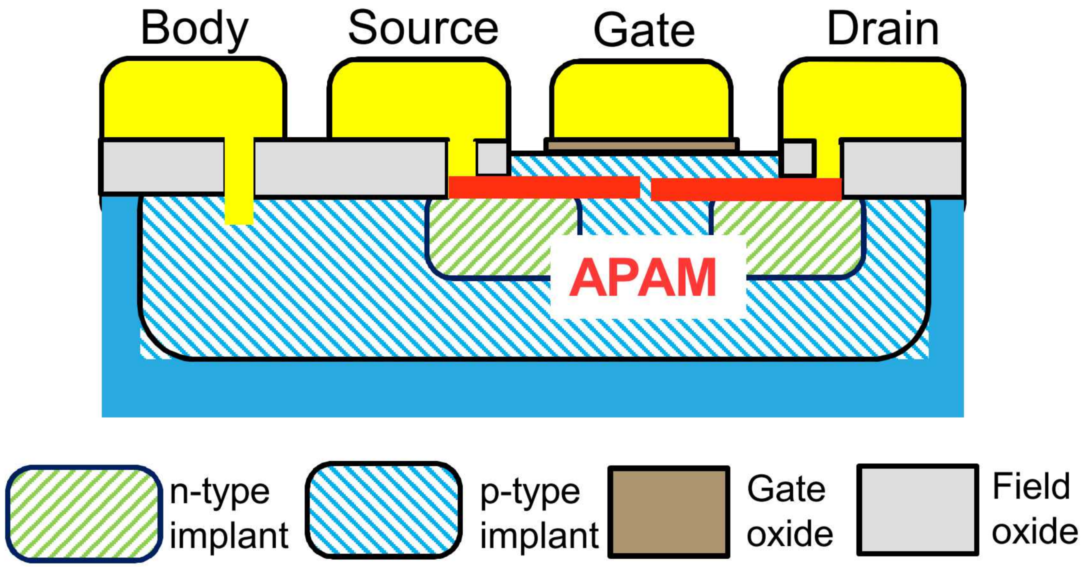
Can you make a 'real' transistor with APAM?

<u>Now (3 US labs, 6 labs worldwide)</u>



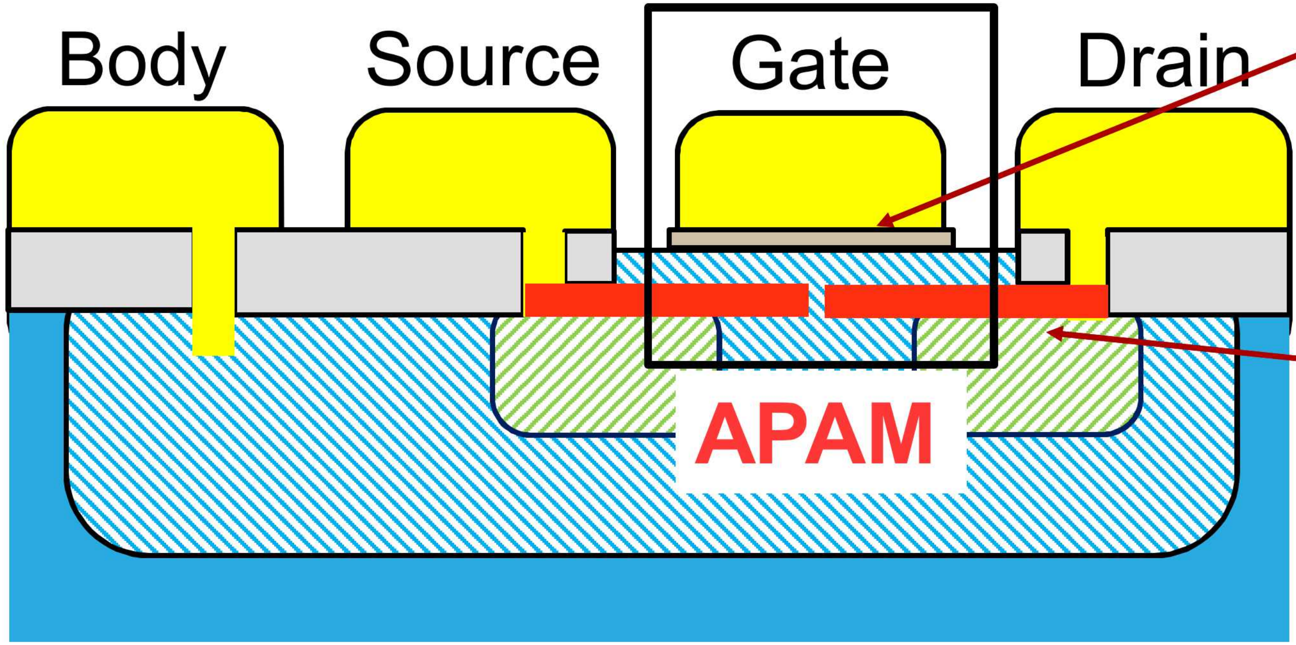
- Only works at cryogenic temperatures
- Devices consist only of phosphorus!

<u>Desired future state</u>



- Works above room temperature
- Device is complex

“Real” APAM transistor



Surface gate

[Surface-gated SET: Anderson, arXiv:2002.09075]

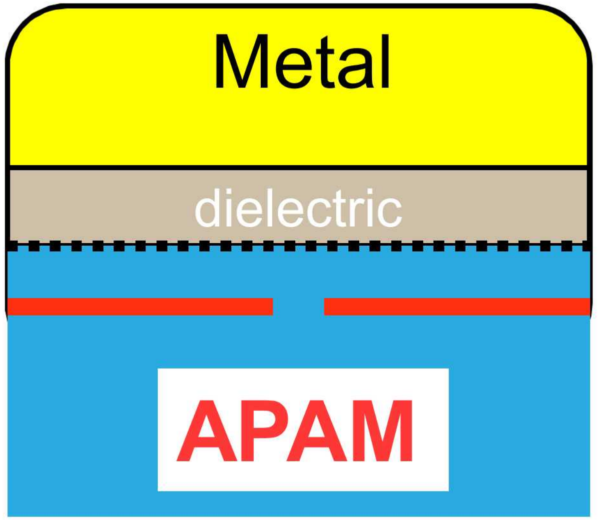
Doping profiles to confine current

Surface gate challenge: thermal budget

Dopants readily diffuse ~ 350 – 550 °C
Low defect silicon oxide needs ~ 800 °C

Modern high-k dielectrics require temperatures that are accessible

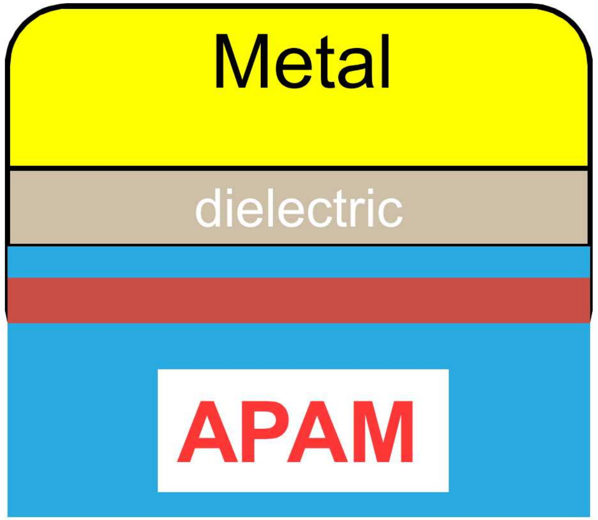
Low temperature



Poor quality interface shields gate
Dopants have remained in place

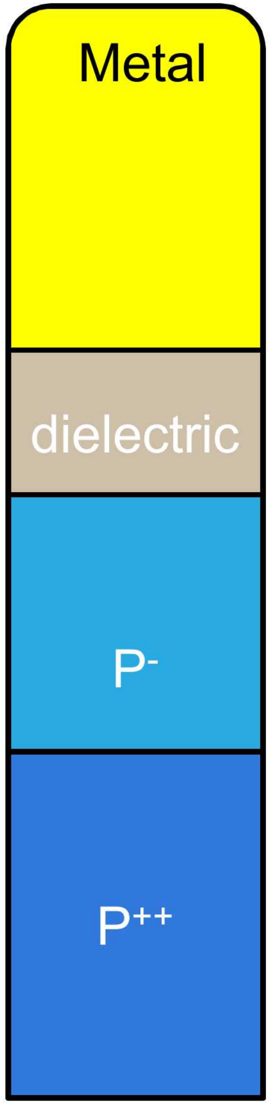
Is there a sweet spot?

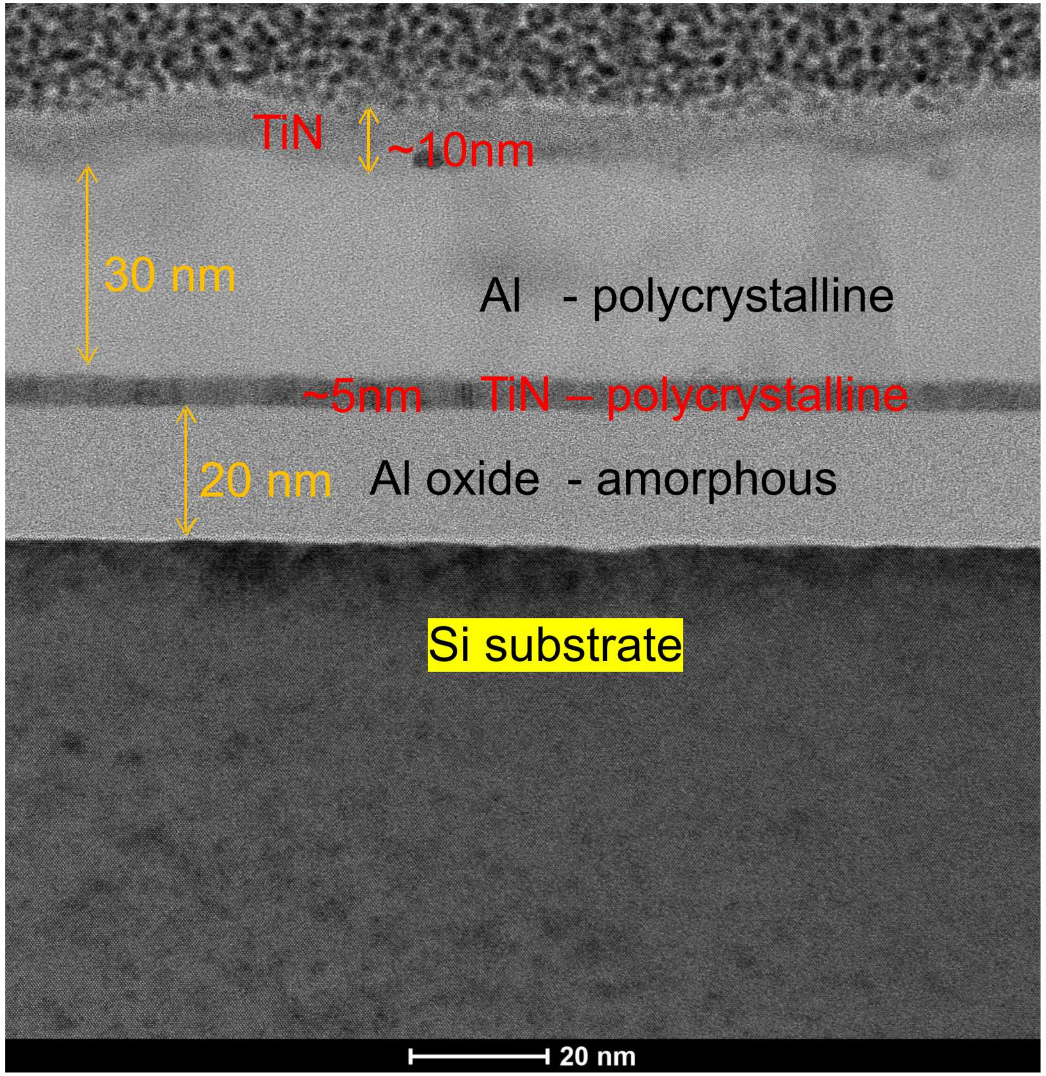
High temperature

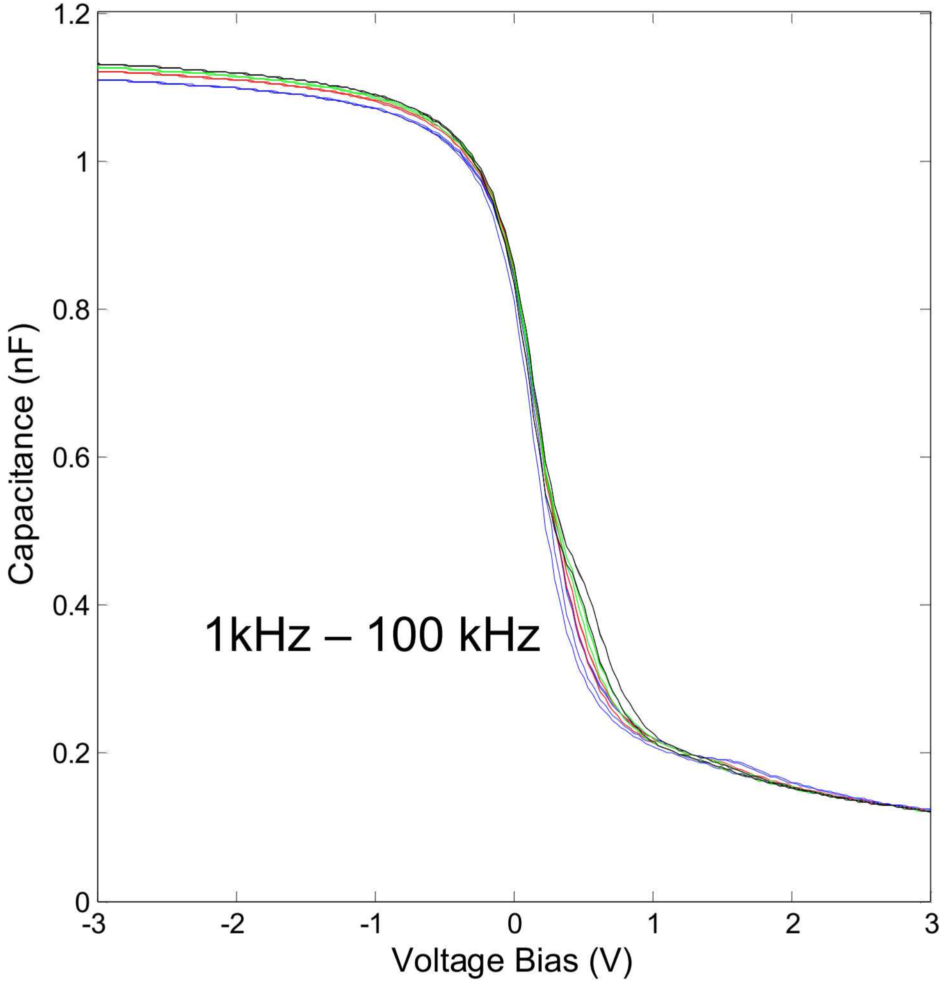


High quality interfaces
Dopants have diffused

Follow strategy for high-k/metal gates

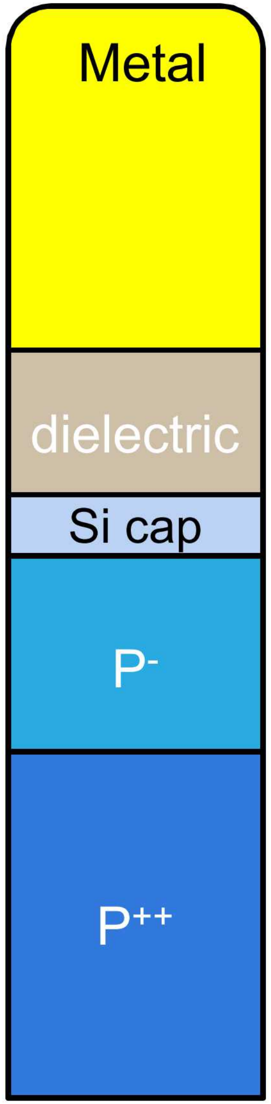


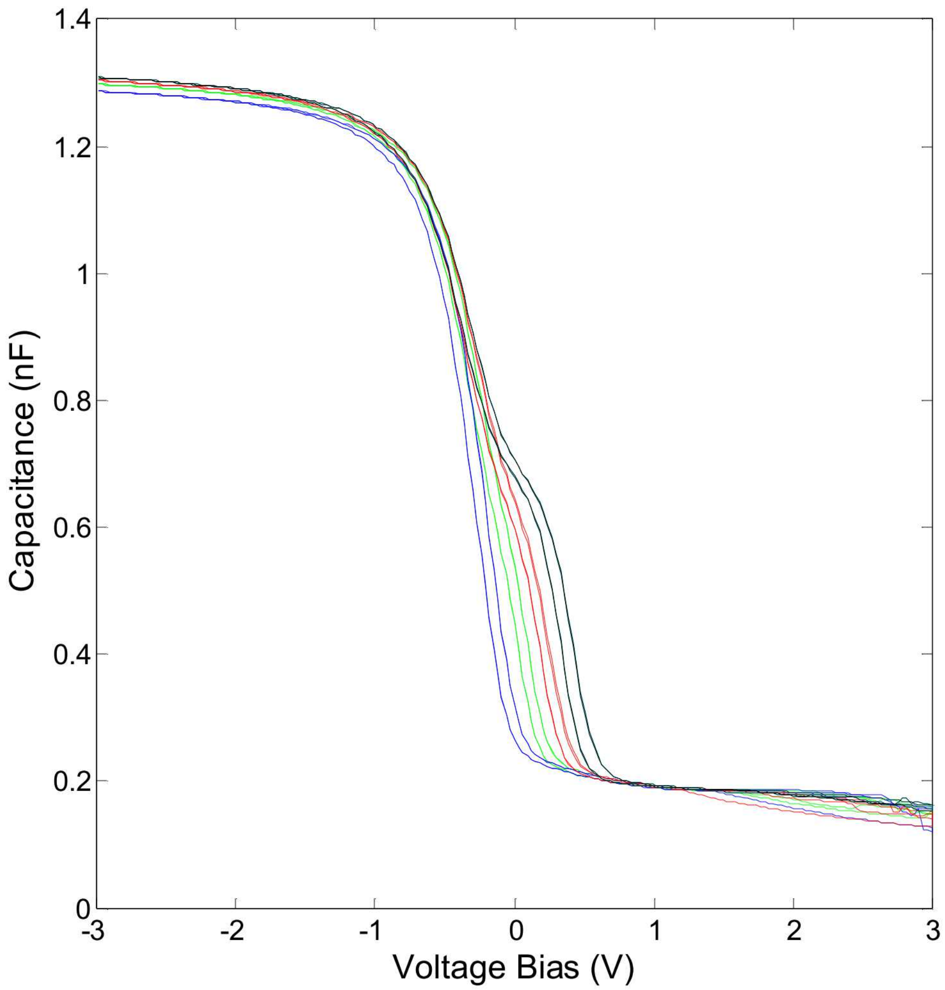




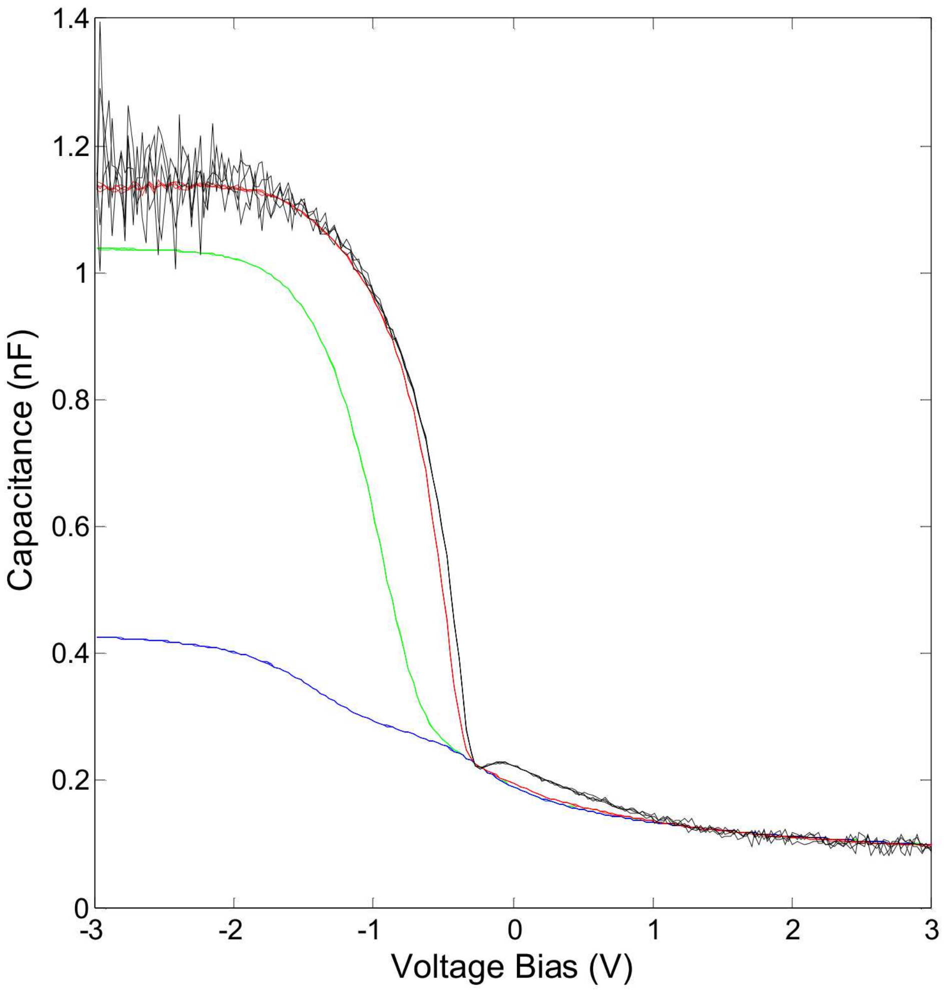
Thermally compatible with APAM (250 °C). Low density of interface defects: 4×10^{10} cm^{-2}

First-ever CV curve on an APAM layer

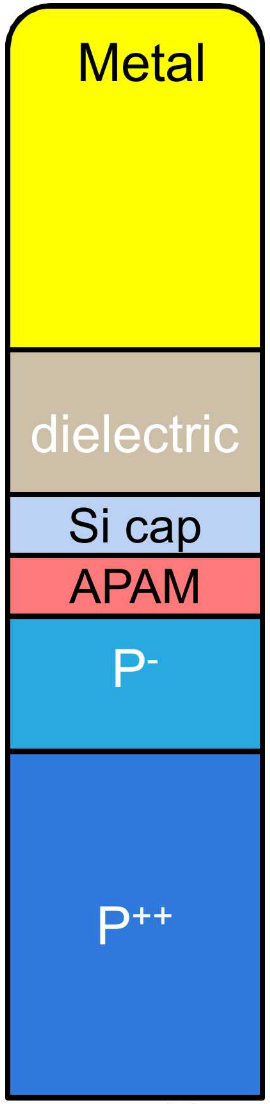




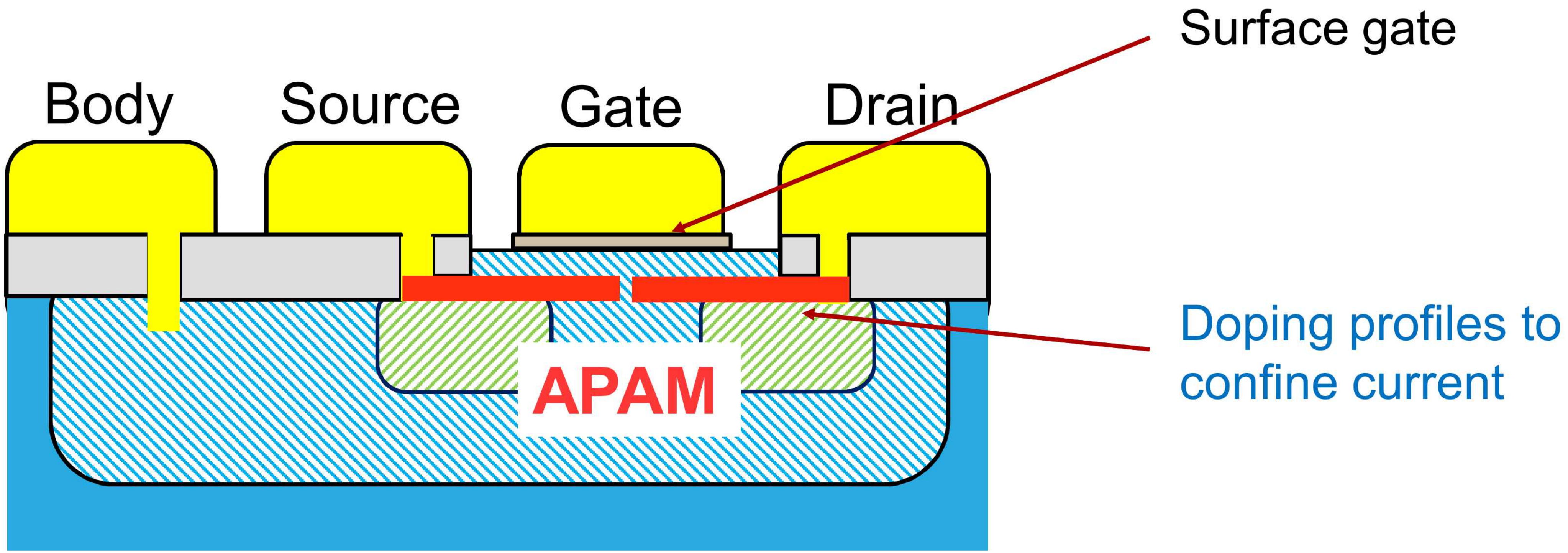
Surface charge: 1×10^{11} cm^{-2}



Soon: finite frequency TCAD model



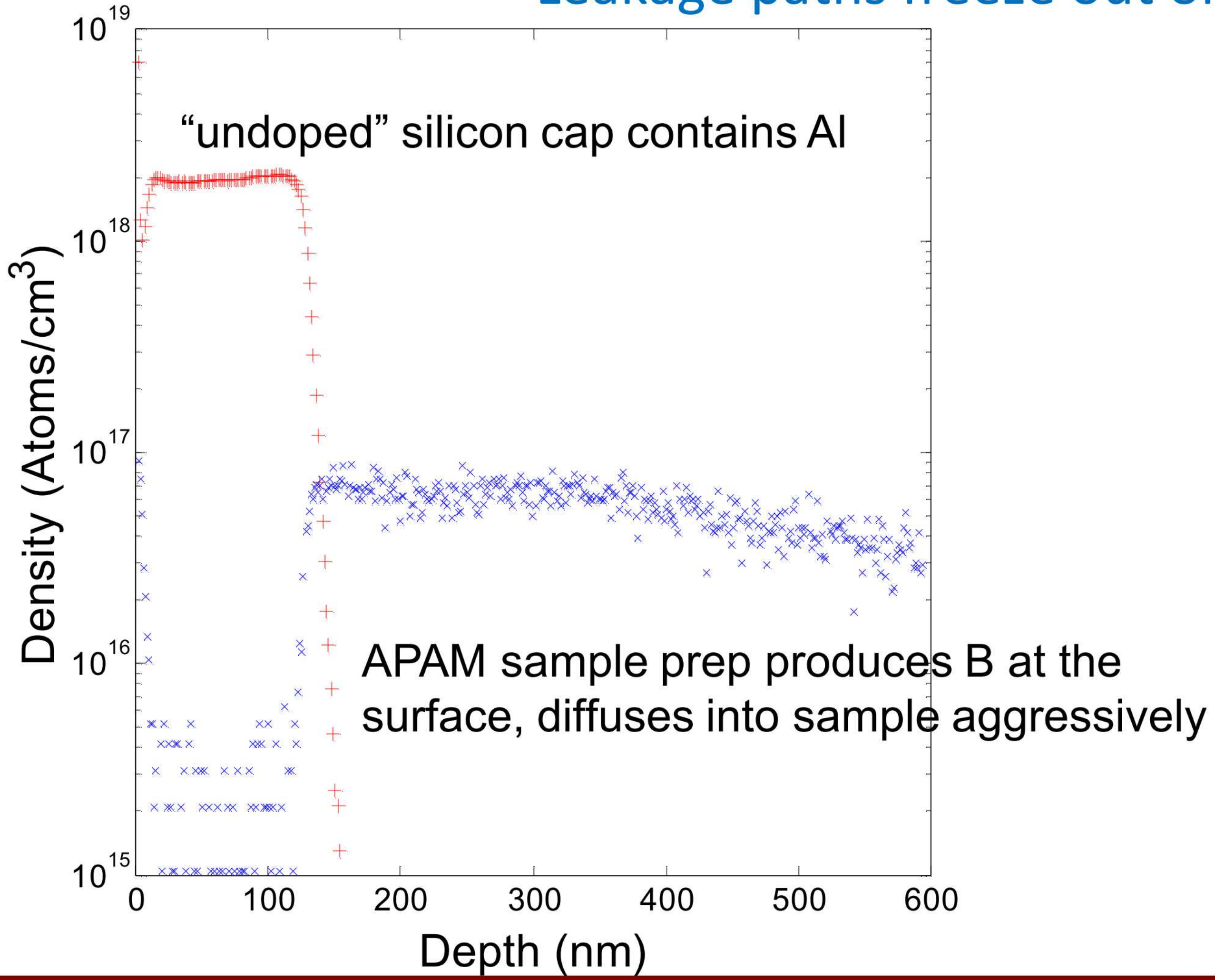
“Real” APAM transistor

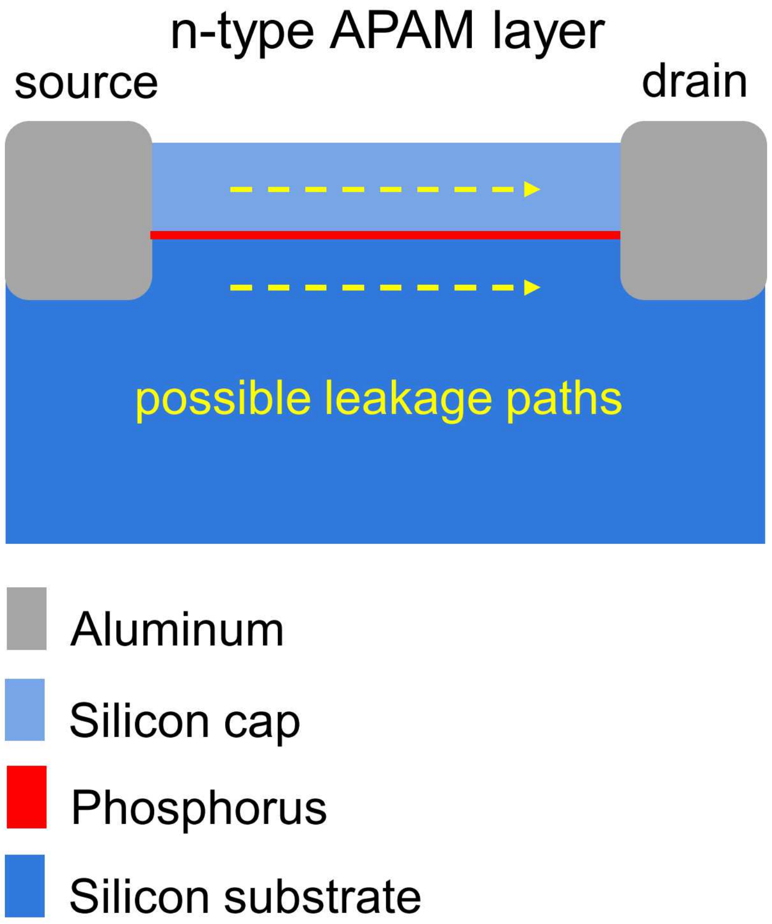


Room Temperature Device Operation

Unintentional doping of cap and substrate

Leakage paths freeze out only at low temperatures



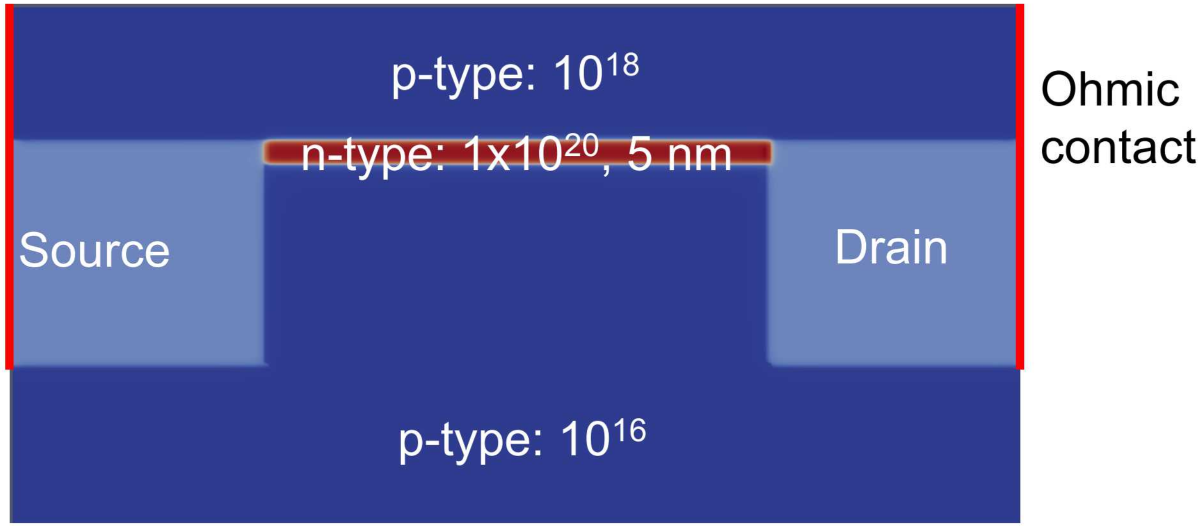


TCAD Simulations

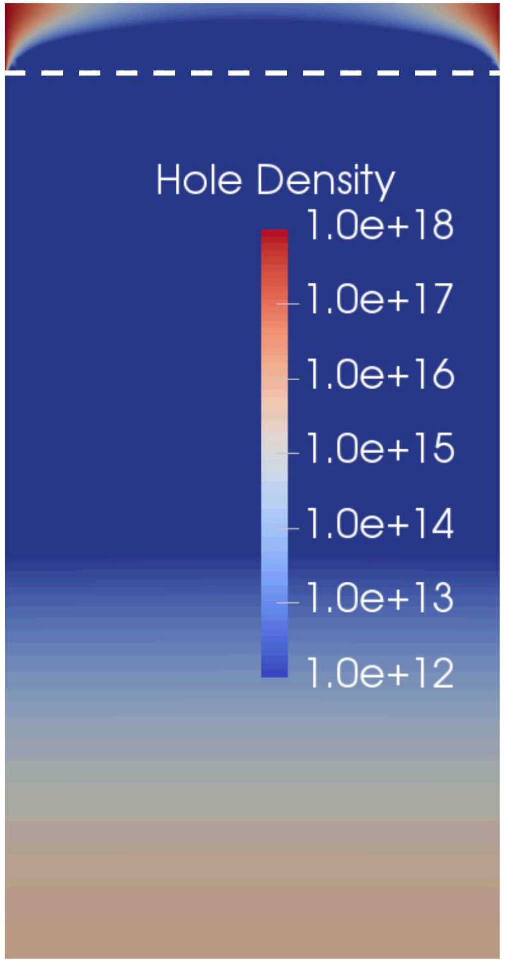
Sandia National Laboratories

APAM layer depletes the substrate and cap

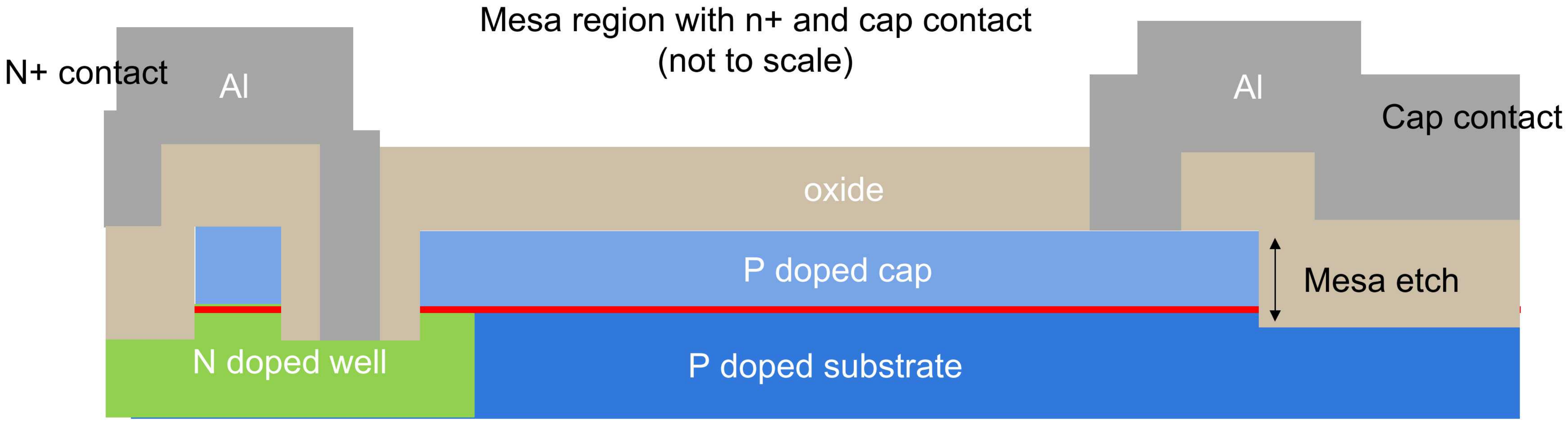
Simulation Structure



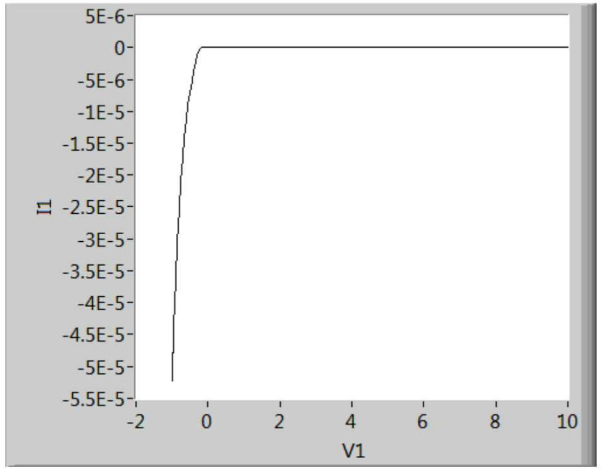
Hole Density from TCAD

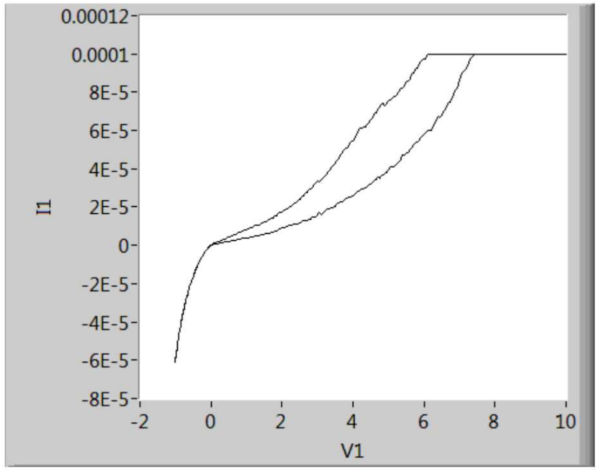


Contact isolation



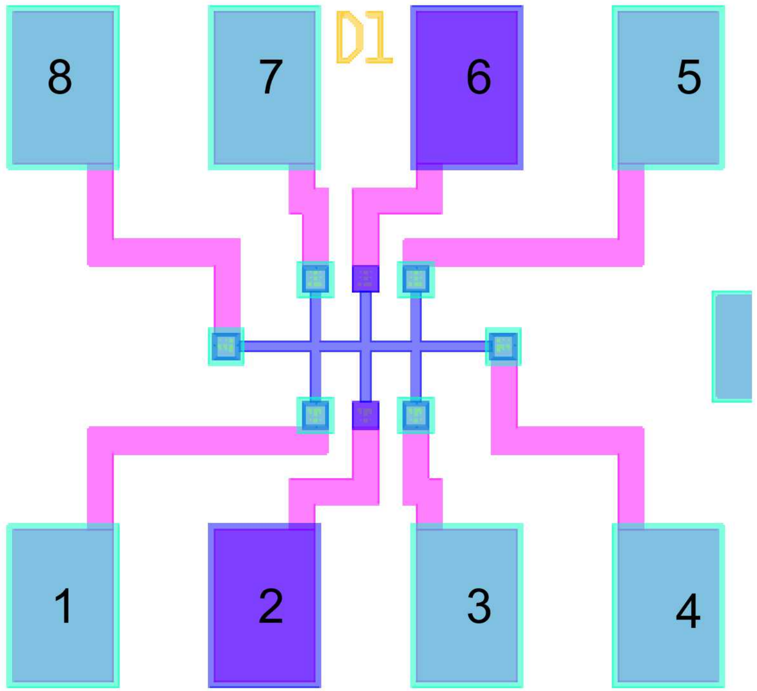
After wire bonding
25 g force





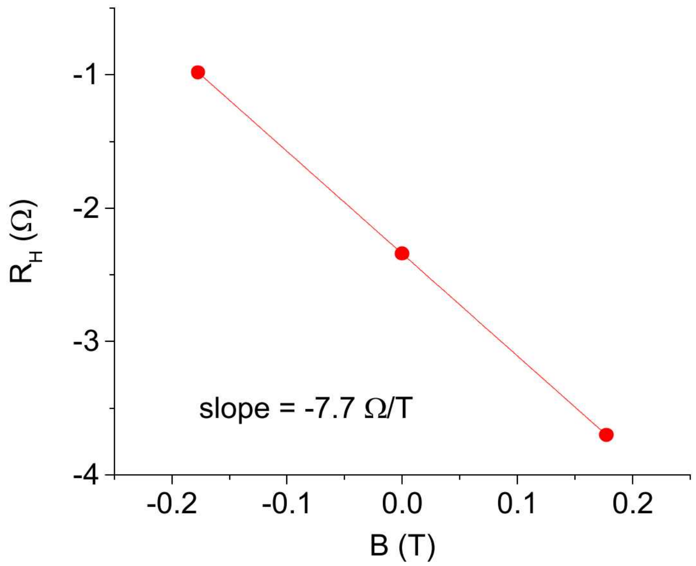
After wire bonding
35 g force

1^{st} measurement of APAM wire at room temp.



R_{xx}: 4.80 mV/450 nA

(20-40 nA leakage at 1V)

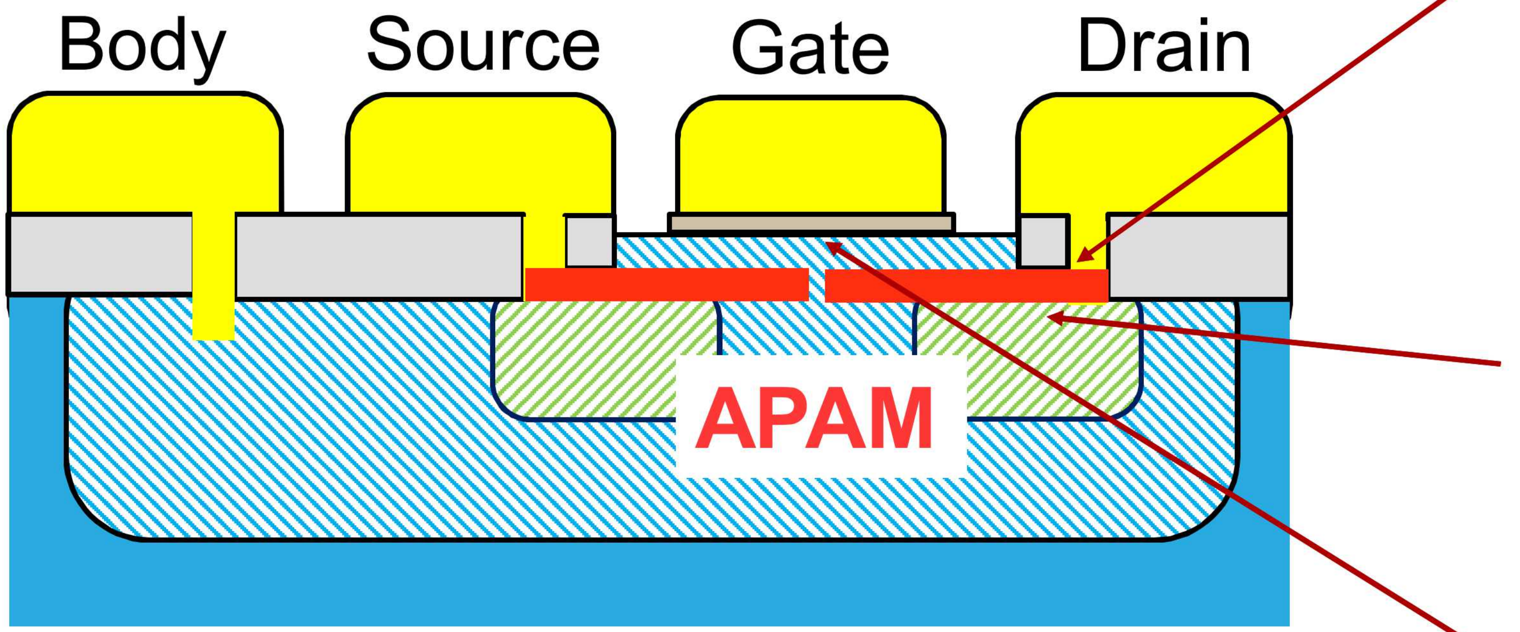


Temperature	Resistivity	Carrier density	Mobility
4 K	600 Ω/sq	1.7×10^{14} cm^{-2}	55
293 K	1070 Ω/sq	0.8×10^{14} cm^{-2}	65

Unclear why density goes down, mobility stays same.

Agrees with IR measurements
Katzenmeyer, in submission to JMR (2020)

What's next?



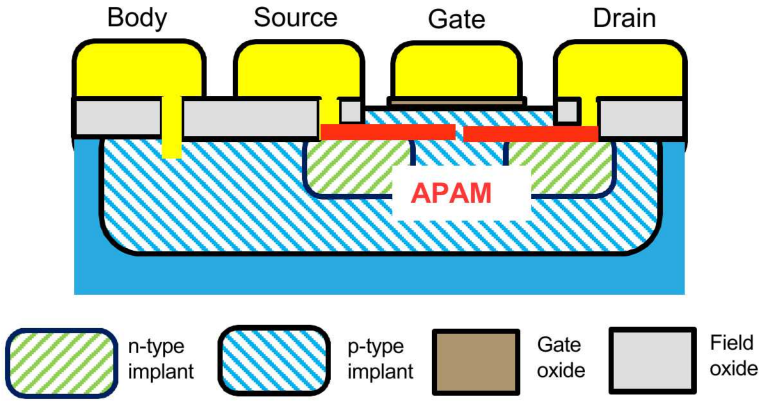
Understand contact resistance

Understand electrical properties in stressful conditions

Design a transistor

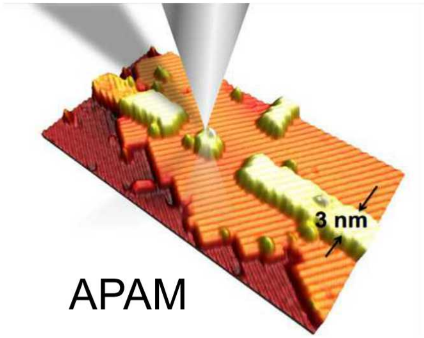
How to get to digital electronics at the atomic scale?

1. APAM devices



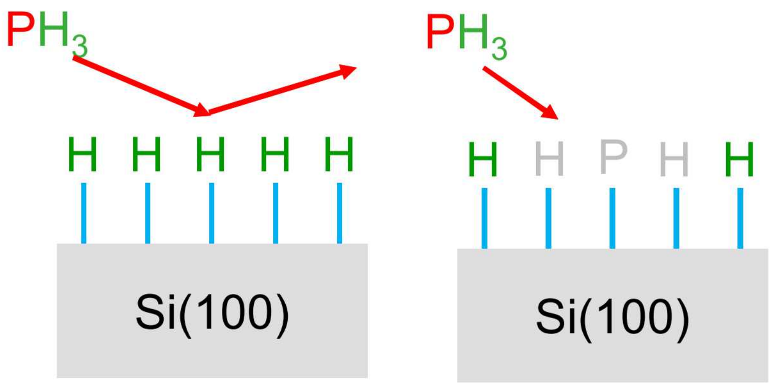
- ✓ Surface gated APAM devices
- ✓ Operate at room temperature
- ❑ APAM transistor

2. CMOS integration



- ☐ Incompatible with CMOS workflows / parts

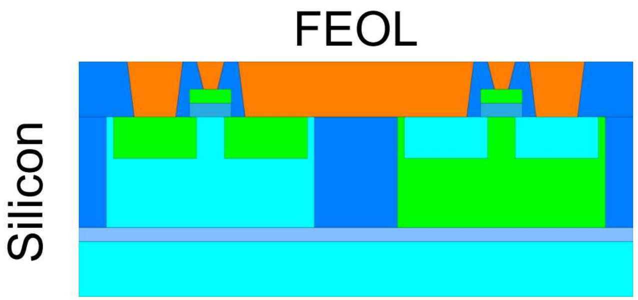
3. APAM toolkit



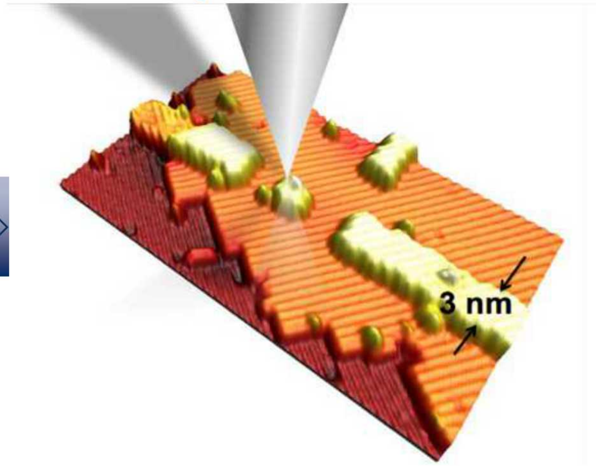
- ☐ One working chemistry

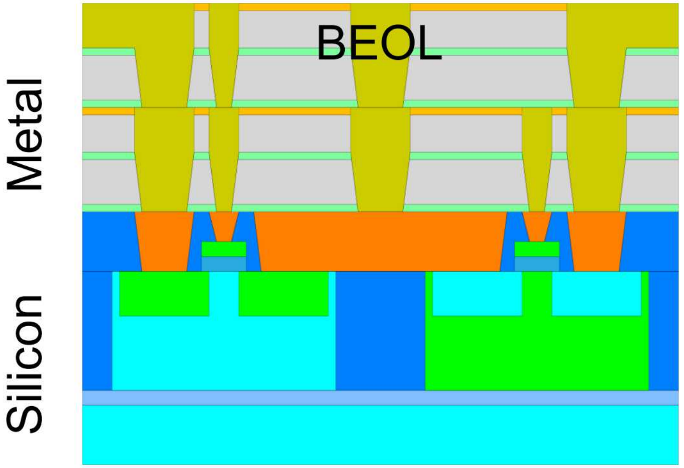
Is APAM thermally compatible with CMOS fab?

Direct CMOS Integration



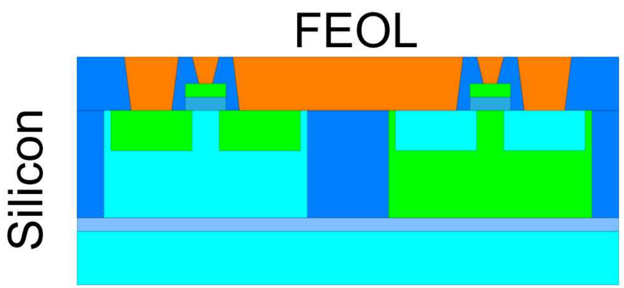
T > 850 °C



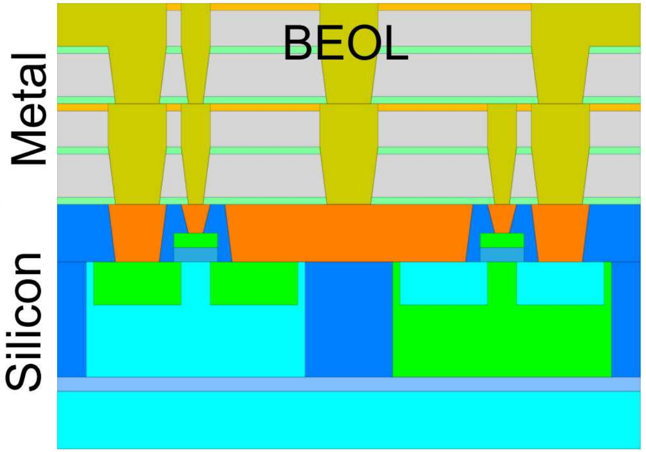


T < 450 °C

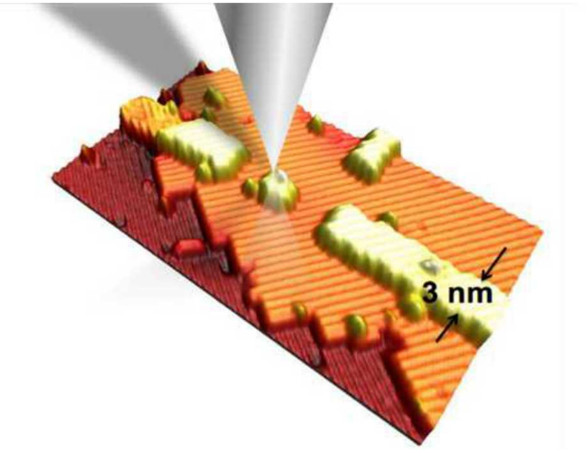
Post CMOS Integration



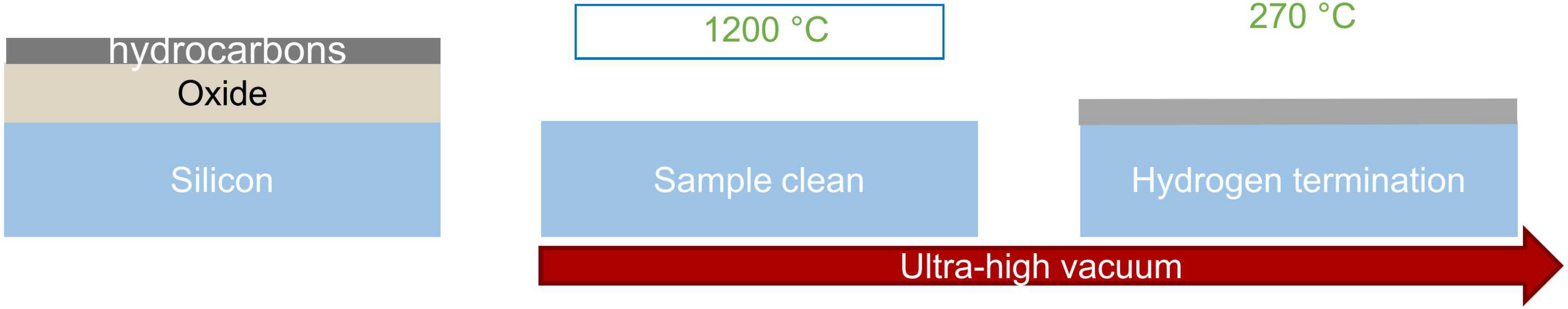
T > 850 °C



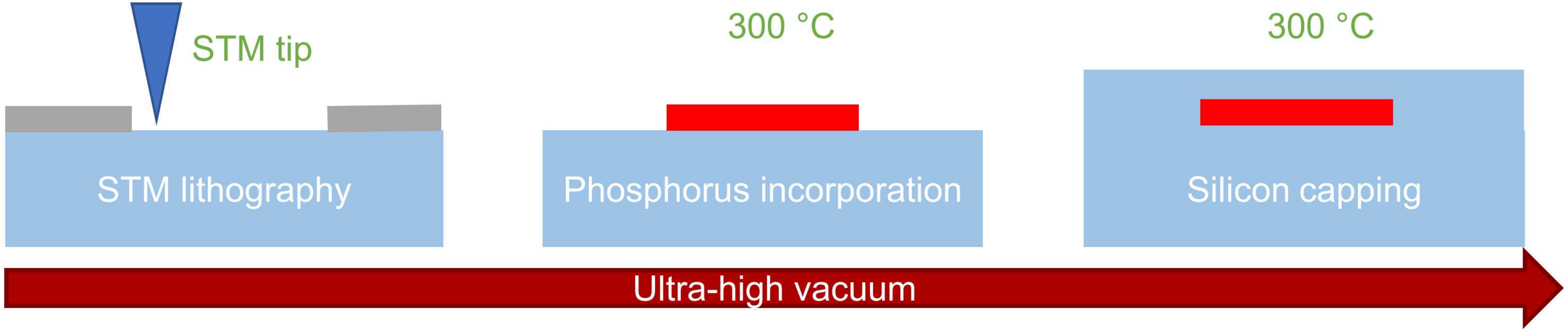
T < 450 °C



APAM process flow

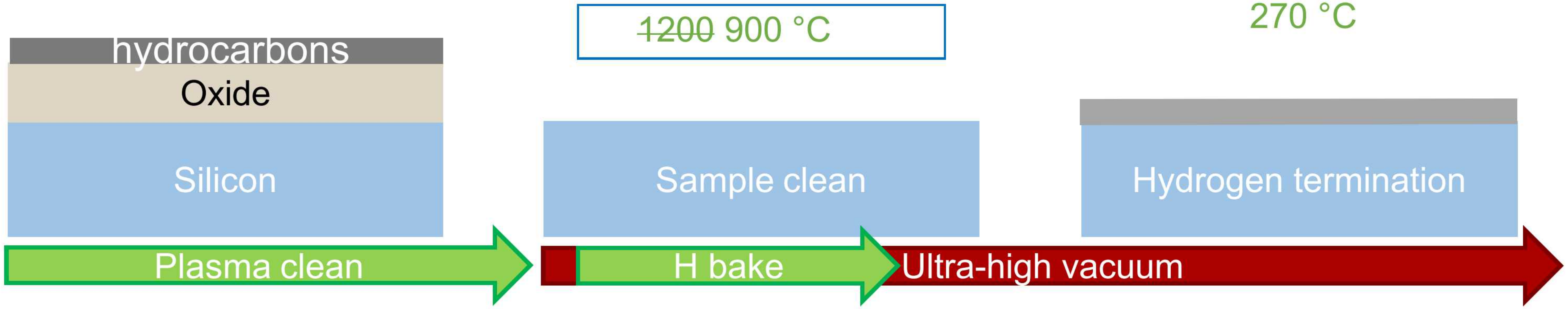


High-temperature clean destroys anything on chip before APAM.



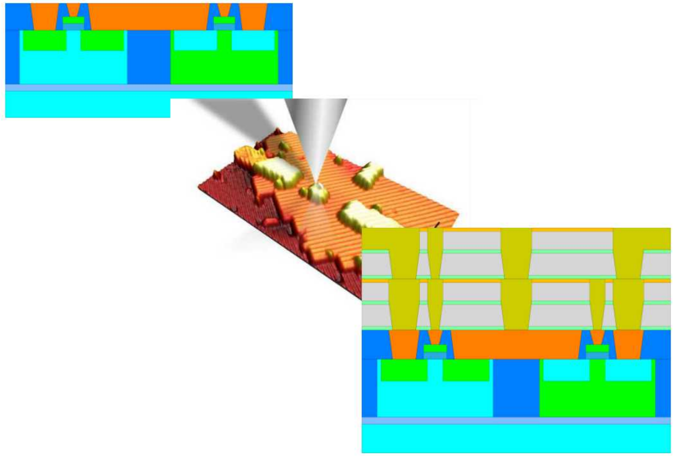
APAM will start to diffuse above 350 – 550 °C

APAM process flow

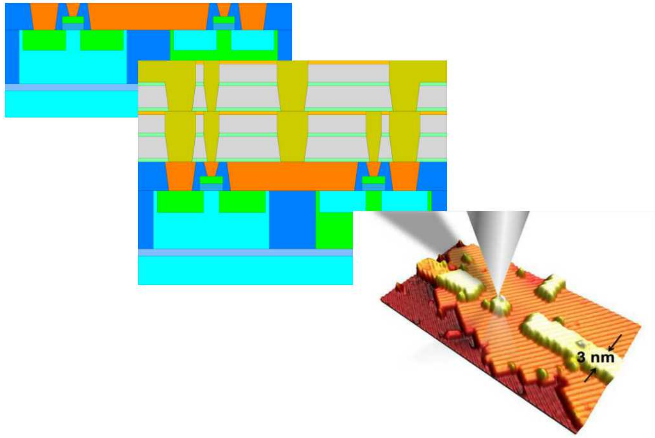


Ward, Appl. Phys. Lett. (2017)

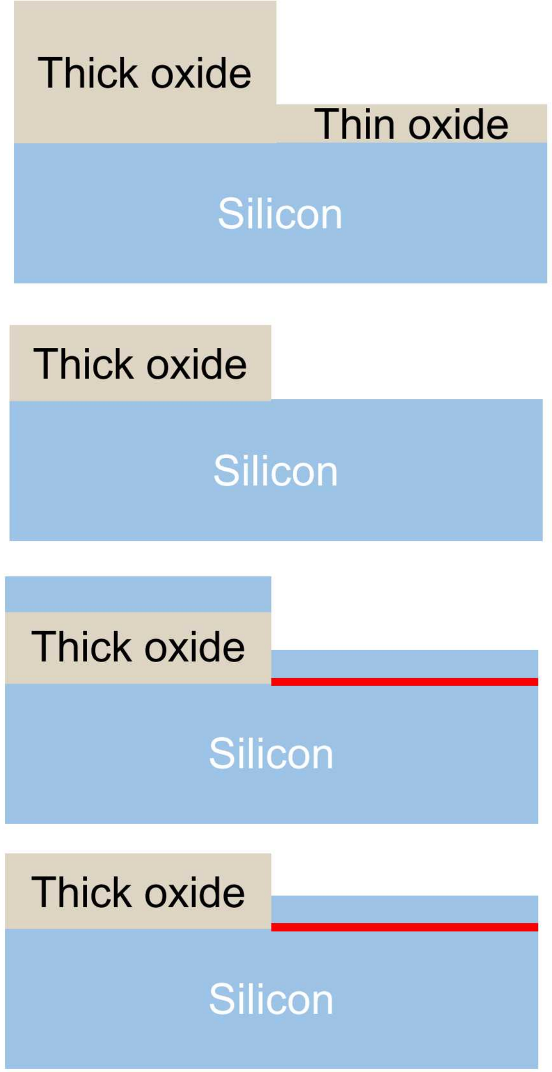
Direct Integration: can we do wafer-scale APAM processing?

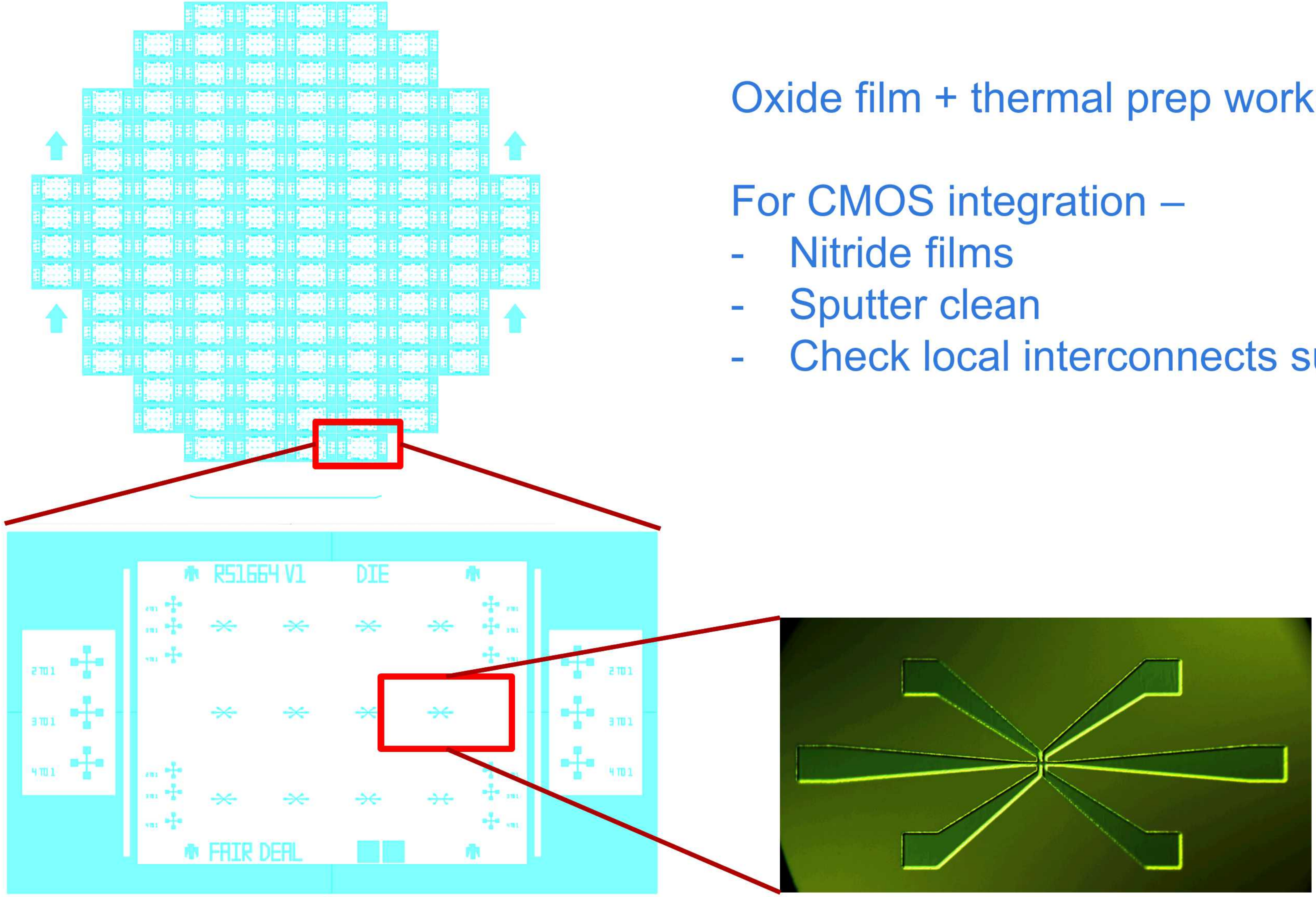


Post-CMOS integration: how low can we drive down process temperatures, even with sub-optimal results?



Scale APAM using hard masks





Oxide film + thermal prep works.

For CMOS integration –

- Nitride films
- Sputter clean
- Check local interconnects survive

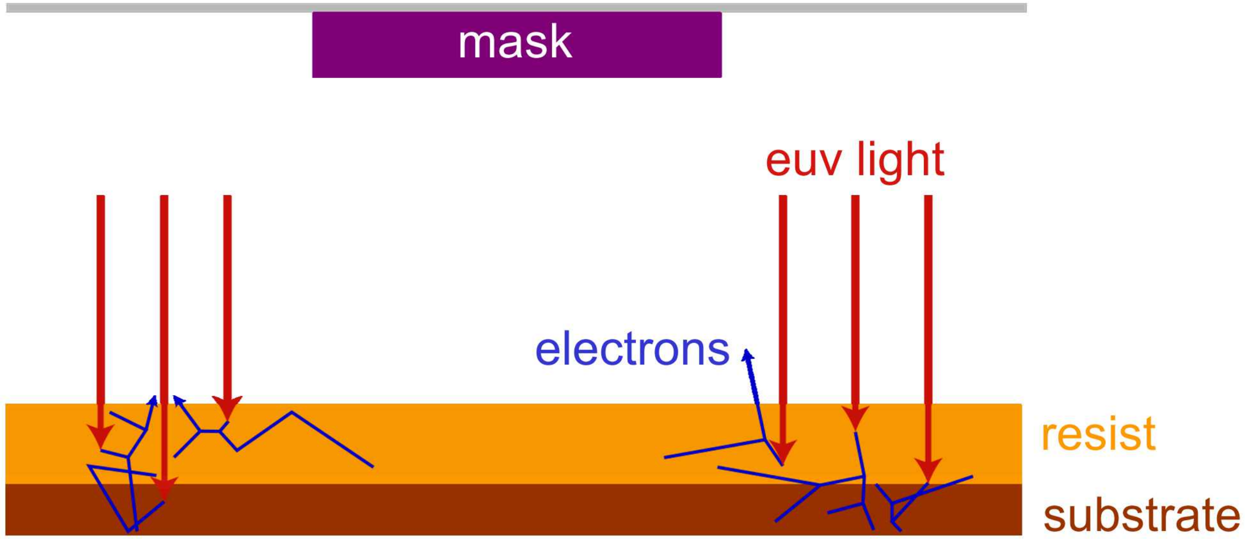
Scrymgeour, Schmucker, Anderson, Campbell

Not just ‘atom-sized transistors’… atomic-scale processing

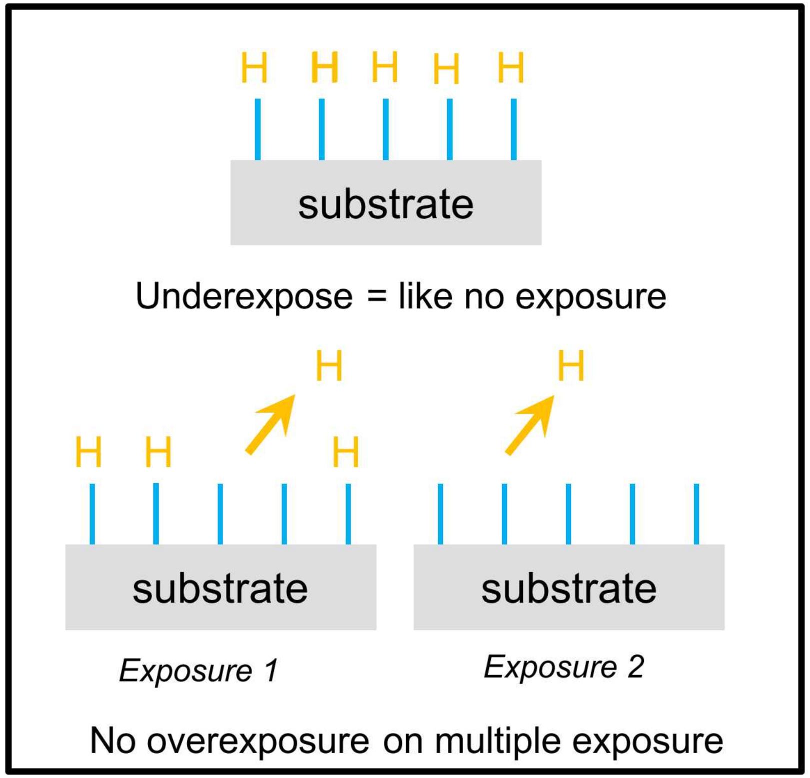
Sandia National Laboratories

Traditional polymer resist

- Shot noise of light
- Statistics of e- generation
- Statistics of polymers



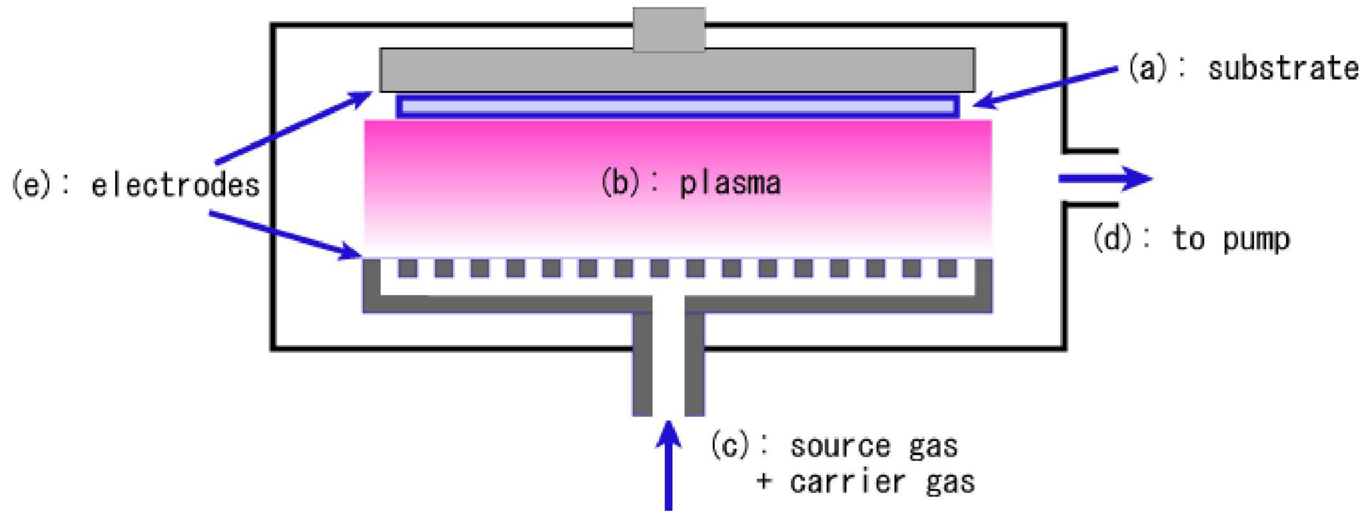
Atomic-scale resist



- Can’t be over-exposed or under-exposed → solves problems with shot noise
- Stable to arbitrary pitch
- *Katzenmeyer, Proc. SPIE (2020)*

Scale APAM process

Wafer-scale processing by adding on to existing tool (ALD or CVD)

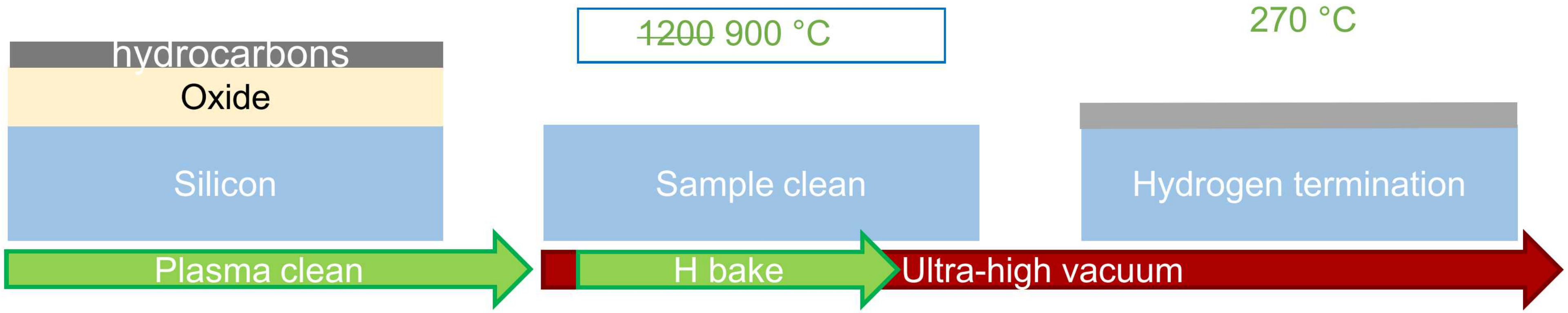


Challenges:

- Elevated pressure
  - After wafer clean – proceed to doping, or preserve surface with H?
  - Kinetics of dopant incorporation
- Low temperature growth
  - Only MBE known to work at these temperatures
  - Radical growth? Beam-assisted? Chemical - TCS/DS?

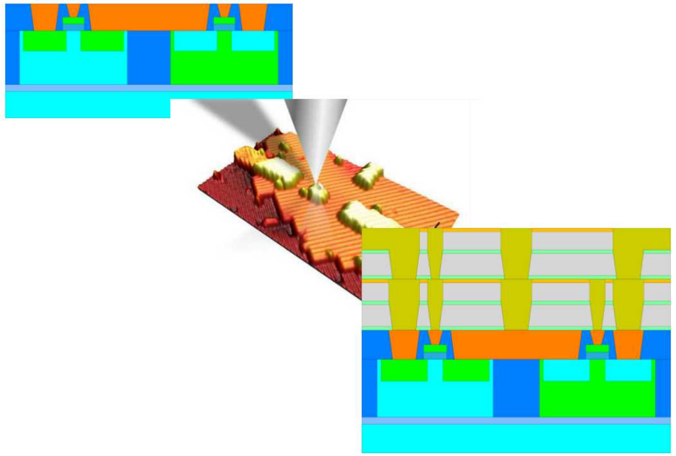
Looking for partners.
Skywater Technologies can host a tool.

APAM process flow

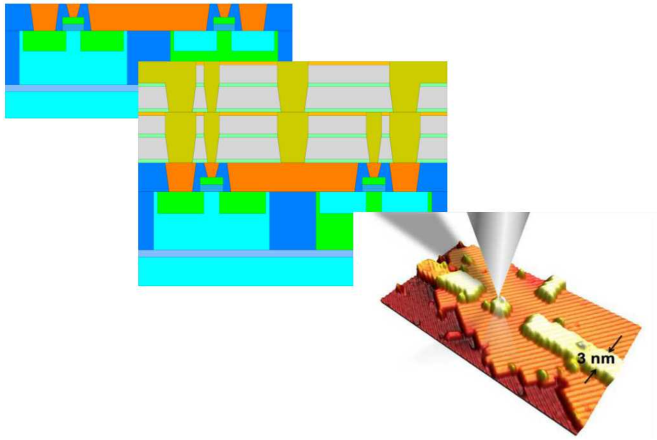


Ward, Appl. Phys. Lett. (2017)

Direct Integration: can we do wafer-scale APAM processing?

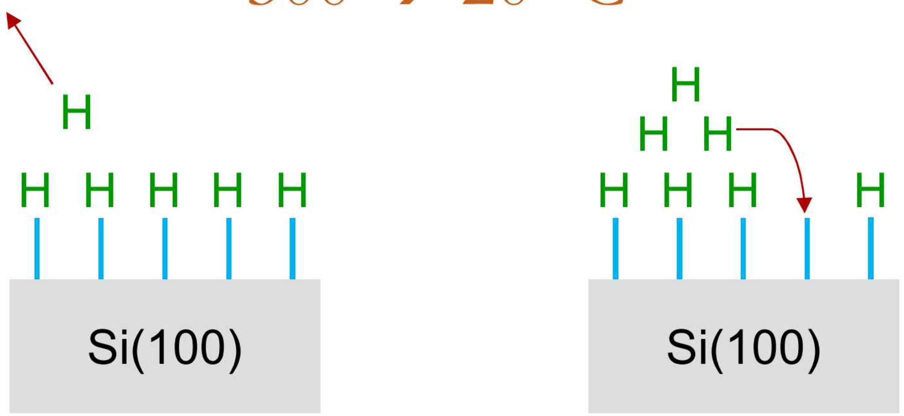


Post-CMOS integration: how low can we drive down process temperatures, even with sub-optimal results?

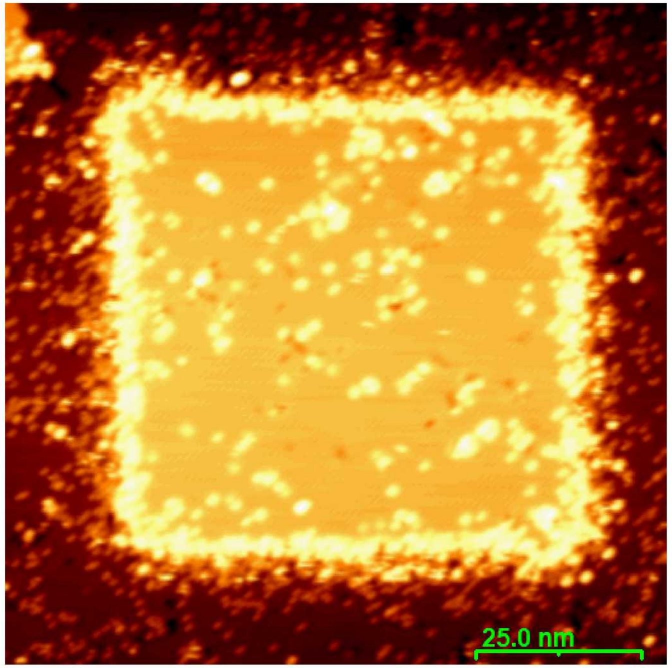


Hydrogen passivation & lithography

300 → 20° C



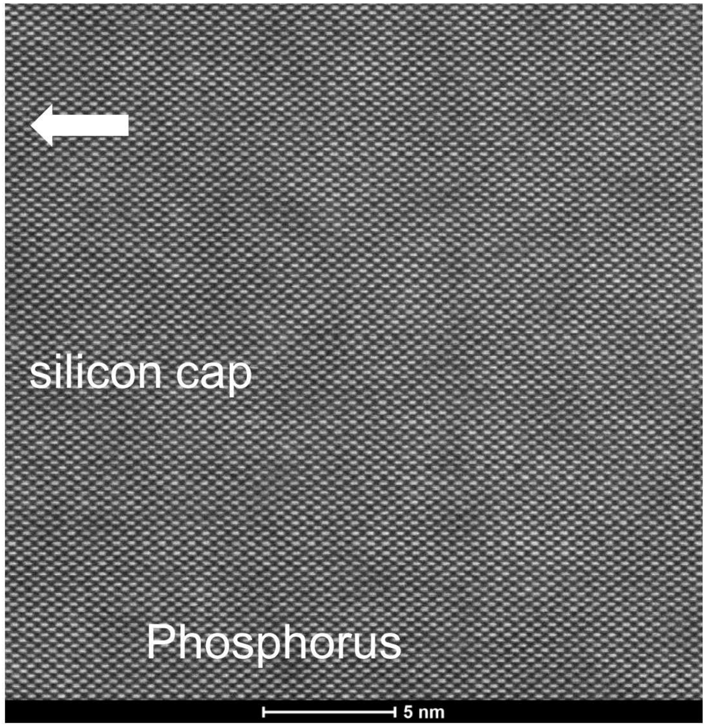
20° C: Hydrogen physisorbed on top of hydrogen passivated silicon



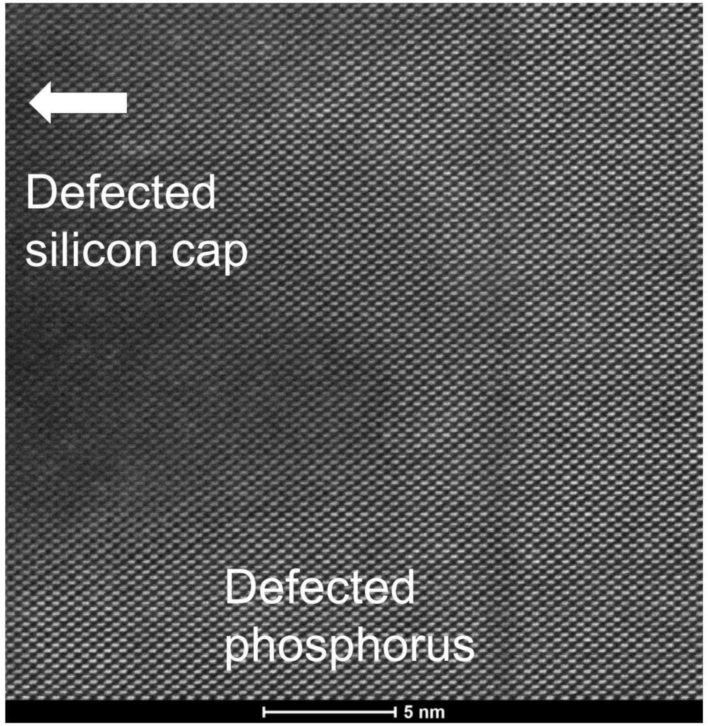
Lithography now requires multiple passes, but works great!

Phosphorus incorporation and capping

350 → 200° C



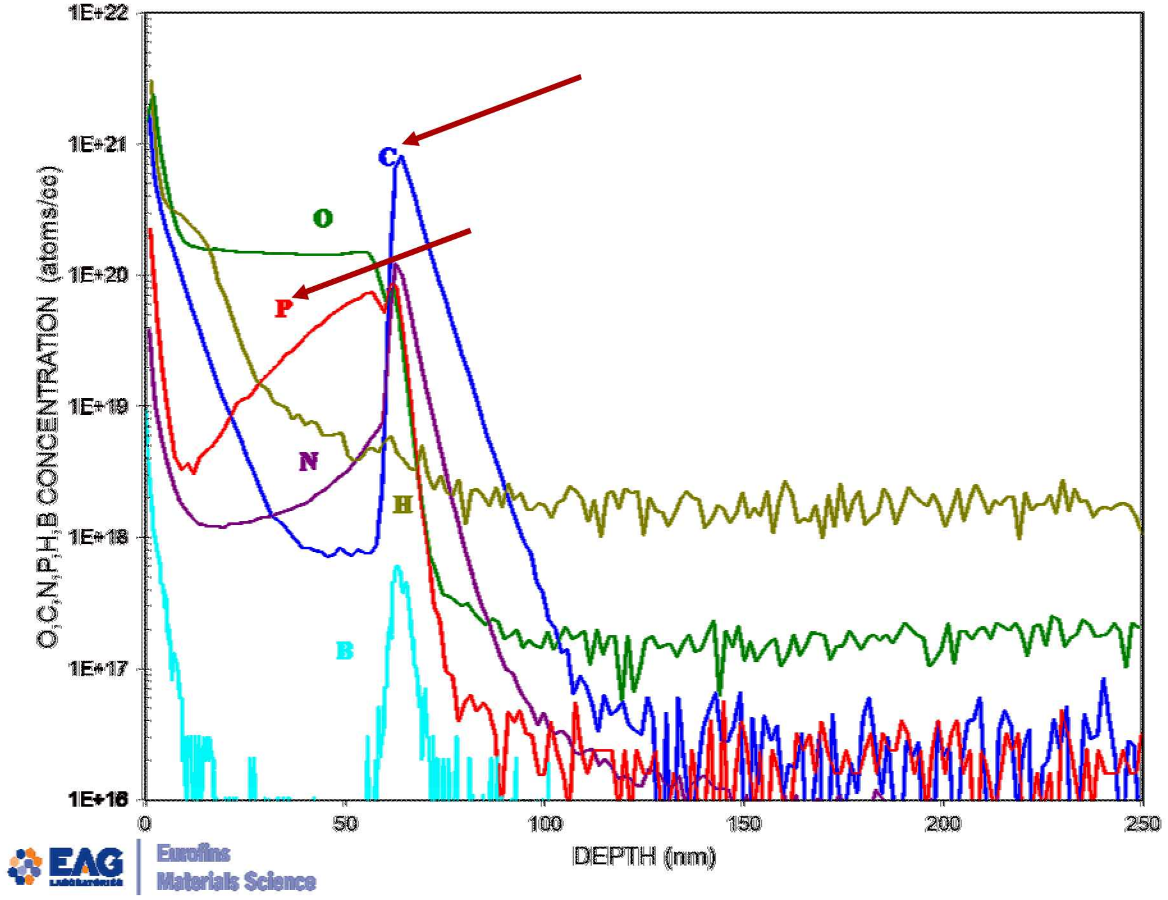
n ~ 1.7 x 10^{14} cm^{-2}
μ ~ 50 cm^2/V-s
σ ~ 2 mS/sq.



n ~ 1.4 x 10^{14} cm^{-2}
μ ~ 20 cm^2/V-s
σ ~ 0.6 mS/sq.

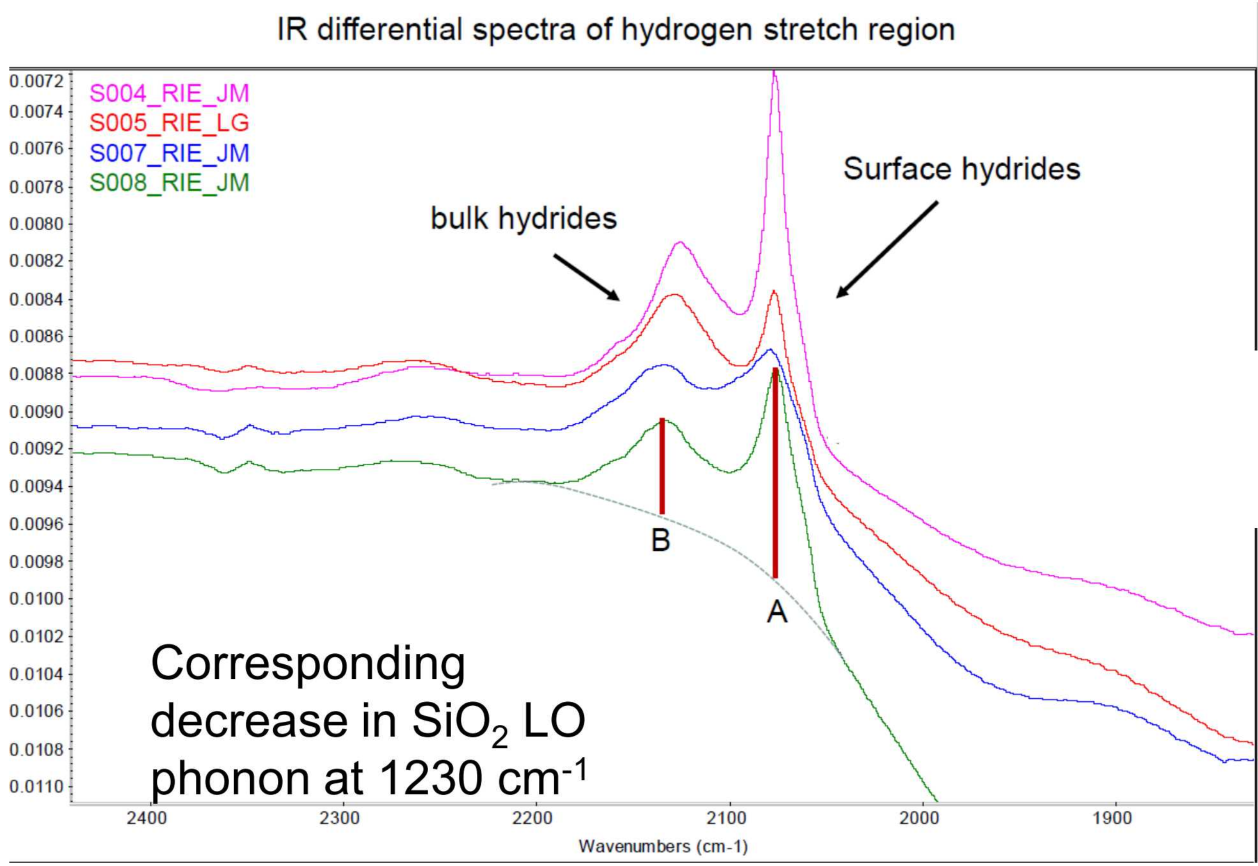
Electrical transport degrades only by a factor of 3 vs. optimal process

Reduced temperature sample prep



Wet preparation is not working

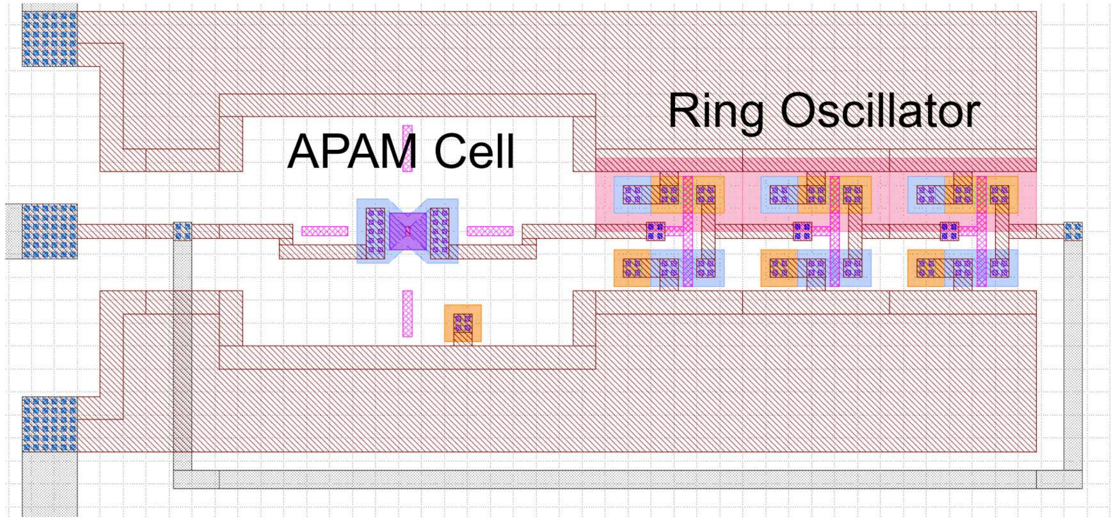
Hines, J. Phys. Chem. C (2009)



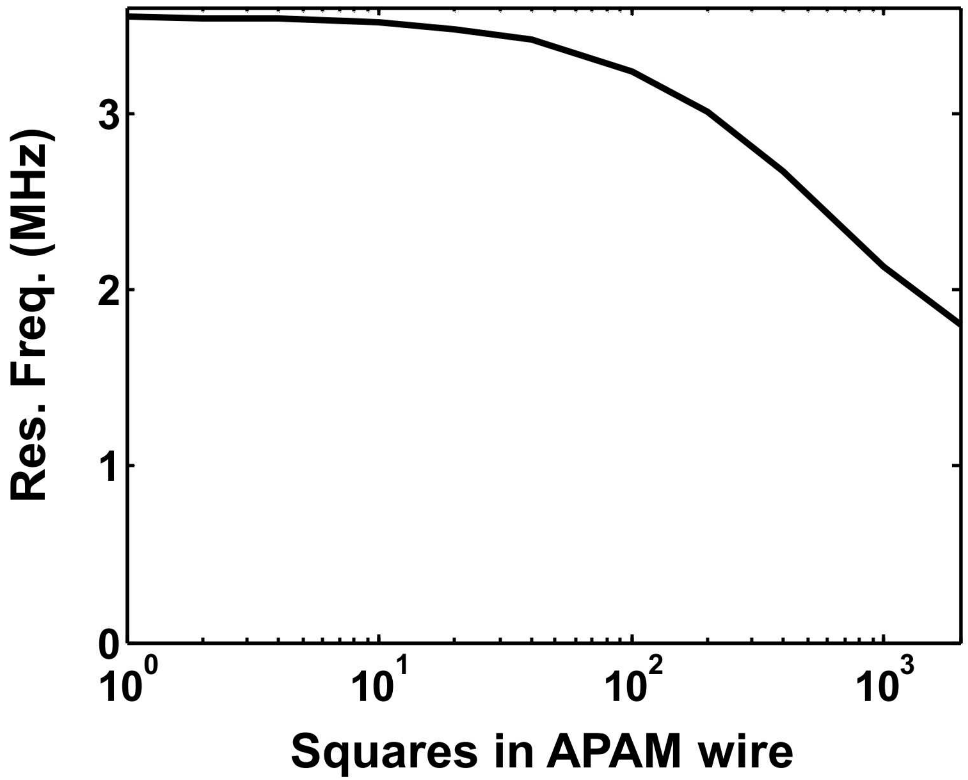
RIE has shown promising results, but reproducibility problems. Trying in a variety of tools.

What's next? Go for it!

Physical Layout



Full-stack simulation



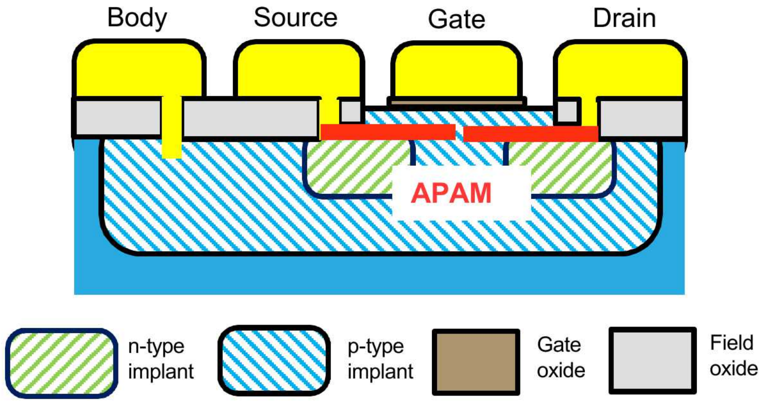
Measure effect of APAM on real CMOS parts

Leenheer, Campbell, Gao, Lepkowski

How to get to digital electronics at the atomic scale?

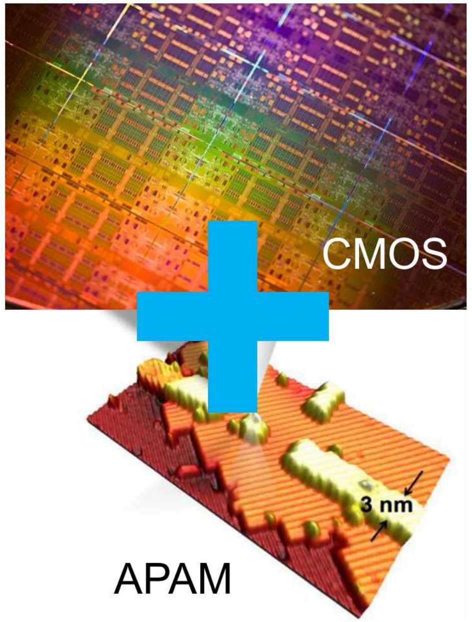
Sandia National Laboratories

1. APAM devices



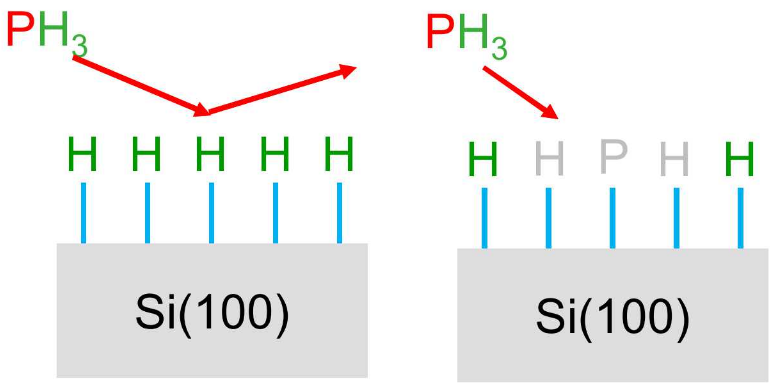
- ✓ Surface gated APAM devices
- ✓ Operate at room temperature
- ❑ APAM transistor

2. CMOS integration



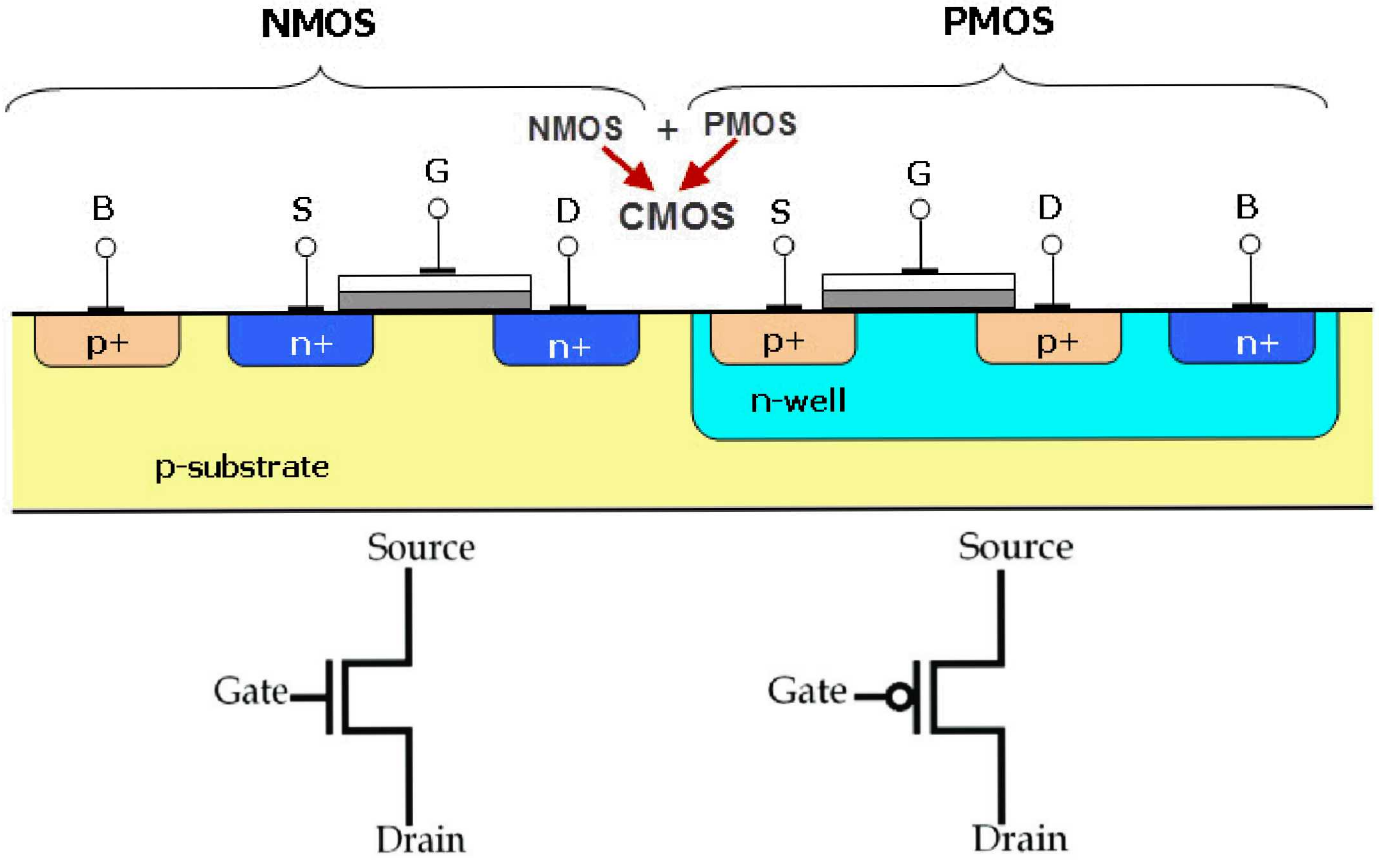
- ✓ Direct integration: wafer-scale APAM litho
- ❑ Wafer-scale APAM process
- ✓ Post-CMOS: reduction of process temperatures
- ❑ Reduced temp. sample prep

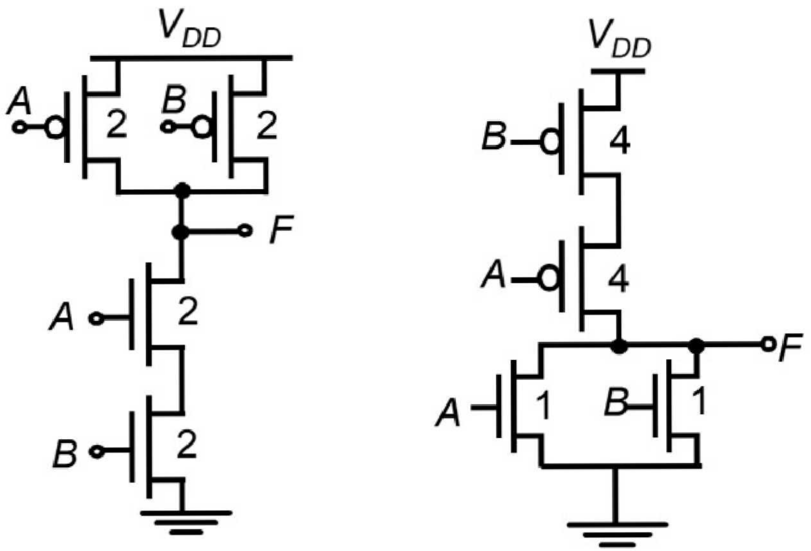
3. APAM toolkit



- ☐ One working chemistry

Need an acceptor chemistry



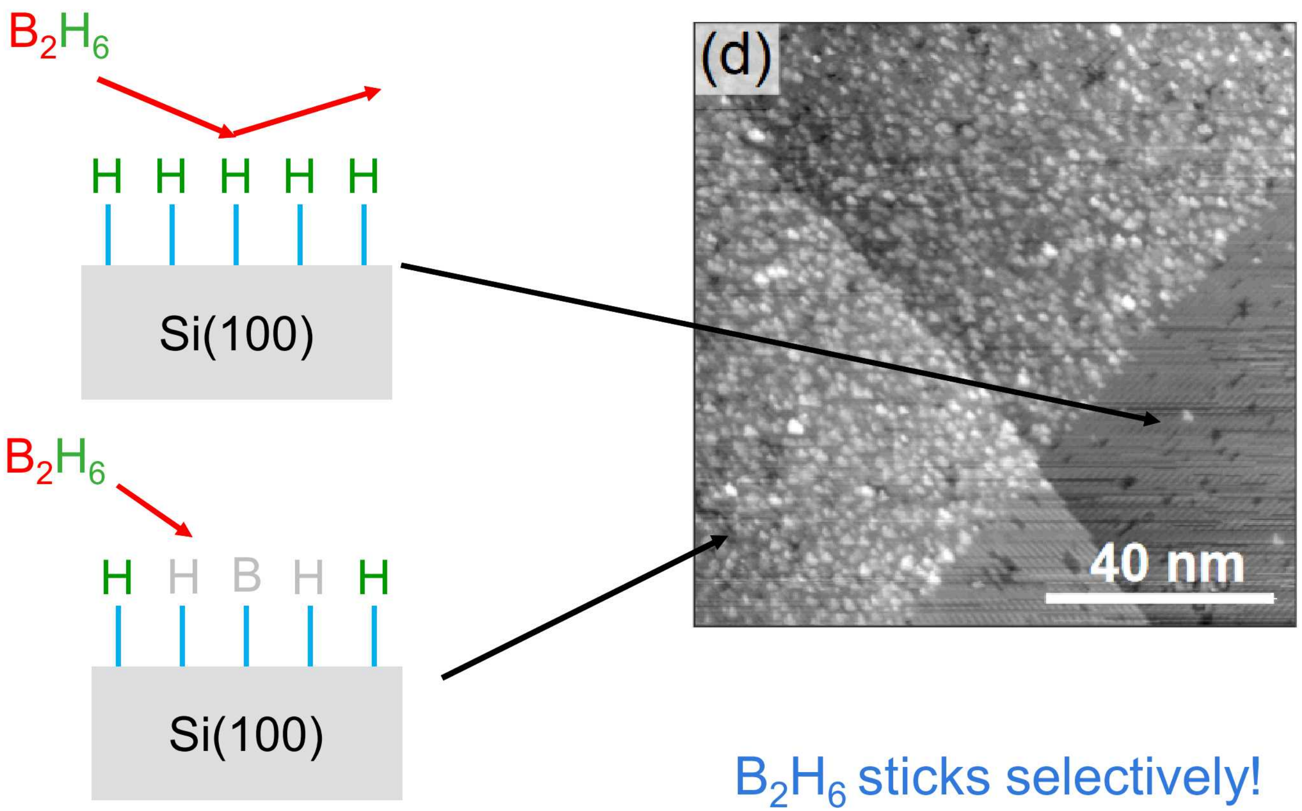


Efficient digital logic requires complementary switches

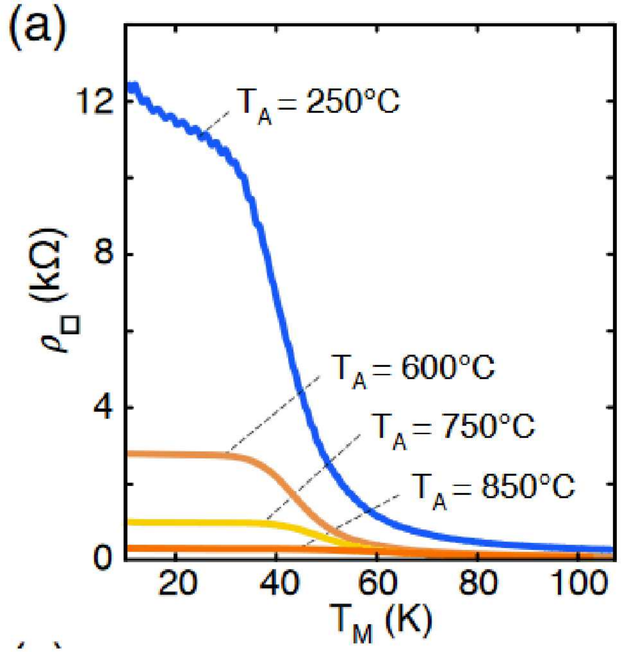
Complementary devices require acceptors.

Diborane provides selective p-type doping

Skeren, arXiv:1912.06188

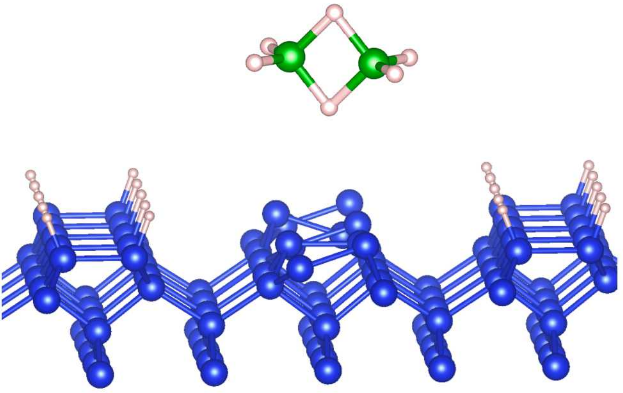


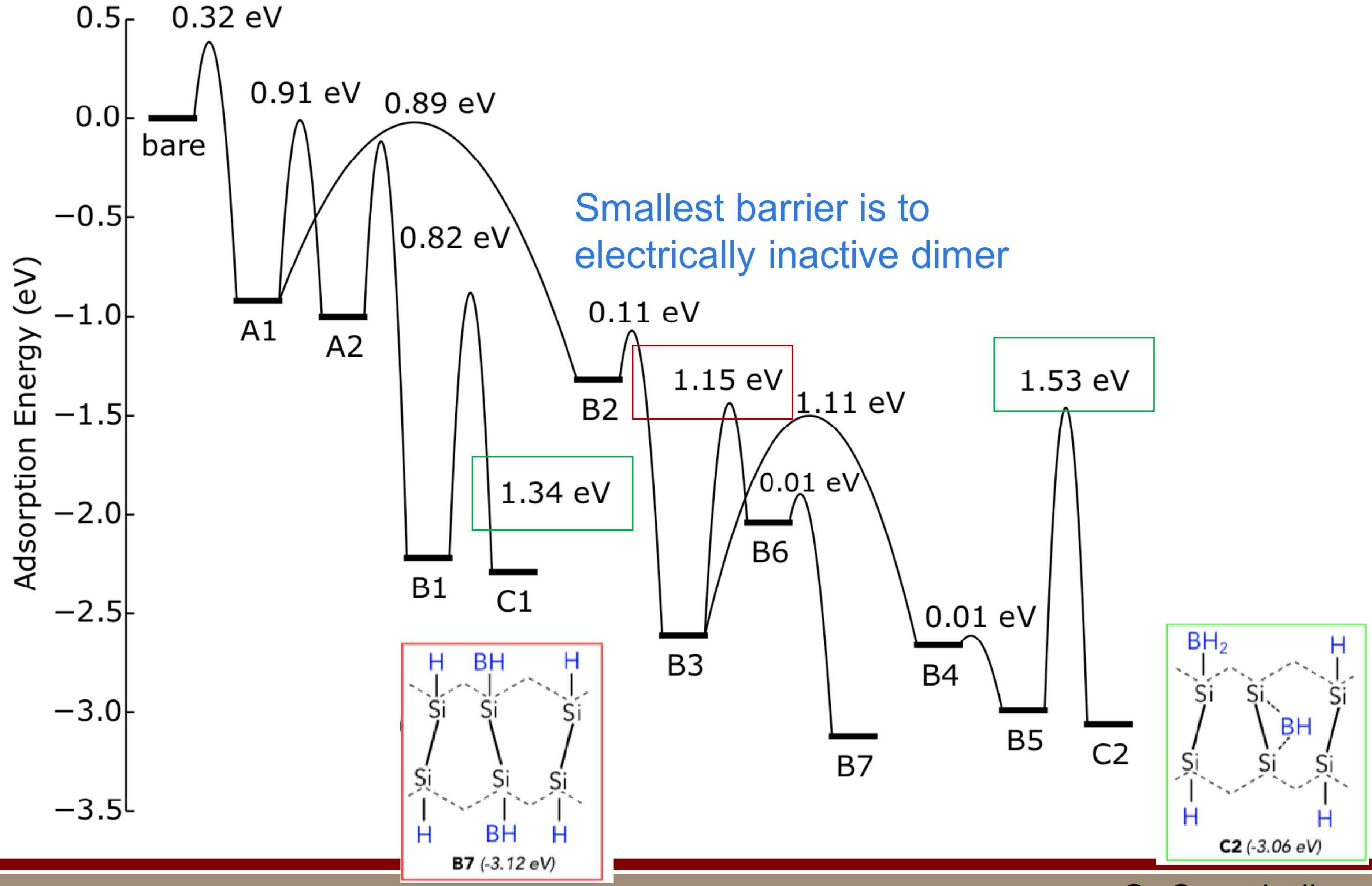
B_2H_6 sticks selectively!



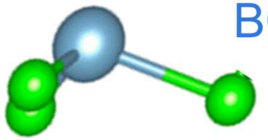
Electrical quality is questionable

Why does diborane have a high resistivity?

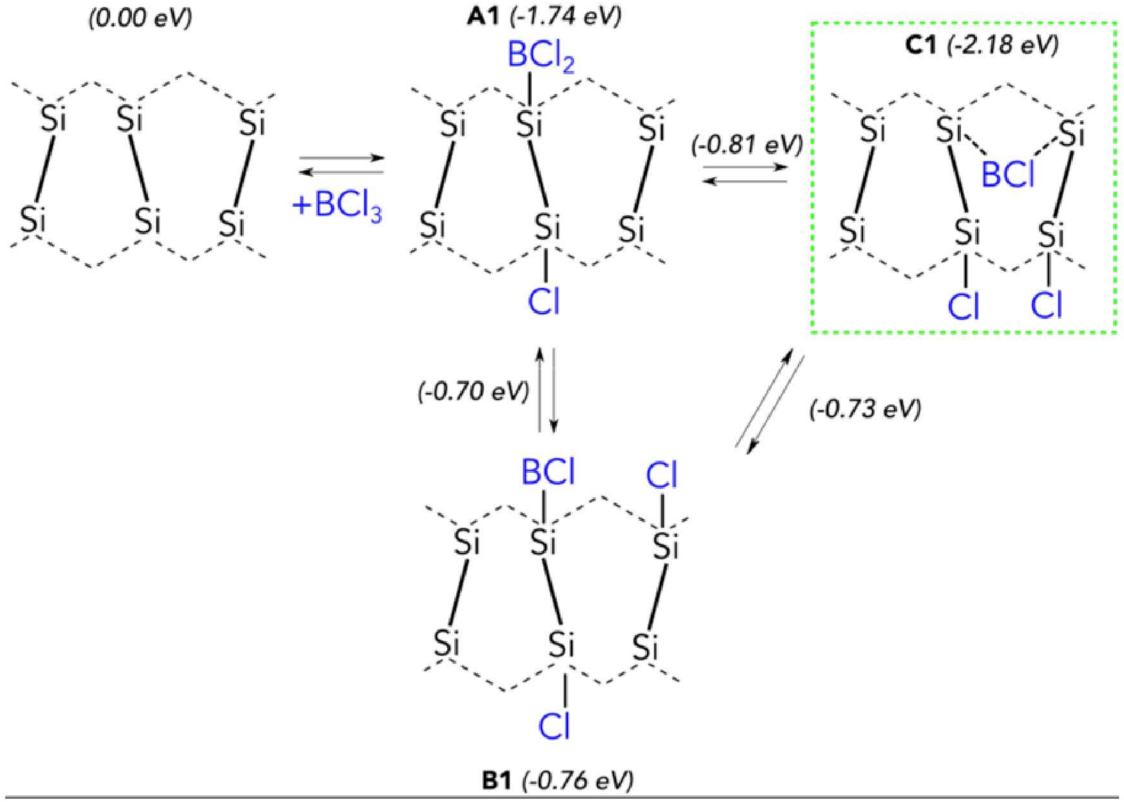


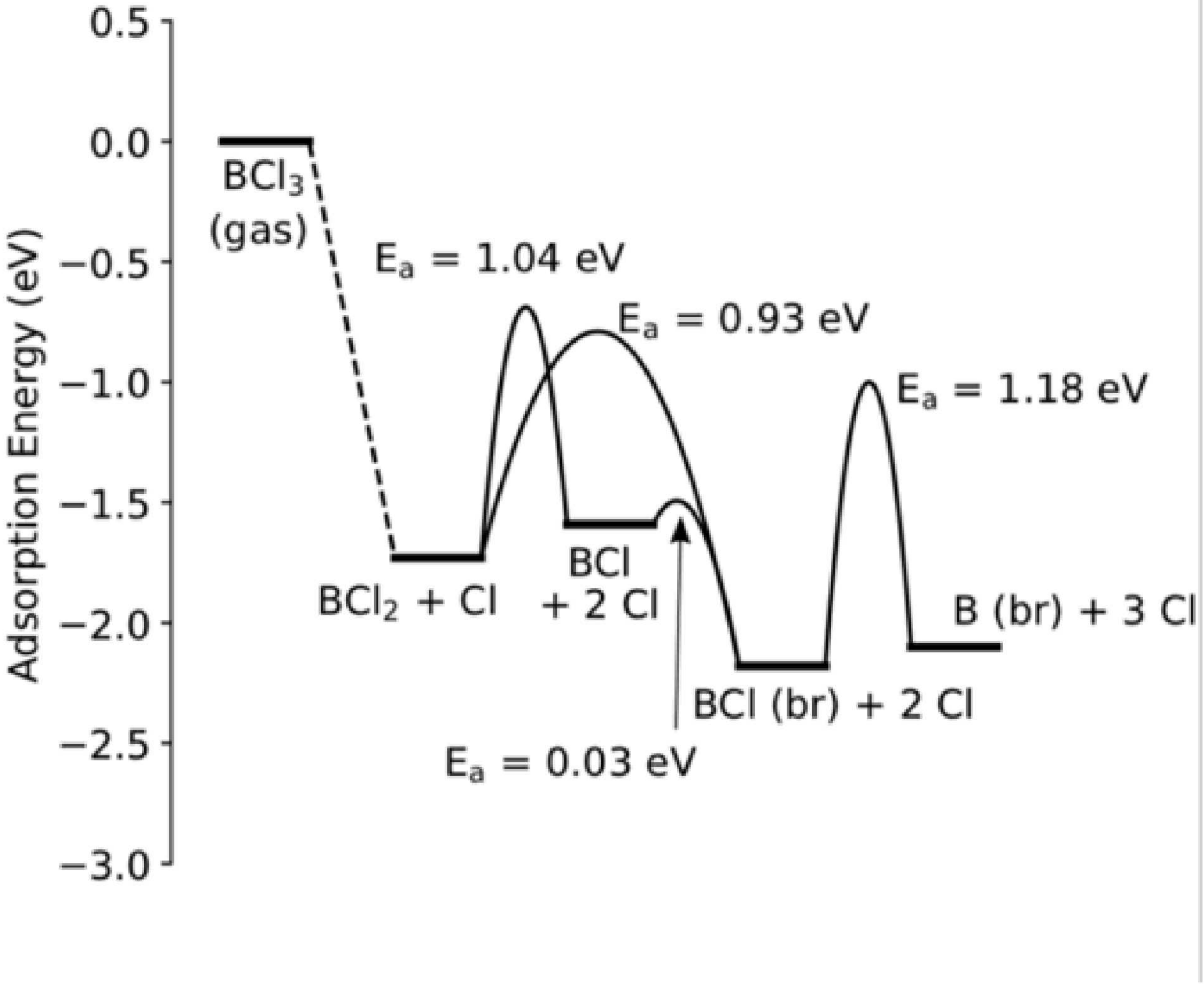


Acceptor chemistry with monomer precursor

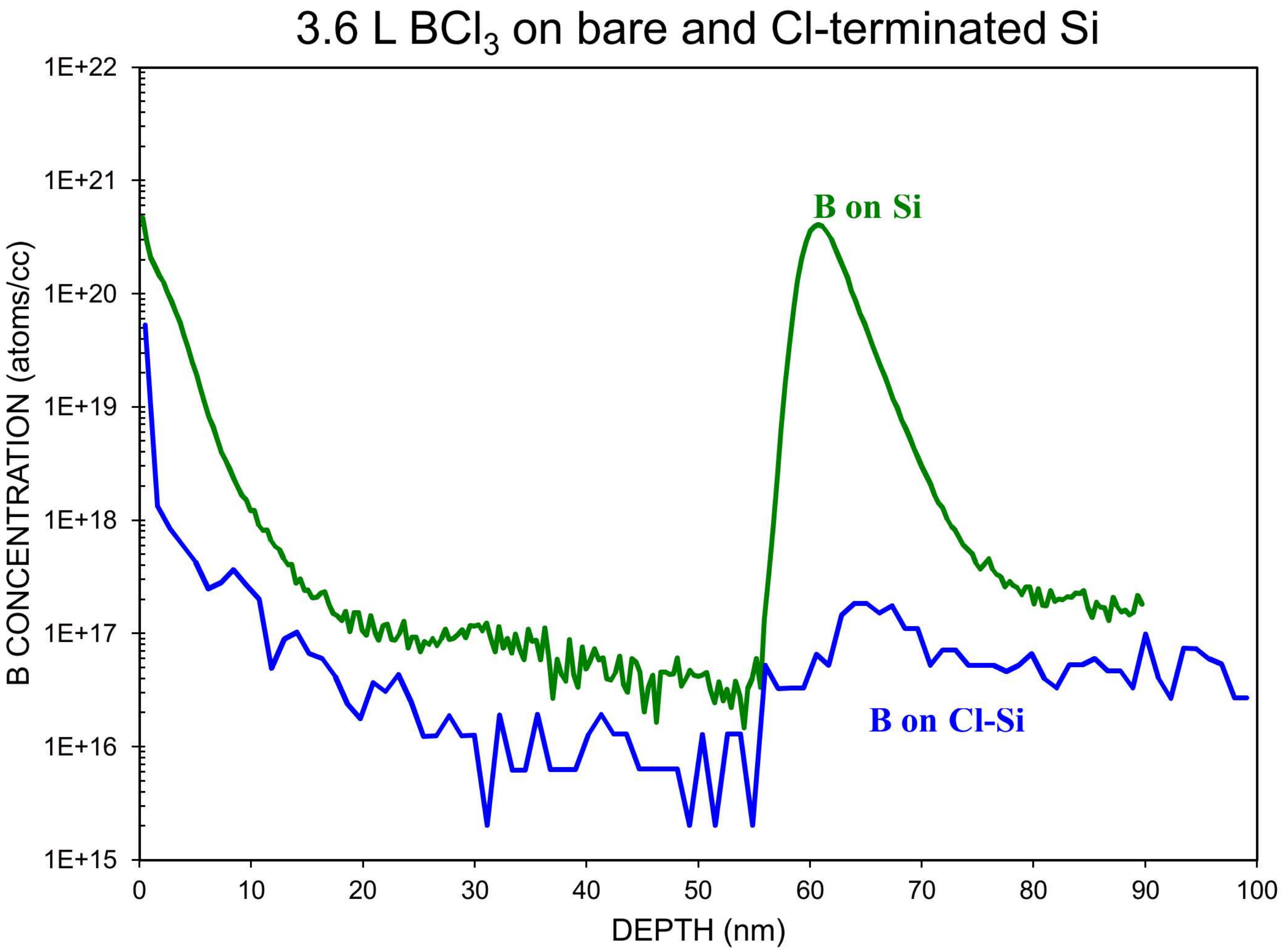


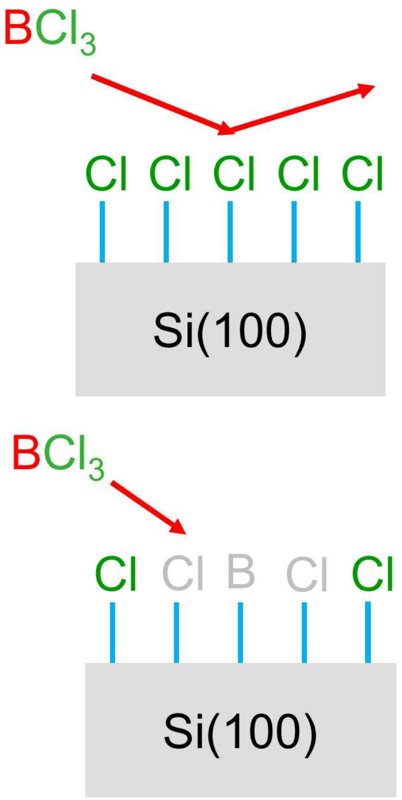
BCl_3 is a monomer, modest barrier



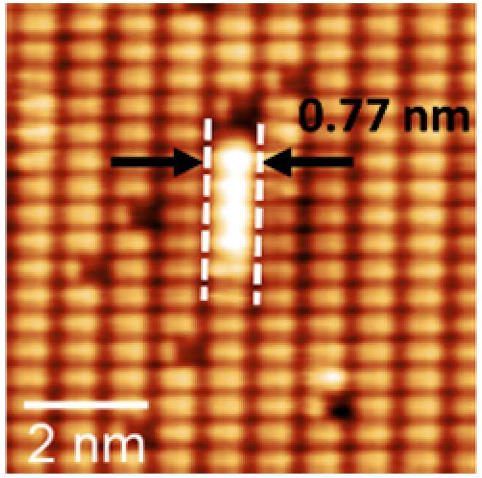


BCl_3 selective to Cl/bare silicon



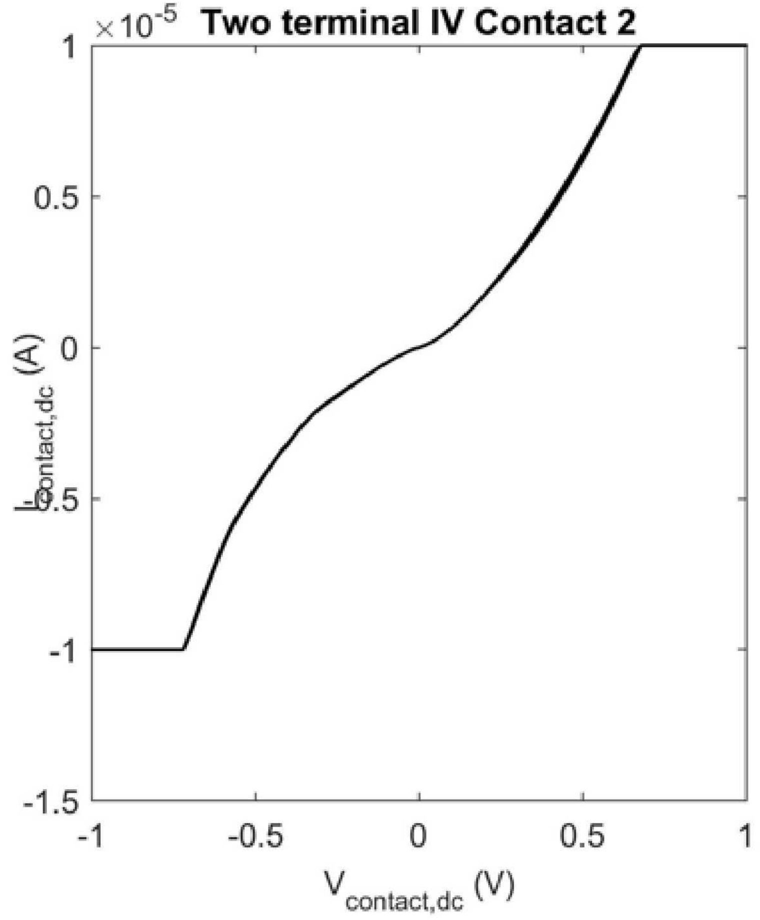


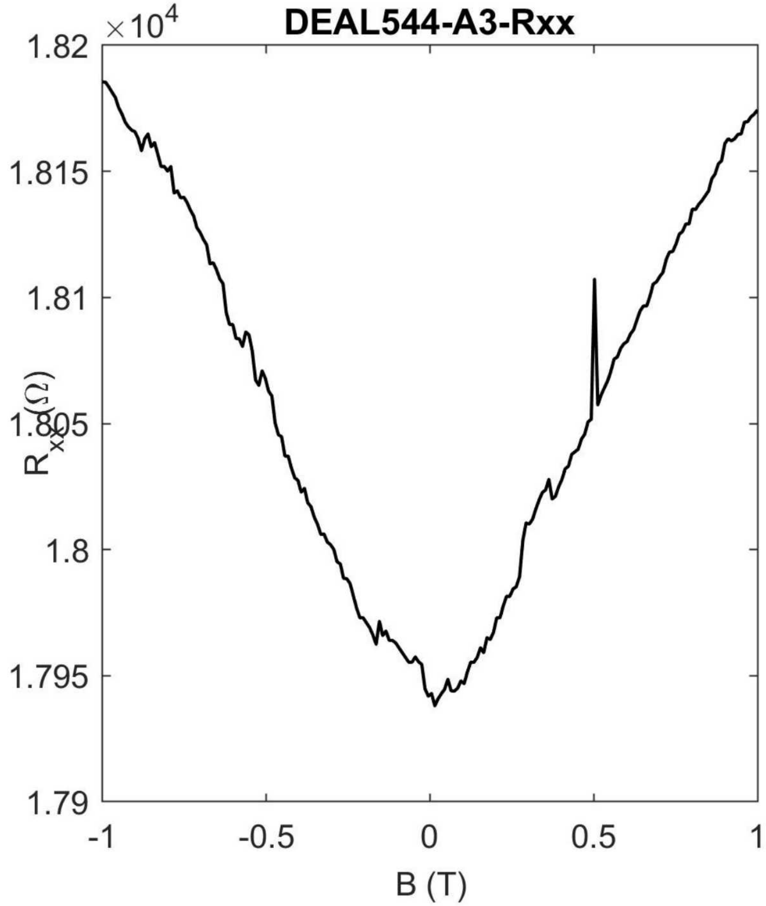
Atomic Precision Patterning



[Dwyer, J. Phys. Chem. A (2019)]

First electrical measurements



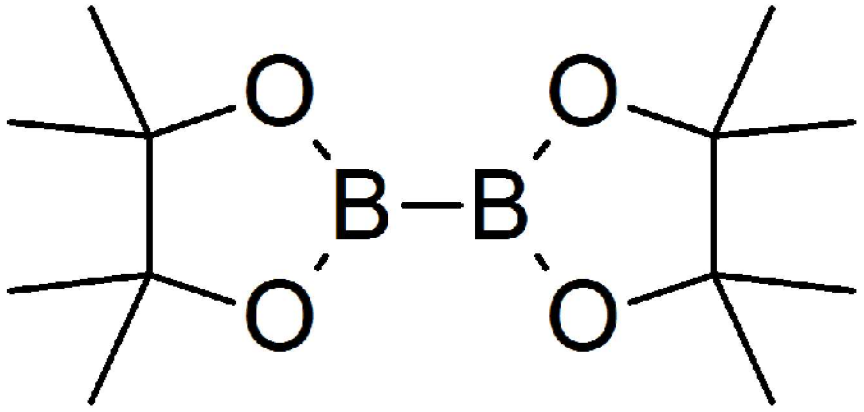


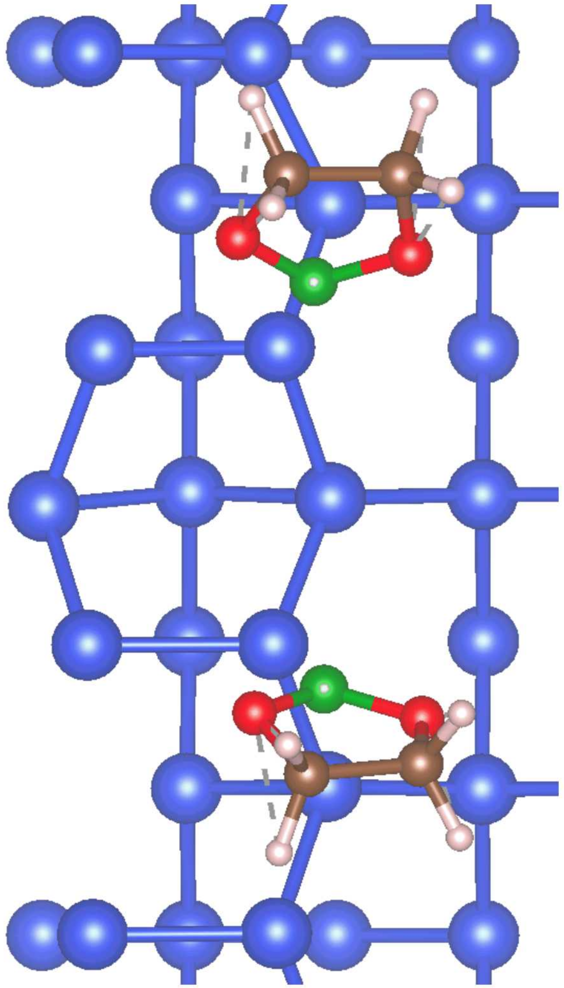
Resistivity of 2.25 kΩ/sq
- 4x worse than phosphine
- 6x better than diborane

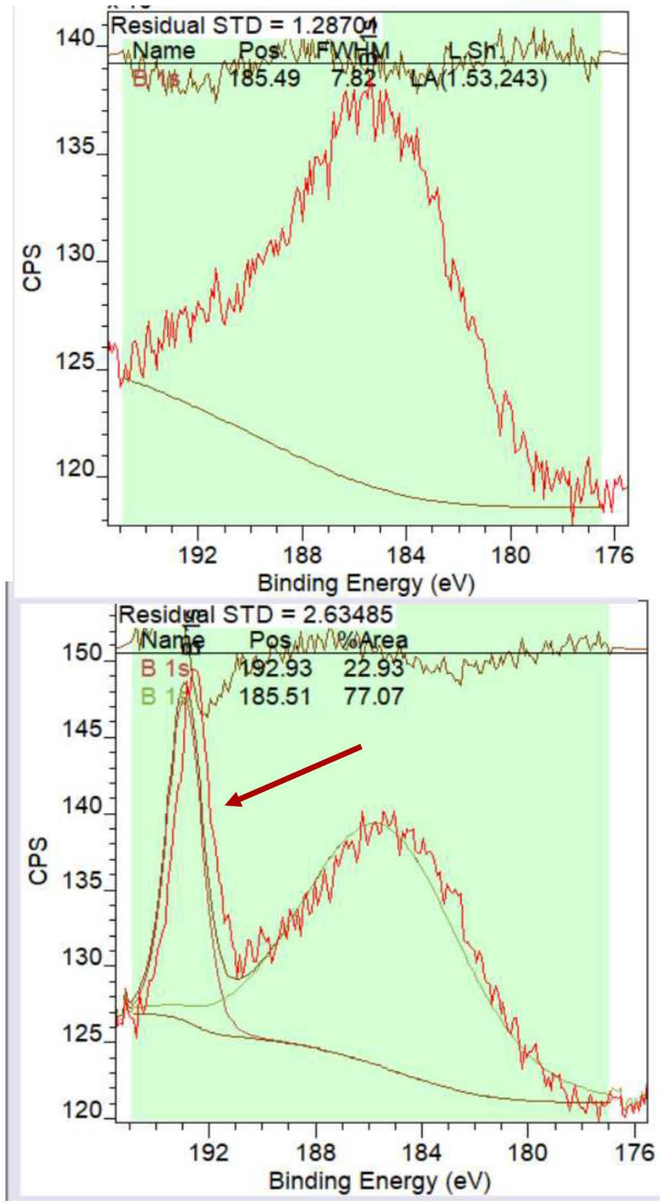
Butera, Dwyer, Campbell, Lu

What's next?

Need wider range of chemistries, but hard to try… try wet chemistry







How do people clean up wet chemistry?

How to get to digital electronics at the atomic scale?

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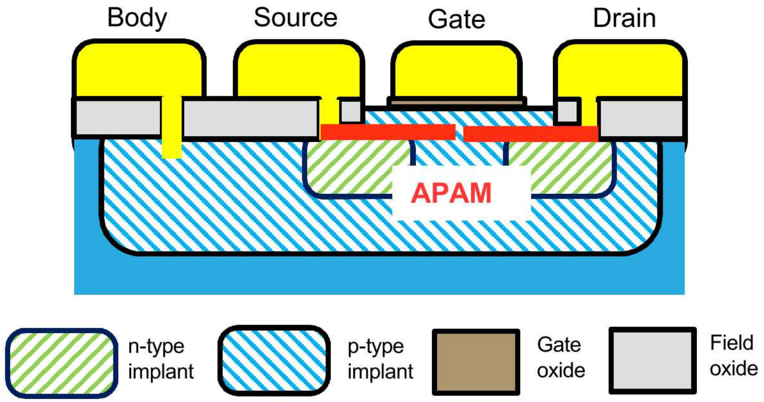
1. APAM devices



- ✓ Surface gated APAM devices
- ✓ Operate at room temperature
- ❑ APAM transistor

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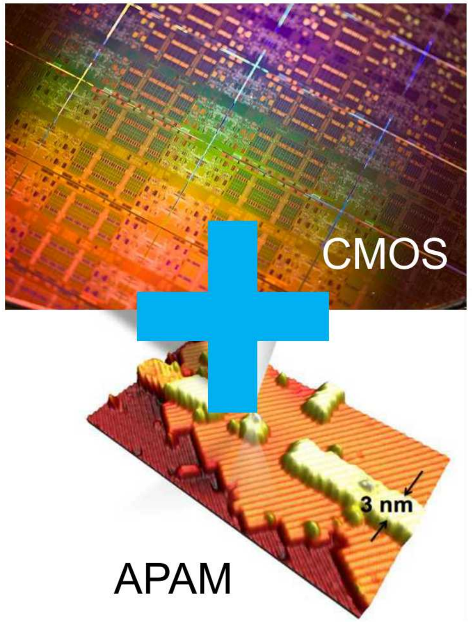
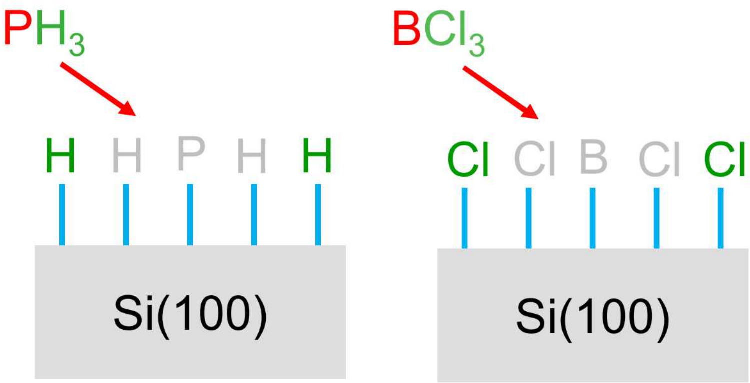


- ✓ Direct integration: wafer-scale APAM litho
- ❑ Wafer-scale APAM process
- ❑ Post-CMOS: Reduced temp. sample prep

3. APAM toolkit



- ✓ Working chemistry with PH_3 / H and BCl_3 / Cl
- ❑ Chemistries for oxides, metal, etching, etc.

Thanks to…

Sandia National Laboratories

Devices	**Modeling**	**Integration**	**Manufacturability**
Lead: Shashank Misra	Lead: Suzey Gao	Lead: David Scrymgeour	Lead: George Wang

Measurement: Lisa Tracy, Tzu-Ming Lu, Albert Grine, David Scrymgeour, Ping Lu, Aaron Katzenmeyer

Microfabrication: David Scrymgeour, Andrew Leenheer, Dan Ward, DeAnna Campbell, Mark Gunter, Phillip Gamache, Sean Smith, Troy England, Andrew Starbuck, Steve Carr, Reza Arghavani

Modeling: Suzey Gao, Denis Mamaluy, Juan P. Mendez, William Lepkowski, Michael Goldflam, Amun Jarzembski, Thomas Beechem, Andrew Baczewski, Quinn Campbell, Steve Young, Peter Schultz

Surface Science: Bob Butera (LPS), Kevin Dwyer (LPS), Andrew Teplyakov (Delaware), Alex Shestopalov (Rochester), Ezra Bussmann, Scott Schmucker, Evan Anderson, Joe Lucero, Jeff Ivie, Fabian Pena, Aaron Katzenmeyer, George Wang, Esther Frederick, Igor Kolesnichenko, David Wheeler, Mike Marshall

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