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Optimal Power Module Design for High Power Density Traction Drive System

Lee Rashkin, Jason Neely, Lee Gill, Jack Flicker, Rachid Darbali-Zamora
Sandia National Laboratories
lrashki@sandia.gov

***Abstract*- This paper describes the design of a very high power density inverter drive module using aggressive high-frequency design methods and multi-objective optimization tools. This work is part of a larger effort to develop electric drive designs with >97% efficiency, power densities of 100 kW/L for the power electronics, and with predicted reliable operation to 300,000 miles. The approach taken in this work is to develop designs that utilize wide band gap devices (SiC or GaN) and ceramic capacitors to enable high-frequency switching and a compact integrated design. The multi-objective optimization is employed to select key parameters for the design.**

Keywords – multi-objective optimization, high power density

I. INTRODUCTION

This work supports research and development to realize next generation electric drive systems with aggressive improvements to electric performance over the current state-of-the-art. Agencies such as the Department of Energy Vehicle Technologies Office (DOE/VTO) have identified performance goals that include 33kW/L electric drive power density, 300,000 miles of operational life, and >97% efficiency [1],[2]. In this work, we focus on the power electronic drive by itself, having the same lifetime and efficiency targets but with a goal of 100 kW/L power density. To meet these goals, new designs must be identified that make use of state-of-the-art and next generation electronic materials and design methods. Designs must exploit synergies between components, for example: converters designed for high frequency switching using wide band gap devices and ceramic capacitors. This project includes the development of design tools that consider the converter volume and performance, and the identification of candidate designs. Early instantiations of the design tools enable co-optimization of the power module and passive elements and provide some design guidance; later instantiations, as part of future work, will enable the co-optimization of inverter and machine. The GOSET toolbox [3] developed by Purdue University is used herein to find the optimal Pareto front and determine the trade spaces for SiC and GaN semiconductor device technologies.

The next section describes the selection of topology, candidate device technologies, and the design tool. Section III describes the electrical loss modeling, and Section IV briefly describes the volume calculation. Preliminary optimization results are then presented as a Pareto Optimal Curve. Finally, some conclusions, and a description of the final manuscript are provided. It is noted that hardware results using a scaled inverter prototype will be included in the final manuscript as well as a description of how the inverter optimization will be modified to co-optimize both the power electronic drive and motor.

II. SYSTEM DESCRIPTION

Several converter topologies were considered including the combined DC-DC⇔DC-AC architecture identified in [4] as well as multi-phase topologies [5], and more exotic configurations [6]. Given the higher projected available battery voltage, the team focused on direct connect DC-AC (no DC-DC boost). Due to the beneficial effect of additional phases on required dc link capacitance and dc link capacitor current ripple [5], the team focused on a 2-level voltage source inverter topology with potential to have more than 3 phases, referred to herein as a *multi-phase inverter*. Fig. 1 shows the selected circuit topology used in the co-optimization problem consisting of a multiphase inverter, DC link capacitor, input inductor, and multiple parasitic terms which vary with component selection and layout.

The design parameters to be included in the optimization are the battery open circuit voltage, V_{in}, the input inductance, L_{in}, link capacitance, C_{link}, number of phases, N_ϕ, switching frequency, f_{sw}, fundamental frequency of the output voltages, ω_r, and the AC filter inductance, L_f, resistance, R_f, and

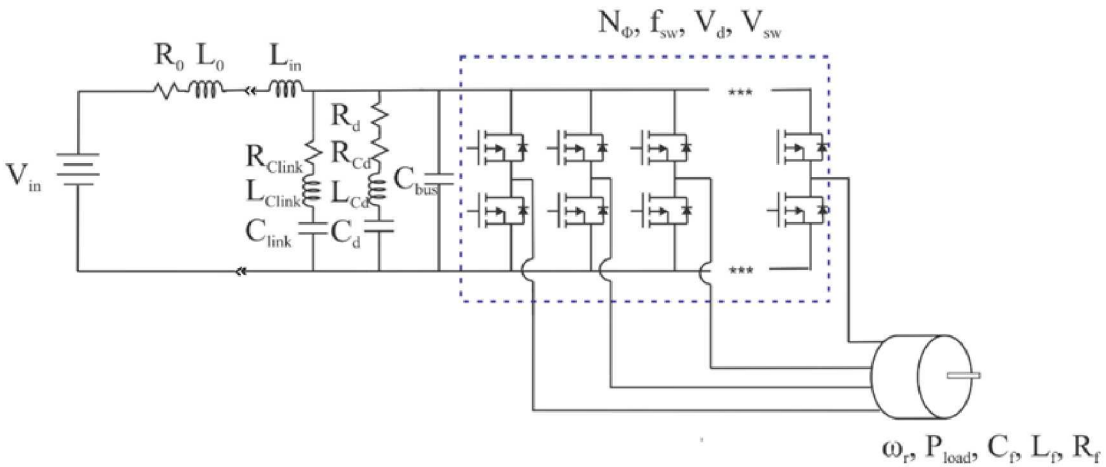

Fig. 1. Circuit topology used in optimization studies.

capacitance, C_f. A MATLAB® script was developed that solved a set of differential equations for the circuit given these parameters, and then post-processed the behavior of voltages and currents in the circuit to determine the volume and losses of the design as well as the voltage and power loss in specified components.

The form factor selected for the principle converter elements is shown in Fig. 2. Therein, the module with devices, conductors, and flat capacitor assembly are packaged together. This approach has several advantages for thermal management and reduction of parasitics, as discussed in [7]. This form factor was used as a basis for the dimensional analysis.

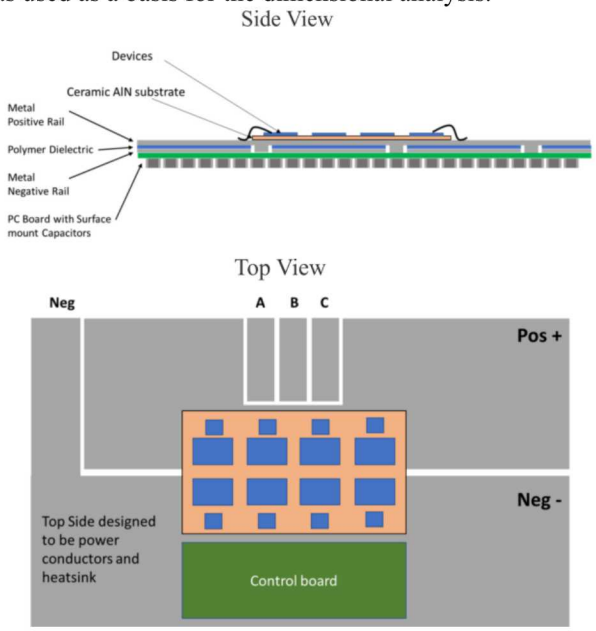

Fig. 2. Candidate Design considers a flat integrated form factor that includes module and DC link capacitor

III. System Loss Modelling

Estimating the power loss of the inverter system is critical towards to evaluating design tradeoffs between both power density and efficiency for different individuals in the design space of the inverter.

A. Resistive Losses

Losses due to resistive elements are modelled as I^2R heat loss. These include series equivelent resistance (ESR) in the filter inductors, ESR in the DC link capacitor, and battery cable resistance. The *on*-resistance of the MOSFET switches and diodes is discussed below.

B. Switching Losses

The switching loss model proposed in [8] is used as the basis of the loss estimation, though slight modifications are adopted in order to apply the model to both SiC and GaN devices. In short, as suggested in [8], the turn-on and turn-off switching losses are calculated based on the charge equivalent representation of the parasitic device parameters, which additionally determines the voltage and/or current rise and fall times.

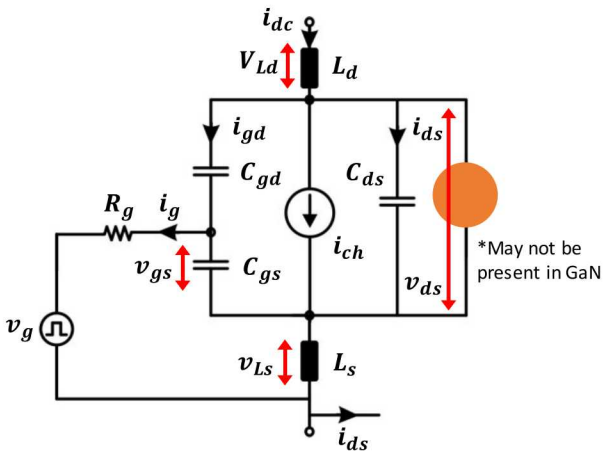

Fig. 3. Linearized semiconductor model with body diode for SiC. The body diode is omitted for GaN HEMT device

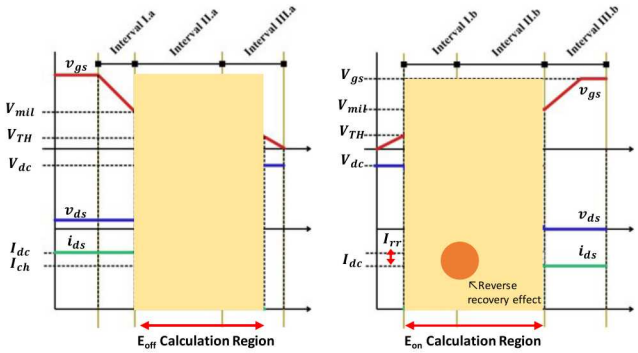

Fig. 4. (Left) turn-off and turn-on (right) gate voltage, v_{gs}, drain-source voltage, v_{ds}, and drain-source current, i_{ds}, waveforms along with the energy loss calculation regions.

Fig.1 shows a generic equivalent circuit model of a semiconductor switch. Note that the model depicted is linearized and includes the parasitic junction capacitances of the device (C_{gs}, C_{gd}, and C_{ds}), internal and external gate resistance (R_g), and the parasitic packaging stray inductance in the source and drain (L_s and L_d). The body diode is also included in the model for the SiC MOSFET. However, such a body diode may not be present for the GaN device, like GaN HEMT and any other types, depending on the physical device structure.

Without presenting the detailed explanation of the mathematical expressions, Fig. 2 shows both the turn-on and turn-off transient voltage and current behavior. Fig.2(a) illustrates that the turn-off switching loss occurs between Interval II.a and Interval III.a whereas Fig.2(b) shows the appropriate turn-on region between Interval I.b and Interval II.b. Additionally, the turn-on and turn-off energy losses can be expressed in (1) and (2) as follows

$$E_{off} = \frac{1}{2}V_{dc}I_{ch}t_{Interval\ II.a} + \frac{1}{2}(V_{dc} + V_{Ld})I_{ch}t_{interval\ III.a} \quad (1)$$

$$E_{on} = \frac{1}{2}(V_{dc} - V_{Ld})(I_{dc} + I_{rr})t_{interval\ I.b} + \frac{1}{2}(V_{dc} - V_{Ld})I_{ds}t_{interval\ II.b} \quad (2)$$

where V_{dc} is the dc voltage across the half-bridge, I_{ds} is the current through the load, I_{ch} is the current through the device channel, Q_{oss} is the equivalent charge stored in each device junction capacitance of C_{oss}, and I_{rr} is the reverse recovery current contribution from the body diode. The detailed mathematical expressions are not presented in this paper; the goal here is to provide a description of the methodology of the switching loss estimation and comparison between different device types.

Eqn (2) is written as an approximated expression, though there is a significant energy loss mechanism from the body diode of the other switch in the half-bridge, undergoing reverse recovery phase. Additional E_{rr}, which is energy lost during reverse recovery is calculated more accurately, and a modified equation is used for the switching loss calculation of the SiC device. For the GaN HEMT device in consideration, E_rr is ignored as the body diode is not physically present in the device structure.

To simplify the problem statement of the comparison between SiC and GaN in terms of switching losses, commercially available parts were selected and required parameters were extracted from the datasheets [9] and [10]. Table 1 shows the comparison between the SiC and GaN devices selected for the design tradeoff studies. Fig. 5 shows the total switching losses for GaN and SiC using this method extrapolated to higher power devices. Fits to the surfaces for E_{Ton} and E_{Toff} for each device type were constructed for faster computation.

C. *Conduction Losses*

For conduction losses of the switches, conduction resistance (Ron) was calculated for SiC and GaN vertical planar MOSFETs using the formalism and equations for intrinsic layer resistivity described in [11].

For systems with SiC switches, a proposed SiC 1200V MOSFET with doping and layer thicknesses necessary to approximate the static operation of a commercially available device (CREE C2M0080120D [12]) was modelled to find on-state resistivity. Unfortunately, no vertical planar MOSFET composed of Gallium Nitride (GaN) is commercially avialable. Therefore a modelled device was used. This modelled GaN MOSFET had an architecture similar to the SiC MOSFET, namely the doping levels and physical demensions of the gate, channel, and oxide layers. However, to account for the differences in GaN critical field and mobility, the drift layer thickness was scaled to achieve a similar 1200V hold-off to the SiC MOSFET.

Due to GaN's high critical electric field compared to SiC (3.45 eV [13] vs. 3.23 eV [14]), the drift thickness for a GaN device for a given breakdown voltage is smaller, yielding decreased conduction losses (this is reflected in the high unipolar figure of merit for GaN compared to SiC [15]). For a similar MOSFET structure, GaN exibits 54% lower Ron than SiC (Fig. 5). It should be noted that this comparison is not optimized for a GaN MOSFET and a truly optimizaed GaN MOSFET would most likely have even lower conduction losses compared to a SiC MOSFET.

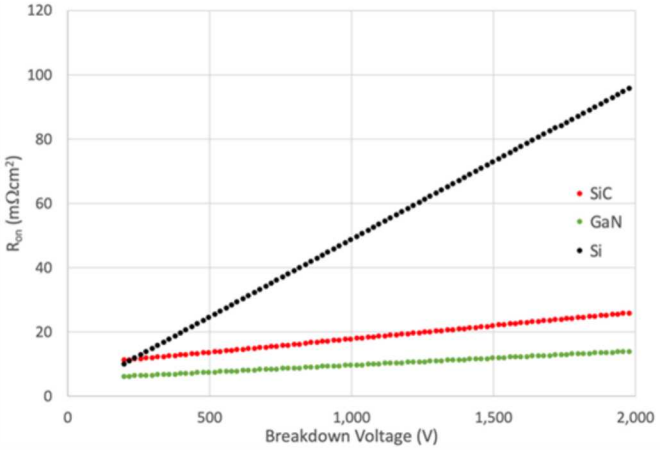

Fig. 5. Ron vs. MOSFET breakdown voltage for vertical planar MOSFET for Si (black), SiC (red) and GaN (green). Compared to SIC, GaN has a 54% lower value for Ron.

TABLE I
CHARACTERISTIC COMPARISON BETWEEN SELECTED SIC AND GAN DEVICE [9], [10]

Comparison	GaN	SiC
Manufacturer	GaN Systems	CREE
Model #	GS66516B	C2M0080120D
Voltage	650 V	1200 V
Current	60 A	36 A
$R_{ds(on)}$	25 mΩ	80 mΩ

IV. COMPONENT VOLUME MODELLING

A. *Module and Capacitor Sizing*

The power module and capacitor are highly integrated in a flat form factor design.

Given the number of phases, the voltage rating, the peak current and current densities of the devices, the value of DC link capacitance, the selection of capacitor product, and a desired aspect ratio (length to width ratio) for the assembly, the dimensions of the integrated assembly are computed.

The analysis assumes the devices are mounted to a ceramic substrate; two flat bus-plates with dielectric film between them are mounted below; and the DC link capacitor is realized as ceramic capacitors soldered to a printed circuit board (PCB) that connects to the bus plates at several locations (see Fig. 2).

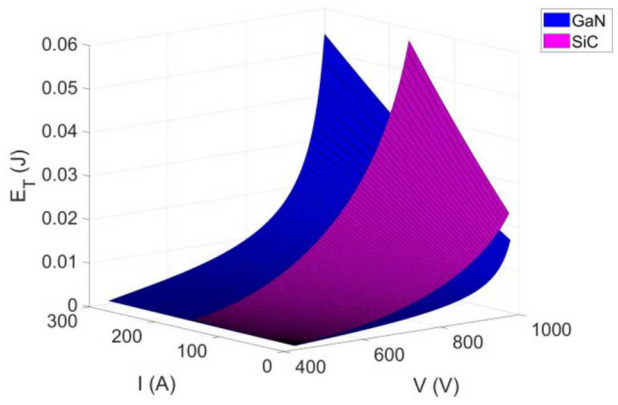

Fig. 5. Total switching losses for GaN and SiC as a function of input voltage and operational current.

From the rated voltage, the required film thickness is calculated, and component spacings are computed based on required creepage. Based on component count and spacing, device layout is then determined to achieve the desired aspect ratio. This is done for the power devices and ceramic capacitors. The volume of the power module is simply the product of substrate length, substrate width, and total thickness (including substrate and device height). The volume of the capacitor is similary computed as the product of the PCB length, PCB width, and thickness (including bus plates, dielectric film, PCB thickness, and capacitor height).

The design assumes a cold plate bonded to the ceramic plate through a cut-out in the capacitor (not illustrated); an approach to estimating the volume of the cold plate is discussed in subsection G.

B. DC Inductor Sizing

The design of an inductor, which includes the size, shape, material type, number of turns, and determining other relevant magnetic characteristics is performed based on the guidelines given in [16]. Such a magnetic design approach is a simplified method to constructing an optimum, dc carrying inductor without relying on trial and error or repetitive design procedures. In order to limit the number of design variables, the magnetic core shape was fixed to an exclusively toroidal shape. Moreover, the material selections are limited to power core, such as Kool Mμ, High Flux, MPP, etc offered through Magnetics Inc.

Among several optimum magnetic design approaches, the A_p methodology, also known as the area product approach is used to design inductors. The area product approach for dc inductors relates several desired electrical characteristics to a core geometrical size equation shown in (3) where K_u is the window utilization facotr, J is the current density expressed in amperes per area [A/cm^2], B_m is the flux density in Tesla [T], L is the inductance, and I is the current through the inductor. This equation calculates the required energy handling capability of a core, a factor that helps the designers select appropriate core size. This ultimately provides a valuable figure of merit for not only the design parameters, but also good understanding of what the optimum magnetic design will look like based on the catalog of available core sizes.

$$A_{p,dc} = \frac{L \cdot I^2 (10^4)}{K_u \cdot B_m \cdot J} [\text{cm}^4] \tag{3}$$

C. Filter Inductor Sizing

The filter inductor sizing is based on the ac inductor design, which the design guidelines are also provided in [16]. Due to the lack of dc flux, the area product equation, for ac inductor is now expressed in (4).

$$A_{p,ac} = \frac{P_t \cdot (10^4)}{K_f \cdot K_u \cdot B_{ac} \cdot J \cdot f} [\text{cm}^4] \tag{4}$$

where P_t is the apparent power in watts, K_u is the window utilization factor, K_f is the waveform coefficient, 4.0 for square wave and 4.44 for sine wave, is B_{ac} the operating flux density, f is the operating frequency, and J is the current density. The units of the parameters are the same as the $A_{p,dc}$.

D. Cold Plate Sizing

The cold plate sizing was determined based on [17] using the equation:

$$V_{cool} = 10^{(-1.6(\log(R_{th})+3)+3))} \tag{5}$$

where V_{cool} is the cooling volume in cubic inches and R_{th} is the desired thermal resistance. R_{th} is determined by the equation:

$$R_{th} = \frac{(T_c - T_a)}{P} \tag{6}$$

where T_a is the ambient temperature of 25°C, T_c is the maximum junction temperature, set to 110°C for SiC and 150°C for GaN, and P is the total loss in the module and capacitor board.

V. GENETIC OPTIMIZATION

One strategy for generating design guidance and optimal designs is a global multi-objective optimization. In this strategy, with the definition of one or more performance metrics, components are simulated together and their performance is measured and compared. For multi-objective optimization, the team used the Genetic Optimization System Engineering Tool (GOSET) developed by Purdue University [3]. This MATLAB® based software package consists of several scripts for implementing and solving a genetic algorithm optimization problem. The genetic algorithm is a probabilistic method for optimizing multi-input systems with nonconvex solution spaces using the principles of genetics and user defined fitness functions. GOSET allows for multiple fitness functions to be co-optimized into a Pareto front. To set up the optimization, circuit schematic and physical layout must be partially defined, and the dimensions of and between components, thicknesses of insulators, lengths of conductors, and other physical dimensions, must be formulated and linked to the schematic definition in order to compute a volume and evaluate the circuit/system performance using a dynamic simulation. Additionally, performance constraints on the allowable DC capacitor voltage ripple, AC voltage noise, and battery current ripple were applied to limit the chosen design to feasible implimentations.

The genetic optimization was run on 99 individuals over 100 generations for systems using SiC devices and GaN devices. The resulting Pareto fronts are shown in Fig. 6. These results show that GaN solutions are closer to the 100 kW/L power density target, with a solution that has a 74.949 kW/L at 89.27% efficiency. This solution is for a three phase inverter with an input voltage of 915.42 V and a switching frequency of 343 kHz. The capacitor board uses 320 ceramic capacitors to achieve the required capacitance. This is still below the

targeted power density and efficiency for the application, so it is useful to look at the component volumes and losses shown in table II.

From these results it is clear that most of the volume and loss is contained in the filter inductors. The cooling system takes up the second most volume while the module contributes the second most loss.

TABLE II
COMPONENT VOLUMES AND LOSSES

Component	Volume (L)	Volume %	Loss (kW)	Loss %
Module	0.01	0.5557	0.3867	23.9519
Capacitor	0.2079	11.5969	0.0001	0.0082
Input Inductor	0	0	0	0
Filter Inductor	1.5116	84.331	1.2278	76.0399
Cooling	0.63	3.5165	N/A	N/A

Based on these results, it is clear that in order to make the power density and efficiency targets it is necessary to reduce the size and loss in the filter inductors.

VI. CONCLUSIONS

In this paper, a genetic algorithm based procedure was used to design a motor drive while optimizing for power density and efficiency. The objective is to identify a design for a 100 kW inverter that meets the target performance of 100 kW/L and 97% conversion efficiency. The design code was run using both SiC and GaN based semiconductor devices. The results fell short of the power density target of 100 kW/L, but it can be seen that improving the sizing and losses in the AC filter inductors through new materials and geometeries is the best way to meet those targets.

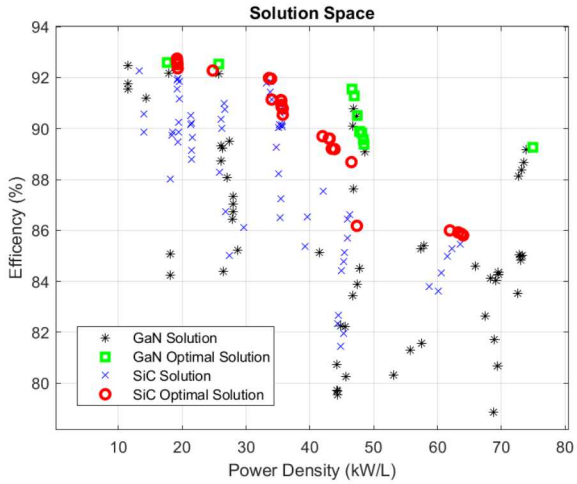

Fig. 6. Comparison between Pareto optimal frontiers for SiC and GaN

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