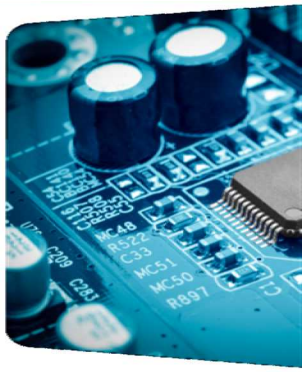
SAND2020-4457C







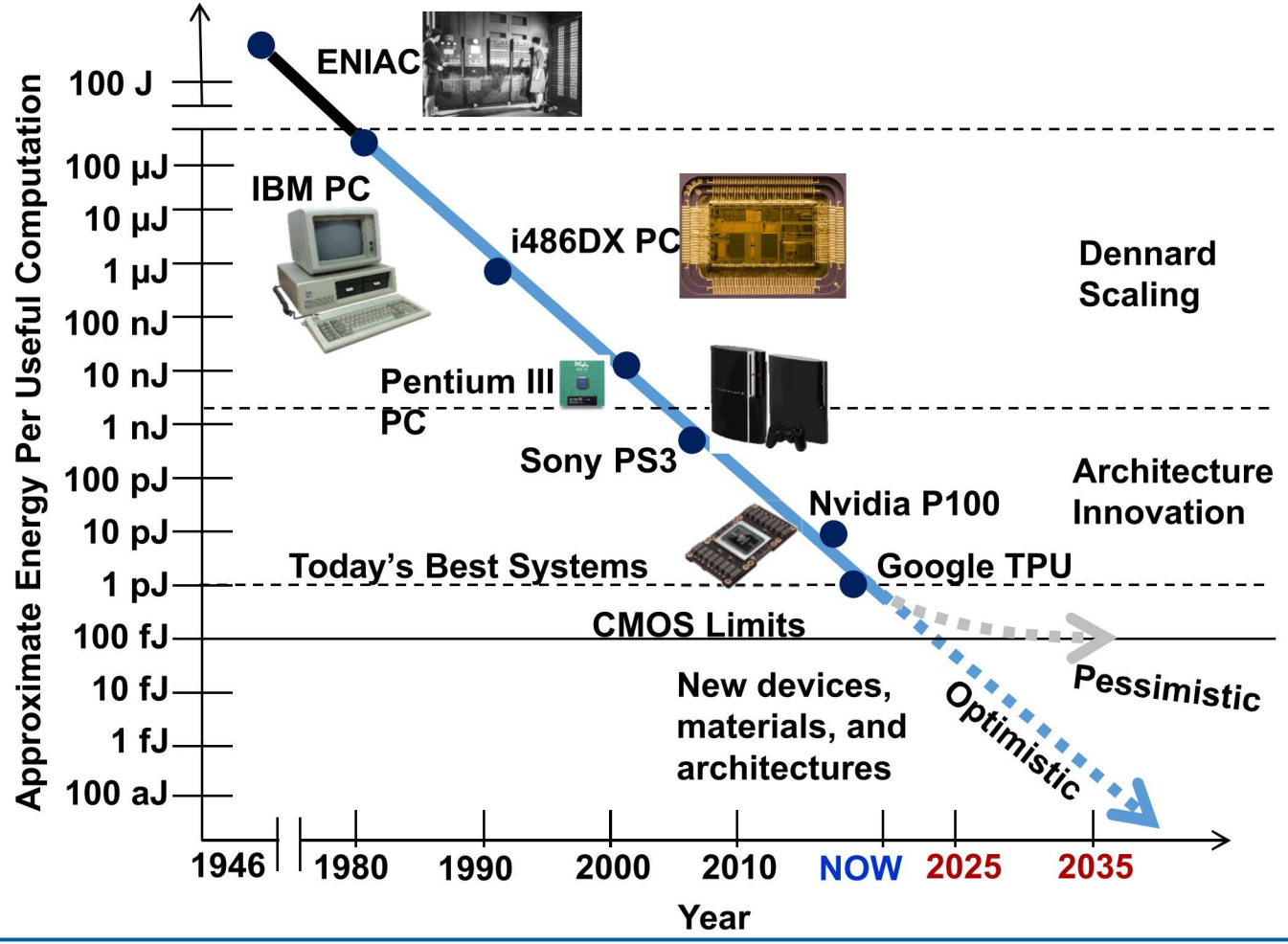
# Beyond CMOS
## & Emerging Research Materials
# IRDS Panel, IEDM 2020

*December 8, 2020*

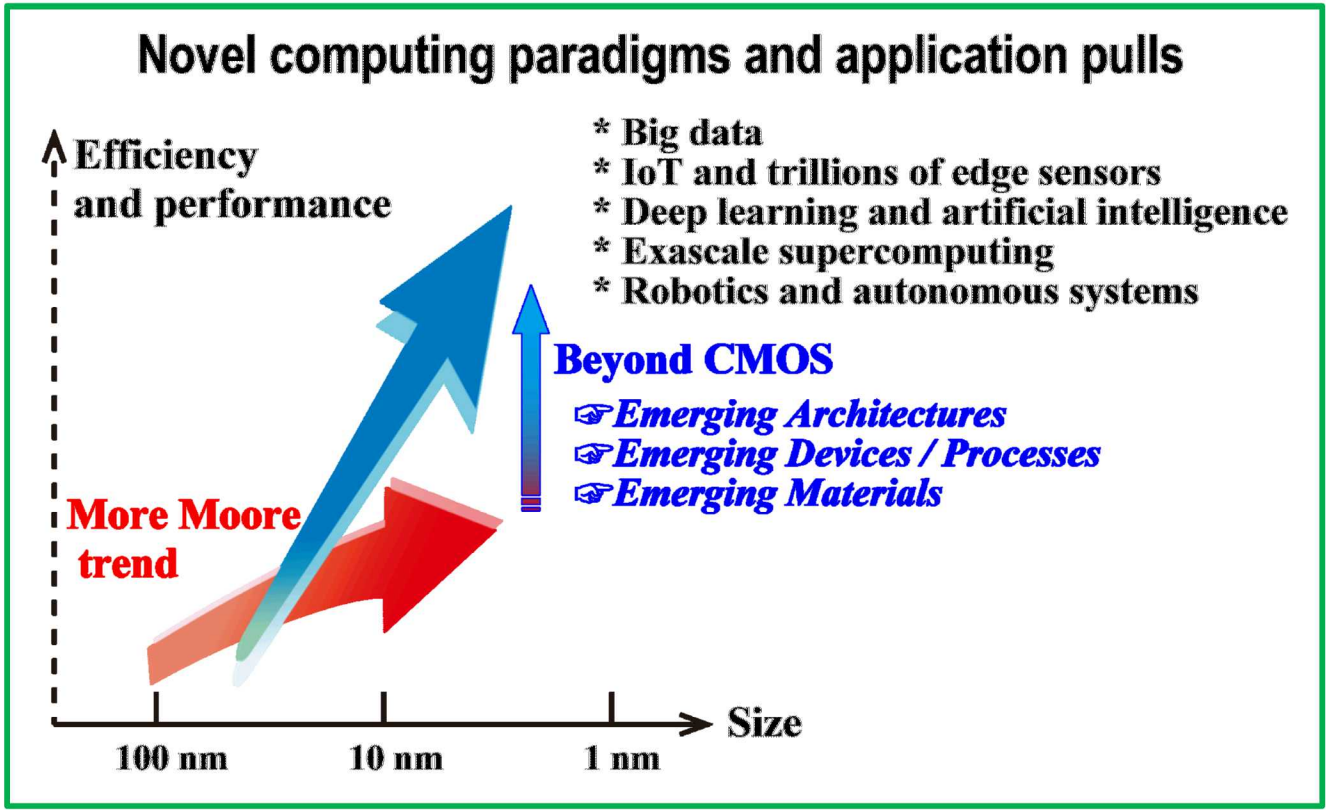
*Presented by Matthew Marinella, Sandia National Labs*



Sandia National Laboratories is a multimission laboratory managed and operated by National Technology & Engineering Solutions of Sandia, LLC, a wholly owned subsidiary of Honeywell International Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA0003525


Approximate Energy Per Useful Computation
100 J
100 µJ
10 µJ
1 µJ
100 nJ
10 nJ
1 nJ
100 pJ
10 pJ
1 pJ
100 fJ
10 fJ
1 fJ
100 aJ
ENIAC
IBM PC
i486DX PC
Pentium III PC
Sony PS3
Nvidia P100
Google TPU
Today's Best Systems
CMOS Limits
Dennard Scaling
Architecture Innovation
New devices, materials, and architectures
Optimistic
Pessimistic
1946
1980
1990
2000
2010
NOW
2025
2035
Year

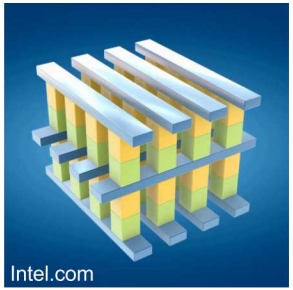
# Objective of the Beyond CMOS (BC) Chapter



# Emerging Memory Devices

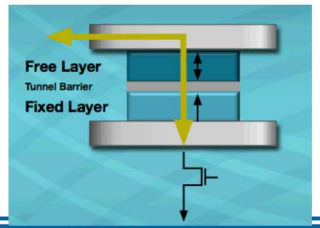
- Memory
  - Volatile
    - SRAM
    - DRAM
      - Stand-alone
      - Embedded
  - Nonvolatile
    - Baseline
      - Flash
        - NOR
        - NAND
    - Prototypical
      - FeRAM
      - MRAM
      - PCM
      - STT-RAM
      - ReRAM
    - Emerging
      - Novel Magnetic Memory
      - Ferroelectric Memory
        - FeFET
        - FTJ
      - OxRAM
      - CBRAM
      - Macromolecular Memory
      - Mott Memory
      - Massive Storage Devices

**Storage Class Memory**



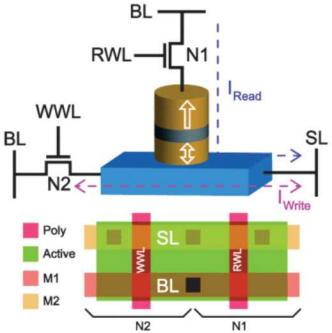

**Successfully tracked and transferred to More Moore**

**STT-MRAM**



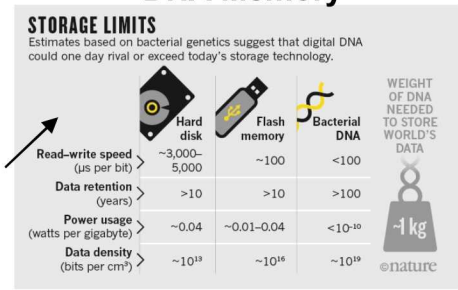

Everspin.com

**New for 2019: SOT Memory**




Z. Wang EDL 39, 2018

**DNA Memory**




Nature.com

# Logic and Information Processing Devices

State variable

Non-charge

Charge

Transistor laser

DWL

Magnetoelectric

NML

Topological insulator

Spin wave

Excitonic

TFET

2D Channel FET

SpinFET

CNT FET

Neg-$C_g$ FET

Si FET

NW FET

Mott FET

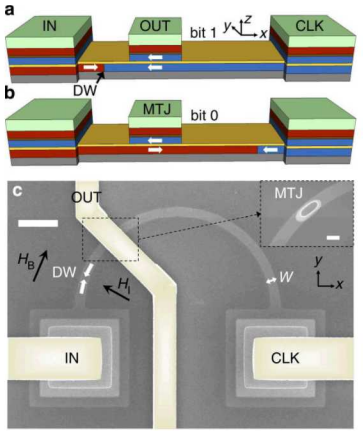
NEMS

Conventional

Novel

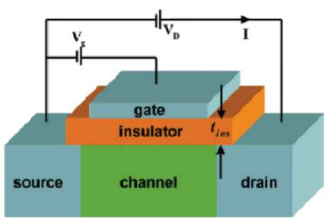
Structure /materials

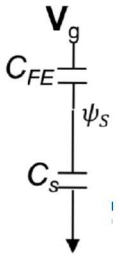
**New in 2019: Domain Wall Logic**




J.A. Incorvia et al, Nature Comm 7, 2016

**Negative Capacitance FET**



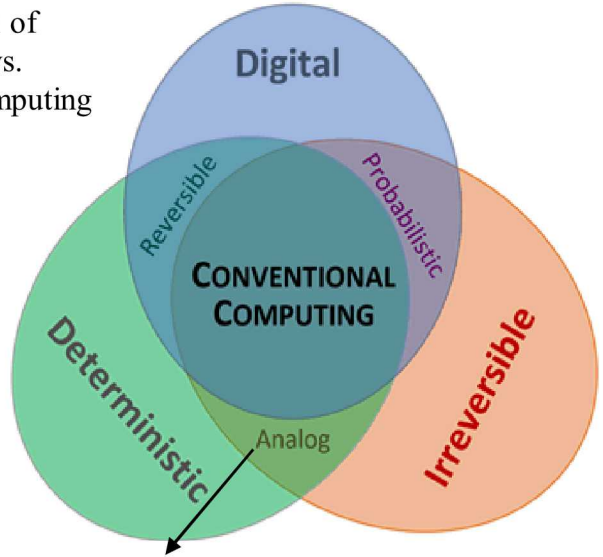



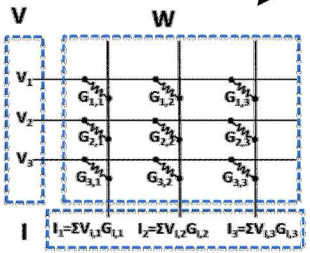

Wong and Salahuddin, TED 2019

# Emerging Device-Architecture Interaction Section

- 1. Introduction
- 2. Analog Computing
  - 2.1. Crossbar-Based Computing Architectures
  - 2.2. Neural-Inspired Computing
  - 2.3. Computing with Dynamical Systems
  - 2.4. Analog Memory & Compute Devices
- 3. Probabilistic Circuits
  - 3.1. Device Technologies for Random Bit Generation
  - 3.2 Probabilistic (p)-bit Logic
- 4. Reversible Computing
- 5. Device-Architecture Interaction: Conclusions/ Recommendations

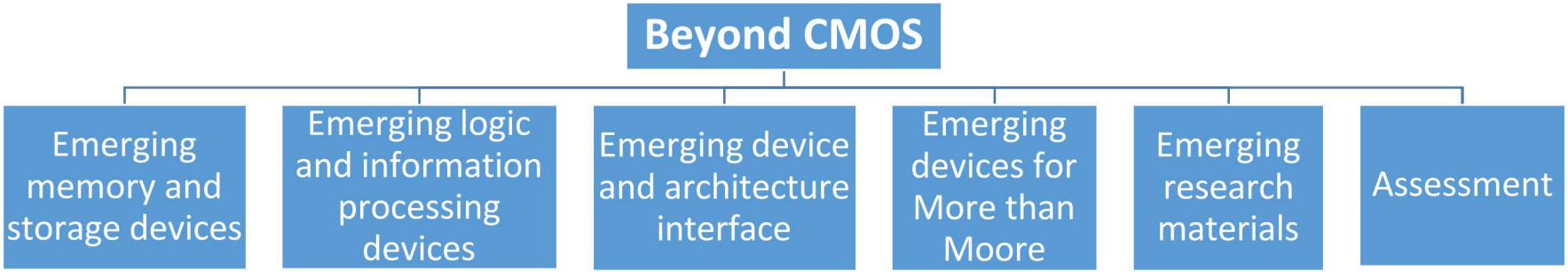
Categorization of conventional vs. alternative computing paradigms



# Extra Slides

# 2019 BC Chapter Structure




- Memory devices
- Selector devices
- Storage class memory

- CMOS extension
- Beyond-CMOS charge-based
- Beyond-CMOS non-charge-based

- Map emerging architecture to suitable devices
- Define FOMs and key challenges

- Emerging devices for hardware security

- Emerging materials for memory and logic
- Heterogeneous integration and packaging
- Modeling and simulation

- Define criteria
- Based on the quantitative benchmarking reported by NRI

# Beyond CMOS Team Members (Partial)

| Member Name | Organization | Region |
|---|---|---|
| Akira Fujiwara | NTT Corp. | Japan |
| An Chen | IBM/SRC | USA |
| Erik DeBenedictis | Sandia | USA |
| Ferdinand Peper | NICT | Japan |
| Geoffrey Burr | IBM | USA |
| Hiroyuki Akinaga | AIST | Japan |
| Kiyoshi Kawabata | Renesas Electronics Corporation | Japan |
| Koichi Matsumoto | Sony Semiconductor Solutions | Japan |
| Masami Hane | Renesas Electronics Corporation | Japan |
| Matt Marinella | Sandia | USA |
| Michael Frank | Sandia | USA |
| Norikatsu Takaura | Hitachi, Ltd. | Japan |
| Paul Franzon | NCSU | USA |

| Member Name | Organization | Region |
|---|---|---|
| Sapan Agarwal | Sandia | USA |
| Satoshi Kamiyama | Tokyo Electron Limited | Japan |
| Scott Holmes | BAH | USA |
| Shamik Das | MITRE | USA |
| Shashi Paul | De Montfort University | Europe |
| Shinichi Takagi | University of Tokyo | Japan |
| Shintaro Sato | Fujitsu Lab | Japan |
| Takahiro Shinada | Tohoku University | Japan |
| Tetsuo Endoh | Tohoku University | Japan |
| Titash Rakshit | Samsung | USA |
| Tohru Tsuruoka | NIMS | Japan |
| Toshiro Hiramoto | University of Tokyo | Japan |
| Wilman Tsai | TSMC | USA |
| Yoshihiro Hayashi | Renesas Electronics Corporation | Japan |

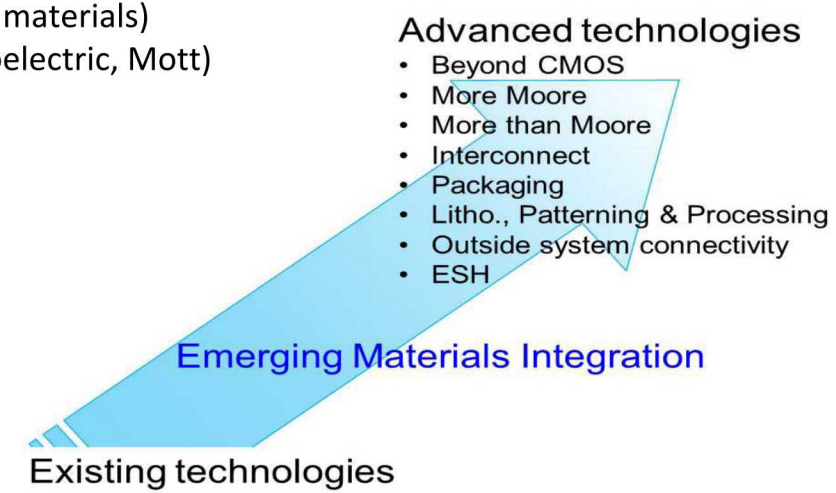
# ERM Team Members (Partial)

Hiroyuki Akinaga (AIST)
Ken Uchida (Keio Univ.)
Katsumi Ohmori (TOK)
Shintaro Sato (Fujitsu Lab.)
Satofumi Souma (Kobe Univ.)
Kei Noda (Keio Univ.)
Eric M. Vogel (Georgia Tech)
Francesca Iacopi (Univ. of Technology Sydney)

Gaku Ichihara (TUS)
Yutaka Ohno (Nagoya Univ.)
Takehito Kozasa (AIST)
Naoyuki Sugiyama (TRC/NIMS)
Yasuhide Tomioka (AIST)
Yoshiyuki Miyamoto (AIST)
Hajime Kobayashi (Sony)

# ERM Section Structure

- Near and long-term ERM challenges aligned with More Moore and Beyond CMOS
- Detailed ERM write-ups and tables are being prepared for:
  - More Moore
    - Logic (Structure (finFET, LGAA, VGAA), channel material (Si, SiGe, Ge, III-V), Doping, Contacts, Gate Stack)
    - Memory (DRAM, NVM)
  - Beyond CMOS
    - Emerging logic and information processing (2D materials, CNTs, spin, Mott, negative capacitance, nanomagnetic, excitonic, photonic, NEMS, topological materials)
    - Emerging memory and select (ReRAM, magnetic, ferroelectric, Mott)
  - Lithography and patterning
  - Packaging and heterogeneous integration
  - Outside system connectivity
- Emerging and/or disruptive concepts and technologies
  - Mobile, IoT, Sensors, Brain-Machine Interfaces, Energy, Medical
- Modeling and simulation
- Summary of links to ESH and metrology



# Novel Device Characteristics and Functionalities

| Unique device characteristics | New functionalities and applications |
| --- | --- |
| Ultra-low operating voltage | Low-voltage circuit/architecture design |
| Built-in memory in logic switches | In-memory computing, logic-in-memory, … |
| Tunable analog characteristics | Analog and neuromorphic computing |
| Native complex function (e.g., majority gate) | Efficient logic designs |
| Programmable randomness | Probabilistic logic, hardware security, … |
| Oscillatory (energy-conserving) characteristics | Neuromorphic and energy-conserving architectures |

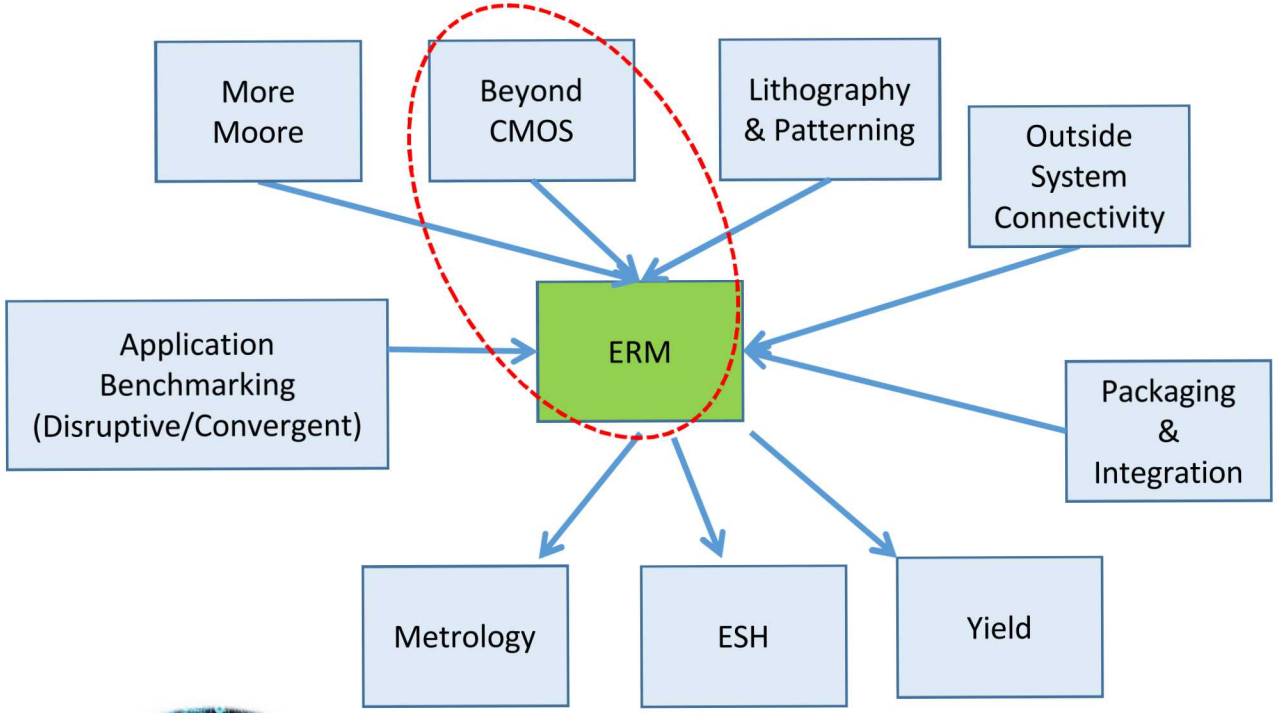
# BC Device-Architecture Interaction Workshop

*Saturday, March 30th, 2019, Monterey, CA*

| Start Time | Topic | Speaker |
|---|---|---|
| 9:00 AM | Welcome & Overview | |
| | **Bio Inspired Systems** | |
| 9:30 AM | Neuromorphic Processing Architectures with In-Memory Computing | Giacomo Indiveri (ETH Zurich) |
| 10:00 AM | Hyperdimensional Computing | Sayeef Salahuddin (UC Berkeley) |
| 10:30 AM | Break | |
| 10:45 AM | Surrogate Gradient Descent Learning and Three Factor Rules | Emre Neftci (UC Irvine) |
| 11:15 AM | Group discussion - Bio Inspired Systems | Giacomo Indiveri, Emre Neftci, Sayeef Salahuddin |
| 11:45 PM | Lunch | |
| | **Analog & Photonic Systems** | |
| 1:00 PM | Photonic Interconnects | David Miller (Stanford) |
| 1:30 PM | Neuromorphic Silicon Photonics | Bhavin Shastri (Queen's University ) & Paul Prucnal (Princeton University) |
| 2:00 PM | Rapid Combinatorial Optimization Using Analog Circuits | Patrick Xiao & Eli Yablonovitch (UC Berkeley) |
| 2:30 PM | Break | |
| 2:45 PM | Group Discussion – Analog & Photonic Systems | David Miller, Eli Yablonovitch, Patrick Xiao, Bhavin Shastri and Paul Prucnal |
| | **Cryogenic & Reversible Systems** | |
| 3:15 PM | Valleytronic Reversible Logic Gate | Yee Sin Ang (Singapore University of Technology and Design) |
| 3:45 PM | Exponentially Adiabatic Switching in Quantum Dot Systems | Craig Lent (University of Notre Dame) |
| 4:15 PM | Break | |
| 4:30 PM | Energy Efficiency in a SET-Based Brownian Circuits: Theory and Simulations | Ilke Ercan (Boğaziçi University) |
| 5:00 PM | Single Flux Quantum based Neuromorphic Computing | Michael Schneider (NIST) |
| 5:30 PM | Group discussion - Cryogenic & Reversible Systems | Yee Sin Ang, Craig Lent, Michael Schneider, Ilke Ercan |
| 6:00 PM | End | |

OSC

# Emerging Research Materials



# Difficult Challenges – Near Term

- *Devices to extend CMOS scaling, utilizing new channel materials and device structures*
- *Electrical devices based on novel mechanisms with performance and/or power efficiency beyond CMOS FET*
- *Novel high-performance memory suitable for embedded applications and denser than SRAM/DRAM*
- *Novel memory devices (including selectors) more scalable than Flash memory for storage applications*
- *Devices suitable for monolithic and heterogeneous integration*
- *Materials and processes:*
  - *that achieve performance and power scaling of lateral fin- and nanowire FETs (Si, SiGe, Ge, III-V).*
  - *that improve copper interconnect resistance and reliability*
  - *for continued scaling of DRAM/SRAM and embedded NVM*
  - *that extend lithography to sub-10 nm dimensions with reproducible properties*
  - *for heterogeneous integration of multi-chip, multi-function packages*

# Difficult Challenges – Long Term

- *Devices based on novel state variables and switching mechanisms to achieve functionalities and performance beyond the capability of CMOS FET*
- *Devices with native behaviors for the implementation of novel computing paradigms, including neural network, analog computing, in-memory computing, photonic computing, etc.*
- *Devices with novel functionalities and applications, e.g., security, energy conservation/ harvesting, etc.*
- *Devices to enable efficient implementation of unconv. and nonclassical computing solutions*
- *Novel device benchmark and device-architecture co-optimization*
- *Materials and processes:*
  - *that achieve 3D monolithic and vertical integration of high mobility and steep subthreshold transistors*
  - *for charge-based and non-charge-based beyond CMOS logic that replaces or extends CMOS*
  - *that replace copper interconnects with improved reliability and electromagnetic performance at the nanoscale*
  - *for emerging memory and select devices to replace DRAM/NVM*
  - *that enable monolithically 3D integrated complex functionality including thermal and yield challenges*

# Summary

Significant updates to BC chapter coming for 2019:

- Updates to emerging memory and logic devices
- More focus on novel computing paradigms and related device requirements
- Integrating Emerging Research Materials into the BC chapter