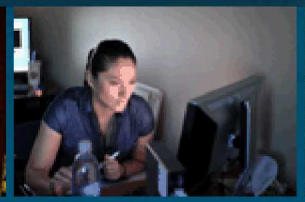
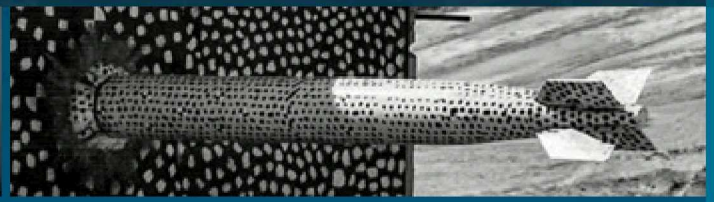
SAND2020-4476C

Component Testing, Co-Optimization, and Trade-Space Evaluation





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Sandia National Laboratories

Project ID: elt223

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Overview

Timeline

- Start – FY19
- End – FY23
- 30% complete

Budget

- Total project funding
  - DOE share – 100%
- Funding received in FY19: $250k
- Funding for FY20: $350k

Goals/Barriers

- Drive System Power Density = 33 kW/L
  - Power Electronics Density = 100 kW/L
  - Motor/Generator Density = 50 kW/L
- Power target > 100 kW
- Cost target for drive system ($6/kW)
- Operational life of drive system = 300k miles
- Design constraints include
  - Thermal limits
  - Transistor / Diode reliability
  - Capacitor reliability

Partners

- Scott Sudhoff, Steve Pekarek – Purdue University
- Jon Wierer – Lehigh University
- Woongie Sung – State University of New York (SUNY)
- Project lead: Sandia Labs, Team Members: Jack Flicker, Lee Rashkin, Lee Gill, Greg Pickrell, Todd Monson, Bob Kaplar

Relevance and Objectives

- The primary purpose of this project is to identify electric traction drive (ETD) designs, including inverter drive and electric machine, that are predicted to meet the goals outlined in the US Drive Electrical and Electronics Technical Team Roadmap [1]:
  - Power Density target for drive system = 33kW/L or a 100 kW peak system
    - Power Electronics Density = 100 kW/L
    - Electric Motor Density = 50 kW/L
  - Operational life of drive system = 300k miles
  - Cost target for drive system ($6/kW)

- To support this design goal, this effort has four objectives
  - Test and demonstrate state-of-the-art devices and new devices developed by Sandia colleagues and collaborator teams in relevant circuits
  - Generate high-fidelity dimensional and electrical models for principal power electronic components within a novel inverter design
  - Co-Optimize inverter and machine designs for power density, reliability, and efficiency
  - Demonstrate and evaluate representative converter prototypes

[1] See the U.S. DRIVE Partnership Plan, at https://www.energy.gov/eere/vehicles/downloads/us-drive-electrical-and-electronics-technical-team-roadmap

Milestones for FY20 and FY21

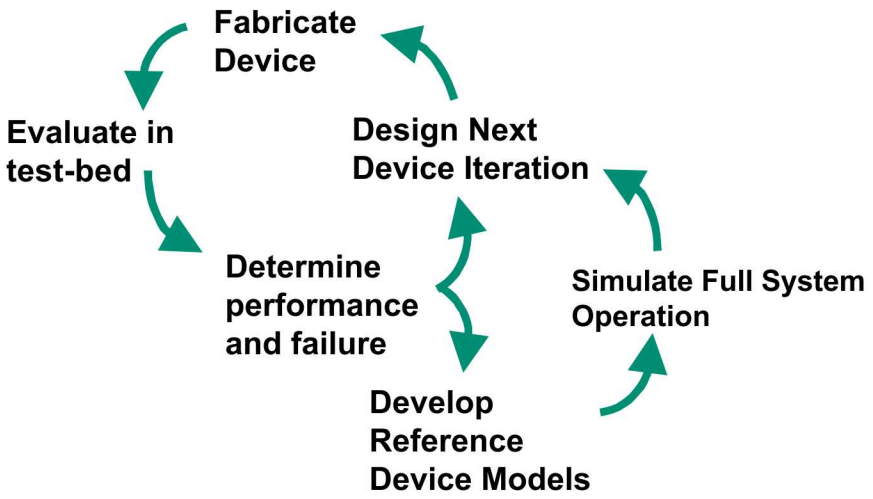
		Milestone	Date	Status
FY20	3.1	Identify a 100 kW candidate design that meets DOE power density and lifetime targets; alternatively, if targets cannot yet be reached, identify a design that is closest on the pareto curve to those targets and quantify performance gap at device/material level	3/2020	Complete
	3.2	Build and test a 5kW scale exemplar and validate electrical and thermal reference models	6/2020	In Progress
	1.4	Implement motor drive into component test-bed and use to evaluate semiconductor device operation	9/2020	In Progress
FY21	3.1	Integrate MTBF computation into inverter drive optimization	3/2021	In Progress
	3.2	Identify a compact distributed-bus filter design that meets EETT ripple requirements and evaluate against discrete component alternative	5/2021	In Progress
	1.1	Demonstrate In-Circuit Operation of SUNY Poly SiC MOSFET	6/2021	Not started
	1.2	Demonstrate In-Circuit Operation of GaN JBS Diode	9/2021	Not started

* Any proposed future work is subject to change based on funding levels

Approach – Component Testing

Objective: Test and demonstrate new devices developed by Sandia colleagues and collaborator teams in relevant circuits

- **Need rapid prototyping for R&D devices before incorporation into full power module**
- Design and construction of custom test assemblies enable
  - Demonstration of newly developed devices
  - Collection of data on performance and reliability (failure modes, mechanisms) used as input in future generations of components
  - Realistically emulating operations and stressors that exist in end-use application (vehicle drivetrain)
    - can be scaled in parameters (voltage, current, temperature, etc.) to suit intermediate maturity devices



Approach – Device-Level Analysis Predicts Performance of SiC and GaN Devices

Objective: Generate high-fidelity dimensional and electrical models for principal power electronic components within a novel inverter design

- To quantify benefits/disadvantages of v-GaN compared to SiC in EDT system, necessary to have models of SiC and v-GaN devices

- While SiC devices are commercially available, v-GaN devices are not
  - Unfair to directly compare operation of commercially available SiC devices with lab-grade v-GaN devices
    - Commercial devices are much larger area
    - Significantly less defect density
    - Optimized for production costs, not just performance alone (e.g. contact metallization)

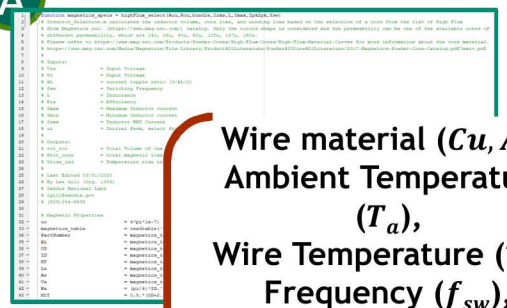
- Therefore, we took information regarding commercially available SiC devices and used first principles modeling to develop speculative v-GaN devices that are similar
  - More appropriate apples-to-apples comparison
  - Only gives approximate order of comparison
    - N.B: Devices of different materials may have different optimization for performance/cost

Approach – Passive Component Models are Carefully Developed using Latest Design Information

Objective: Generate high-fidelity dimensional and electrical models for principal power electronic components within a novel inverter design

Example: Inductor Design Code

A Wire Selection



Wire material (Cu, Al),
Ambient Temperature (T_a),
Wire Temperature (T_w),
Frequency (f_{sw}),
RMS Current (I_{rms}),
Insulation Material (K_{ins})

$$I_{amp} = \sqrt{\frac{T_w - (T_a + \Delta T_d)}{R_{dc}(1 + Y_c)R_{ca}}}$$

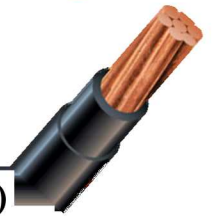
where

I_{amp}	Ampacity
T_w	Wire Temp.
T_a	Ambient Temp.
ΔT_d	Temp Rise due to dielectric loss
R_{dc}	DC resistance
Y_c	Skin & Proximity Effects
R_{ca}	Thermal resistance

Neher-McGrath Ampacity, Resistance, and Temperature Rise Calculation

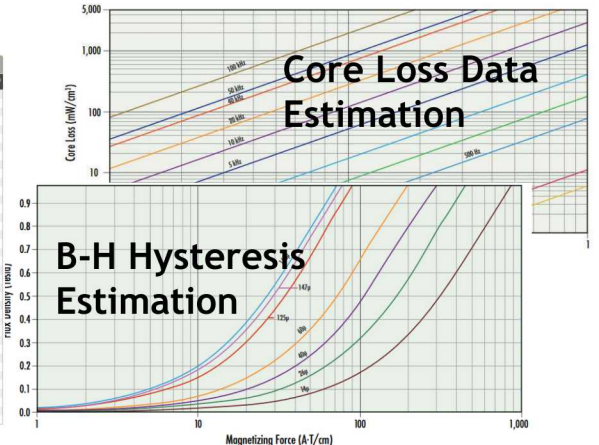
Winding Specification

Wire Size (AWG),
Resistance (R_w),
# of Wire Strains
Frequency (fsw),
RMS Current (I_{rms})



B Inductor Design

Wire Size (AWG),
Resistance (R_w),
RMS Current (I_{rms}),
Pk-to-Pk Current (I_{pk2pk}),
Frequency (fsw),



Magnetic De Specificatio

Core Data {$core\_data$},
Core Volume (V_{core}),
Winding Volume (V_{wind}),
Core Loss (P_{core}),
Copper Loss (P_{cu})

Approach – Co-Optimization & Trade-space Evaluation

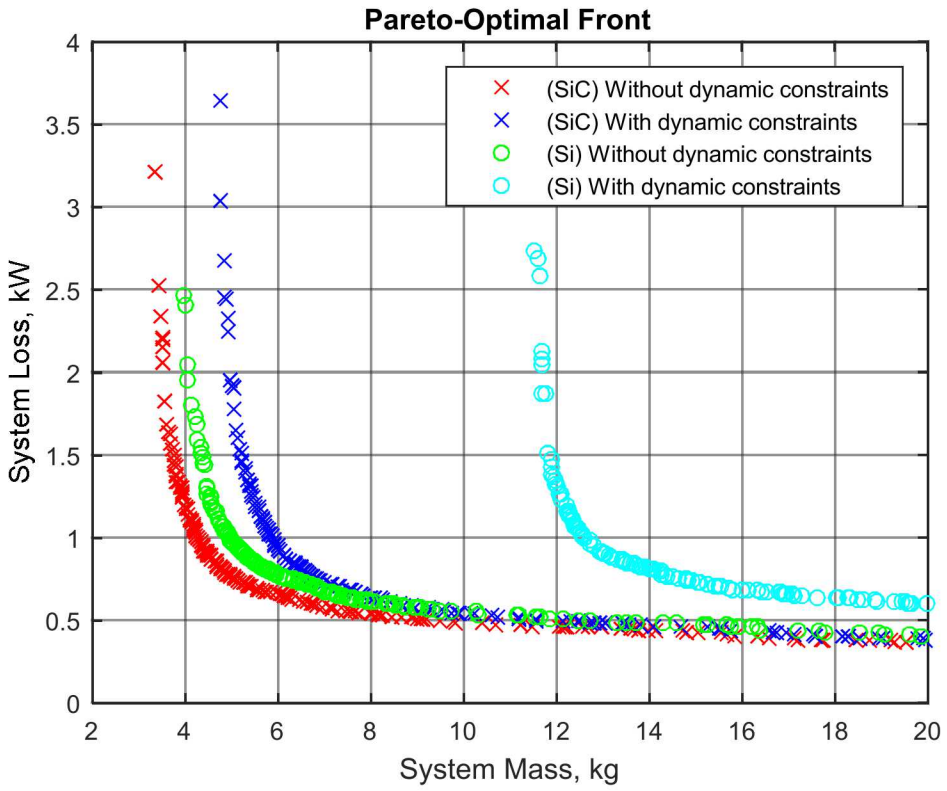
PURDUE UNIVERSITY

Objective: Co-Optimize inverter designs with machine for power density, reliability, and efficiency

Design Codes are Formulated to Co-Optimize Motor & Drive

- High-fidelity models are developed for the motor (by Purdue) and power electronic components (by Sandia)
- Purdue-developed *Genetic Optimization System Engineering Toolbox* (GOSET) [2] is used to identify designs, simultaneously solving for motor and electric drive parameters [3], [4]
- Multiple objectives are considered in the optimization of power electronics: conversion efficiency, power density, and the reliability metric *Mean Time Between Failures* (MTBF)
- In this FY, an Efficiency-Power Density optimization was performed for the inverter drive, and an MTBF-Power Density optimization was performed for a boost converter

Example from Previous Work



[2] S. D. Sudhoff, *GOSET: Genetic Optimization System Engineering Tool: For Use with MATLAB®,* version 2.6, January 1, 2014. URL: https://engineering.purdue.edu/~sudhoff/Software%20Distribution/GOSET%202.3%20manual.pdf

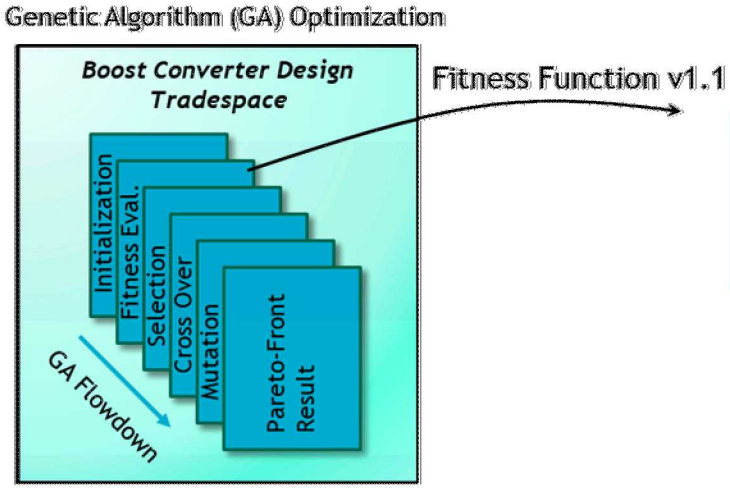
[3] B. Zhang, S. Sudhoff, S. Pekarek and J. Neely, "Optimization of a wide bandgap based generation system," *2017 IEEE Electric Ship Technologies Symposium (ESTS)*, Arlington, VA, 2017, pp. 620-628.

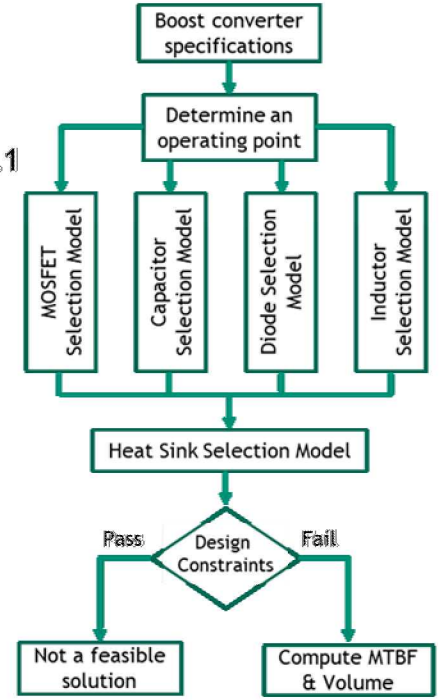
[4] B. Zhang *et al.*, "Prediction of Pareto-optimal performance improvements in a power conversion system using GaN devices," *2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Albuquerque, NM, 2017, pp. 80-86.

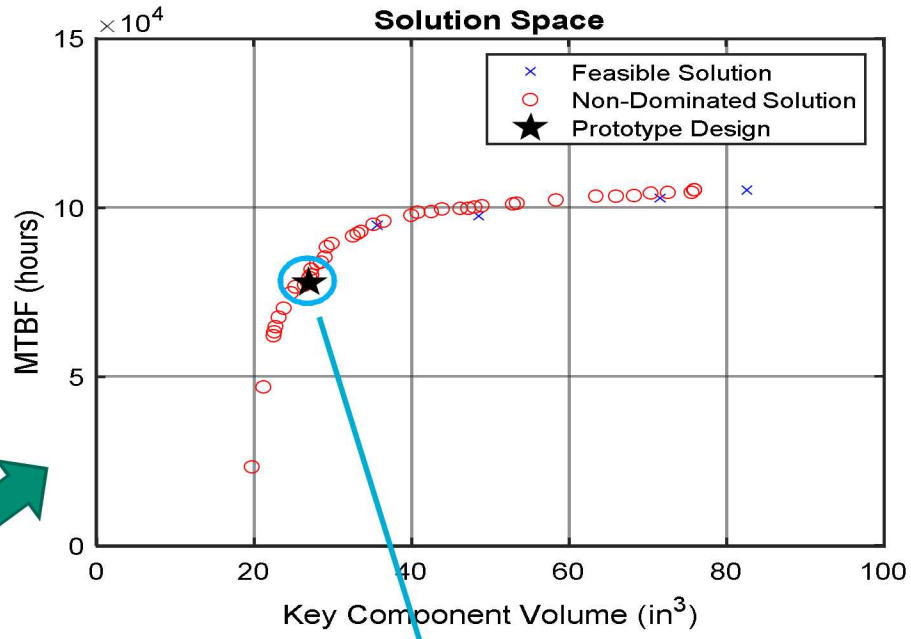
Approach – Hardware Test and Model Validation/Calibration

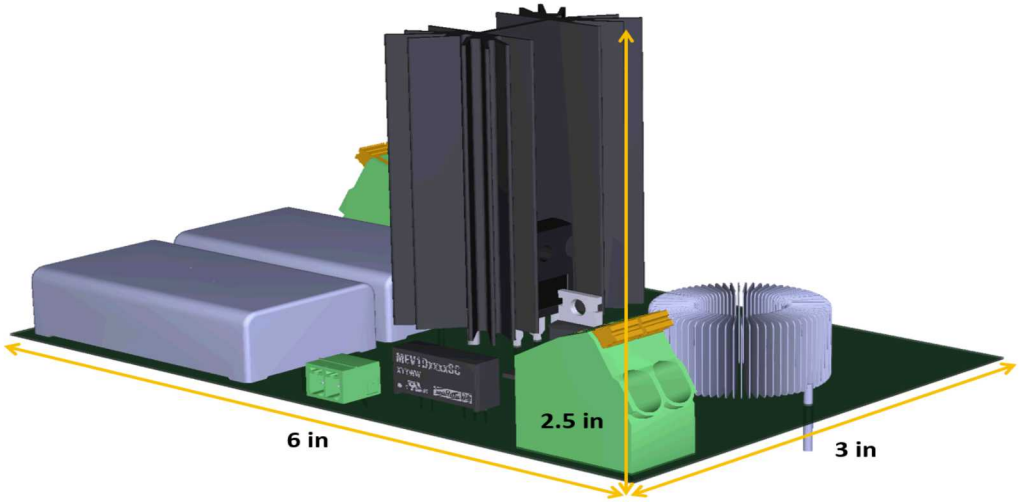
Objective: Demonstrate and evaluate representative converter prototypes

- When the optimization tools get to sufficient maturity, designs will be selected from the Pareto-Optimal sets for both the boost converter and inverter drive
- These hardware prototypes will be constructed, tested, and compared in performance to what was predicted in the models



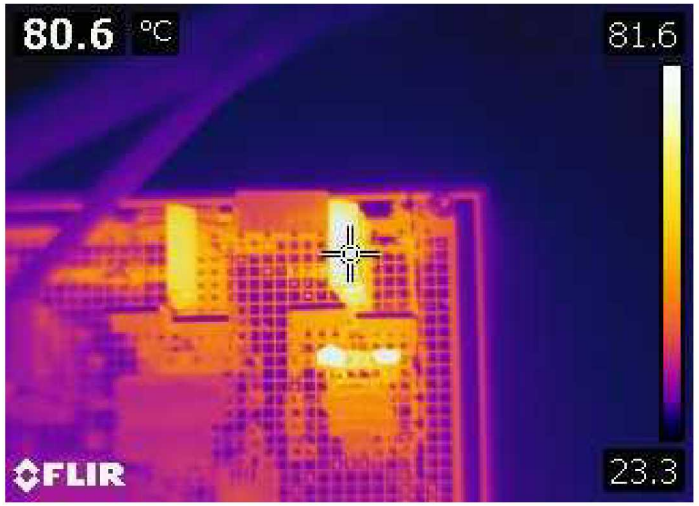


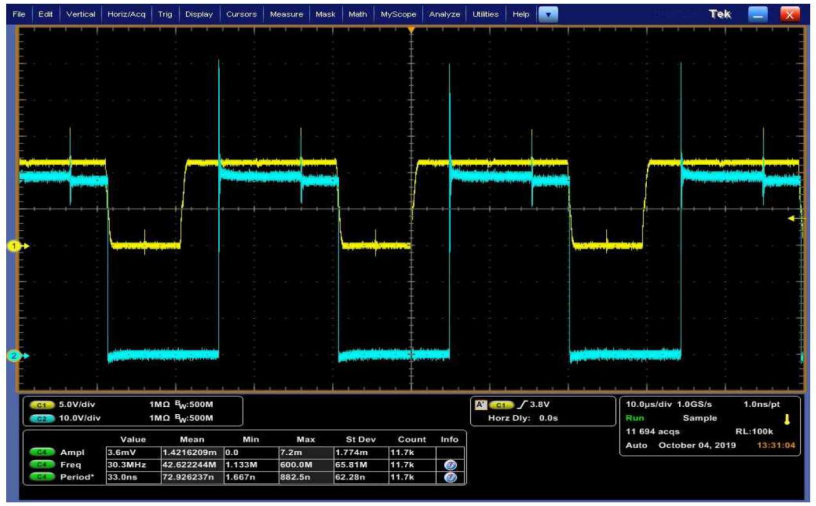


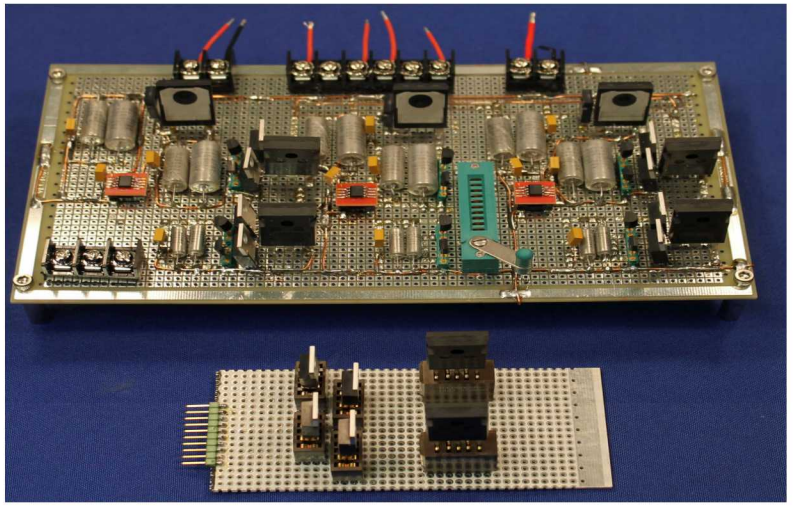


Technical Accomplishments: In-Circuit Testing Capability

- Need **rapid prototyping** for R&D devices
- Data on performance and reliability for input in future generations of components
- Realistically emulate operations and stressors that exist in end-use application but can be scaled in parameters (voltage, current, temperature, etc.) to suit intermediate maturity devices
- Developed brushless DC motor drive test-bed to evaluate performance of fabricated GaN devices
  - 1000 V, 10 A
  - Fully controllable voltage/current
  - Replicated motor dynamics
  - System was commissioned using COTS SiC devices
- This system will be used to evaluate state-of-the-art commercial devices as well as newly developed SiC and GaN devices

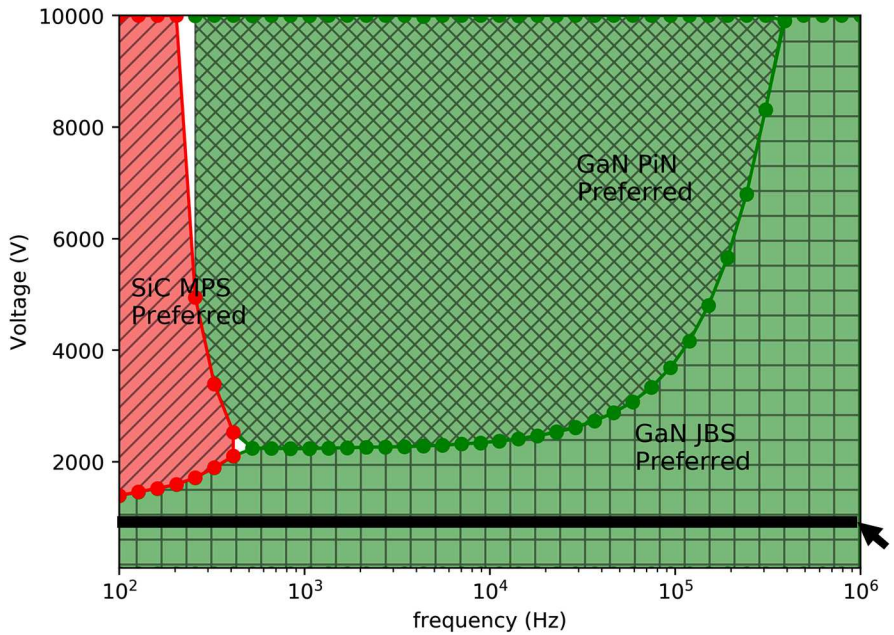


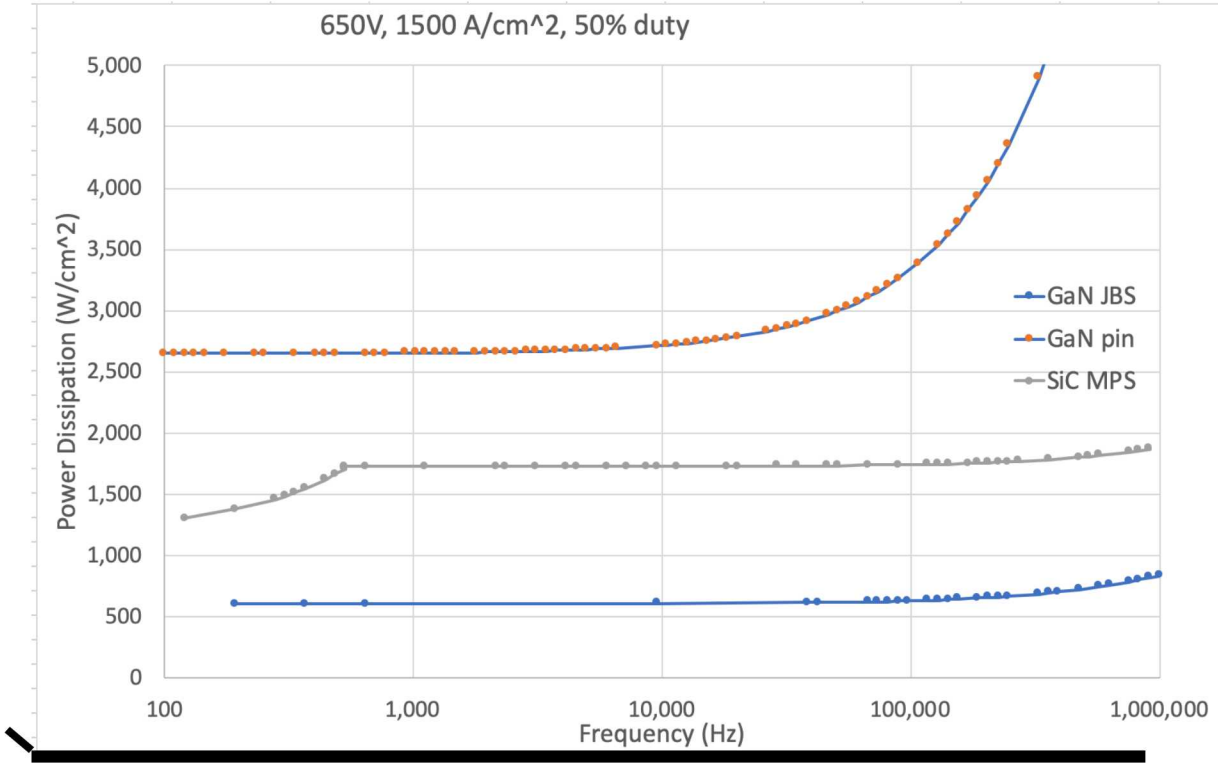




Technical Accomplishments: Device-Level Analysis Predicts Performance of SiC and GaN Diodes

- Developed first principles switching loss of GaN and SiC diodes for different diode types
- Based on analysis in [5]
  - 1D Optimization of diode layer thickness and doping based on device and material type
  - SiC Merged Pin Schottky (MPS) devices (commercially available) compared with v-GaN PiN and junction barrier Schottky (JBS) diodes (speculative)
  - Used switching loss model to define which devices are preferred for all possible operating regimes
    - e.g. v-GaN PiN preferred at high voltage as lower leakage loss overcomes larger turn-on voltage

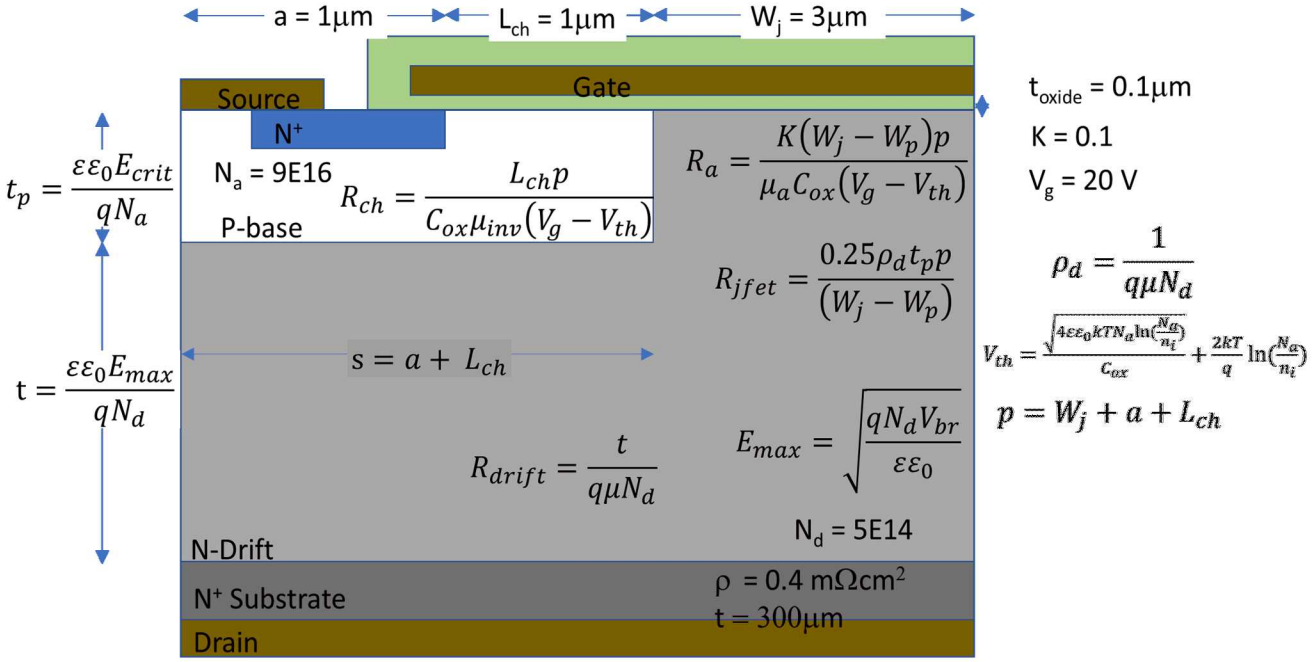


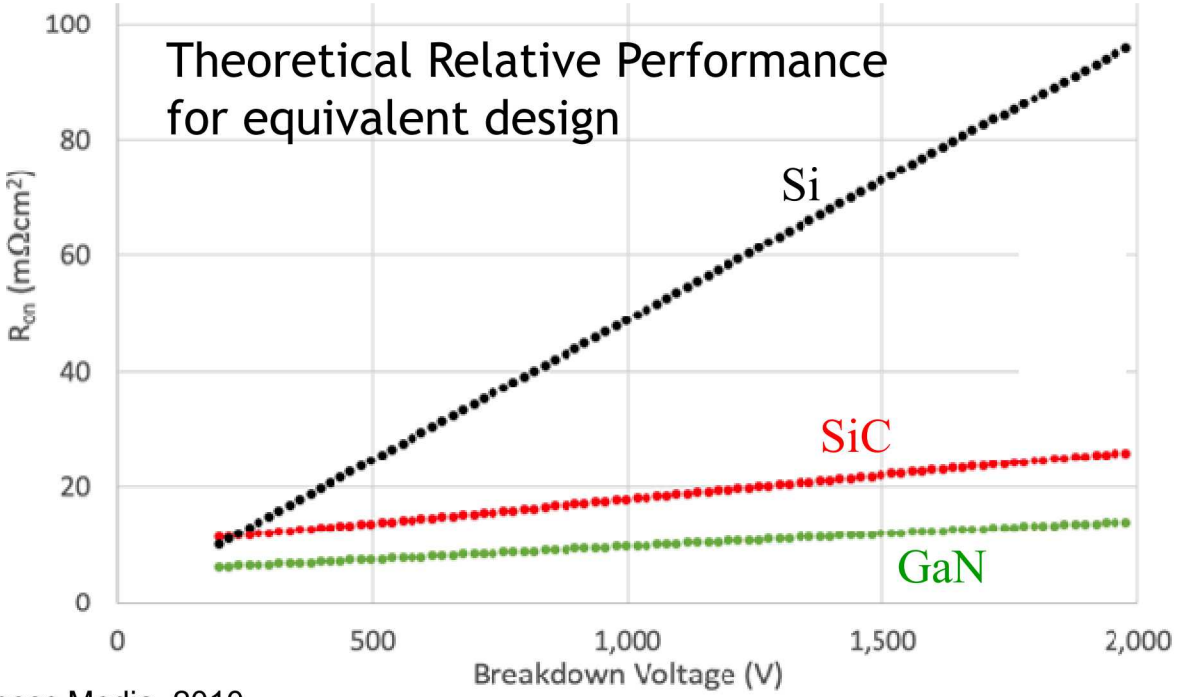


[5] J. Flicker and R. Kaplar, "Design optimization of GaN vertical power diodes and comparison to Si and SiC," *2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Albuquerque, NM, 2017, pp. 31-38.

Technical Accomplishments: Device-Level Analysis Predicts Performance of SiC and GaN MOSFETs

- Developed first principles switching loss of SiC, v-GaN and SiC MOSFET for different diode types
- Based on analysis in [6]
  - Took model SiC MOSFET (commercially available) with estimated layer thickness/doping levels
  - Changed applicable material type *without re-optimization* of layers
  - Calculated change in conduction and switching loss for new speculative device
    - Gives rough order of change between material systems; most likely systemic underestimation of benefit since real device would be optimized

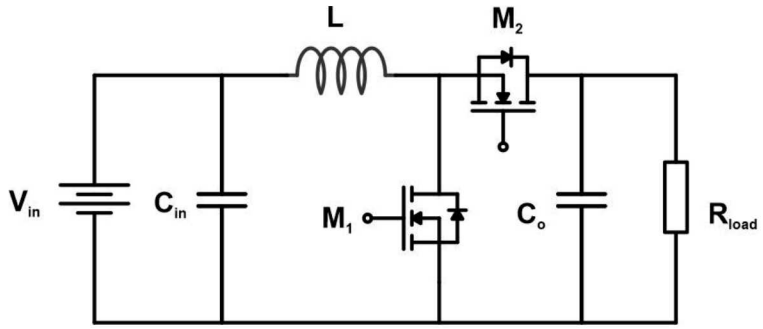




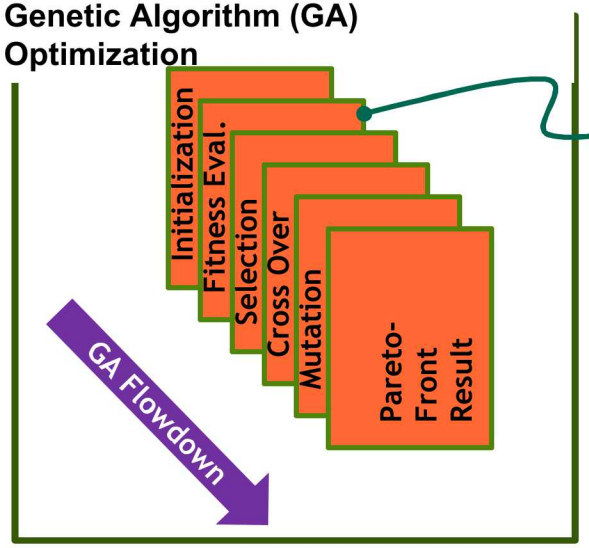
[6] Baliga, B. Jayant. *Fundamentals of power semiconductor devices*. Springer Science & Business Media, 2010.

Technical Accomplishments: Comprehensive Optimization Approach Developed and Applied to Boost Converter Design

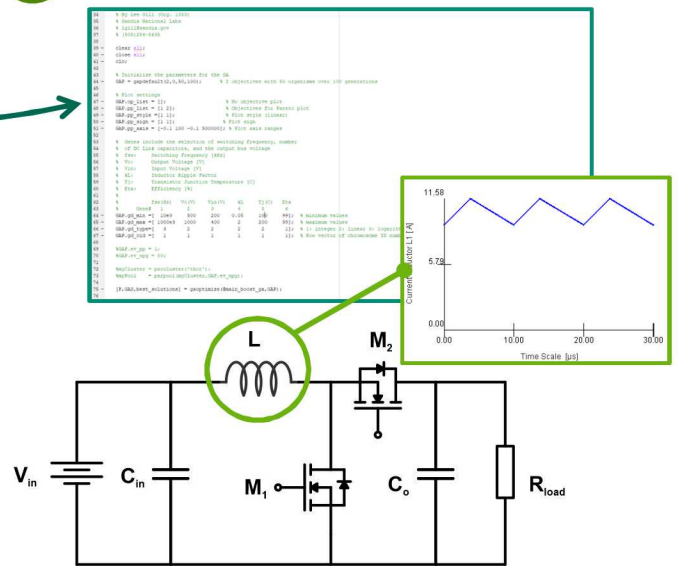
- High Fidelity Models were developed for a synchronous boost converter to support Genetic Algorithm Optimization design codes
- There are 6 components; models support:
  - Electrical property modeling for dynamic simulation
  - Inductor design and dimensional calculation
  - Transistor selection and loss modeling



Genetic Algorithm (GA) Optimization

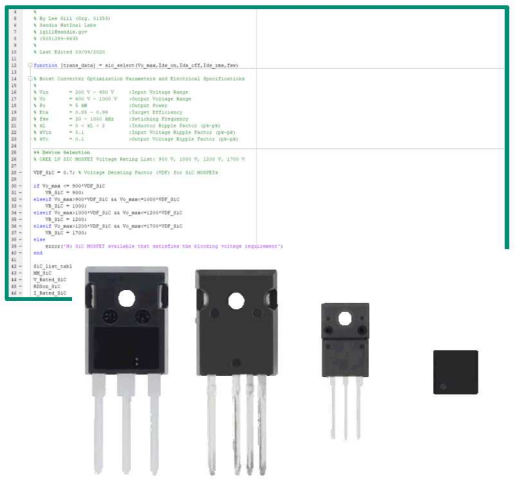


1 **Boost Converter Operating Point**



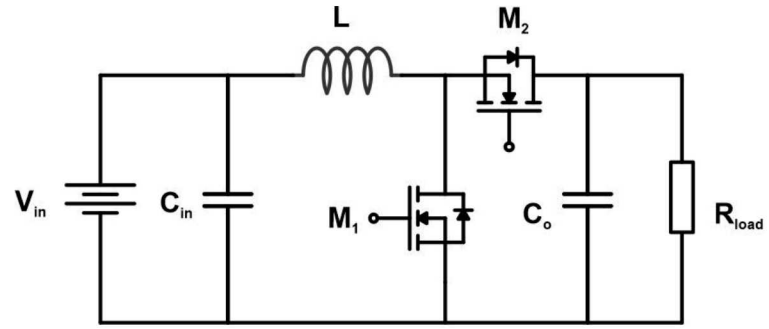
2 **Magnetics Design and Loss Model**

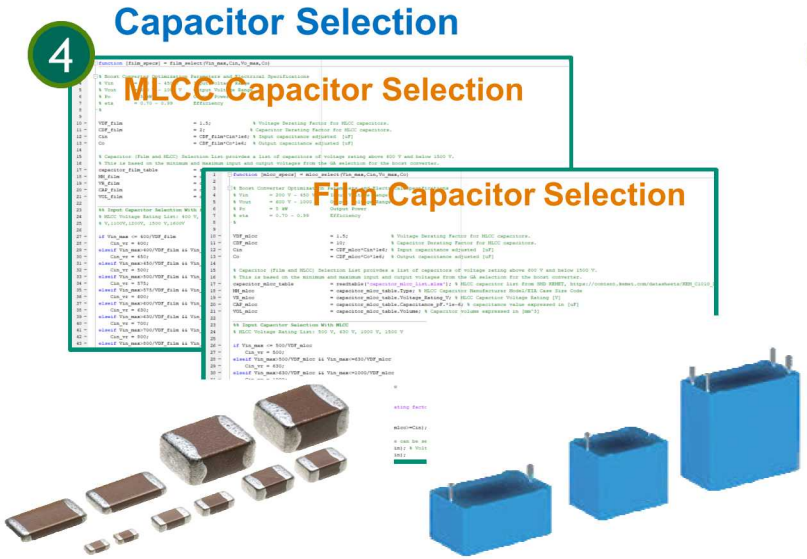
3 **Transistor Device Selection and Loss Model**

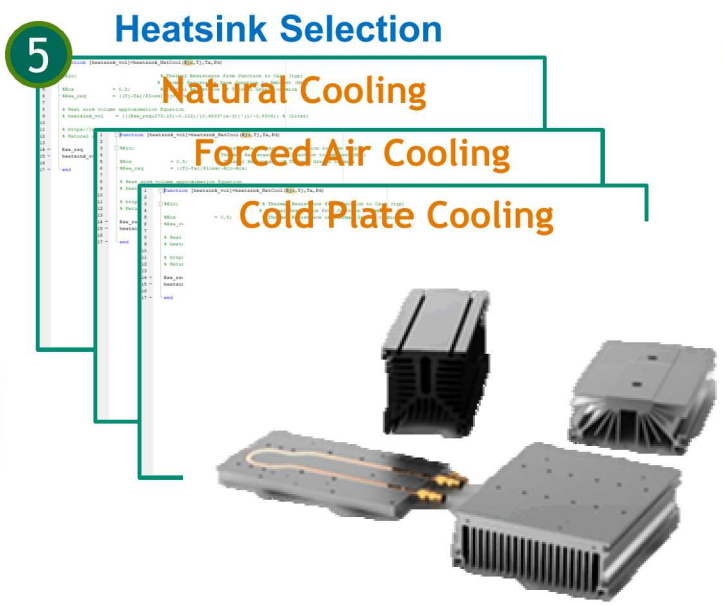


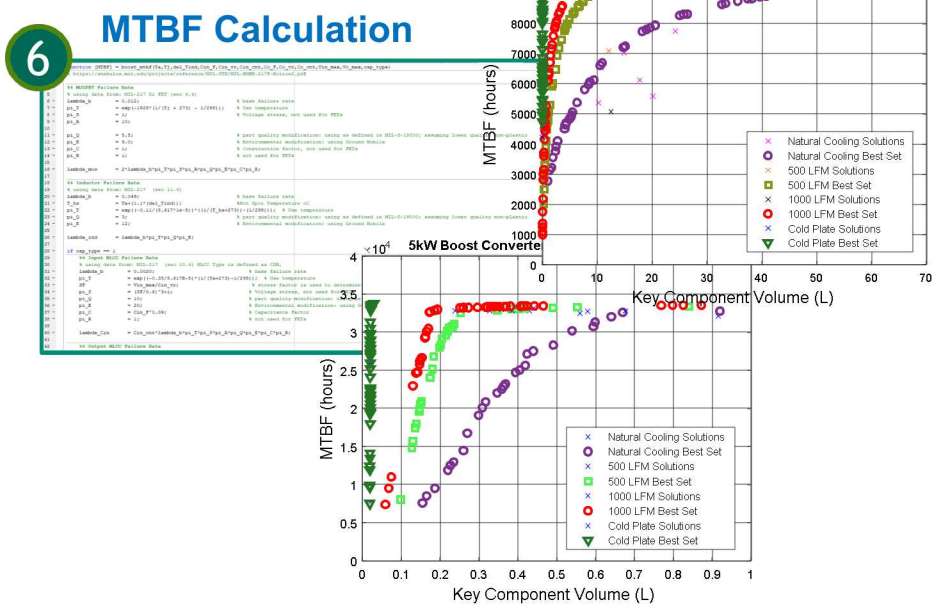
Technical Accomplishments: Comprehensive Optimization Approach Developed and Applied to Boost Converter Design

- High Fidelity Models were developed for a synchronous boost converter to support Genetic Algorithm Optimization design codes
- There are 6 components; models support:
  - Capacitor selection and loss modeling for MLCCs and Film
  - Thermal modeling and heat sink selection
  - Computation of Mean Time Between Failure (MTBF)



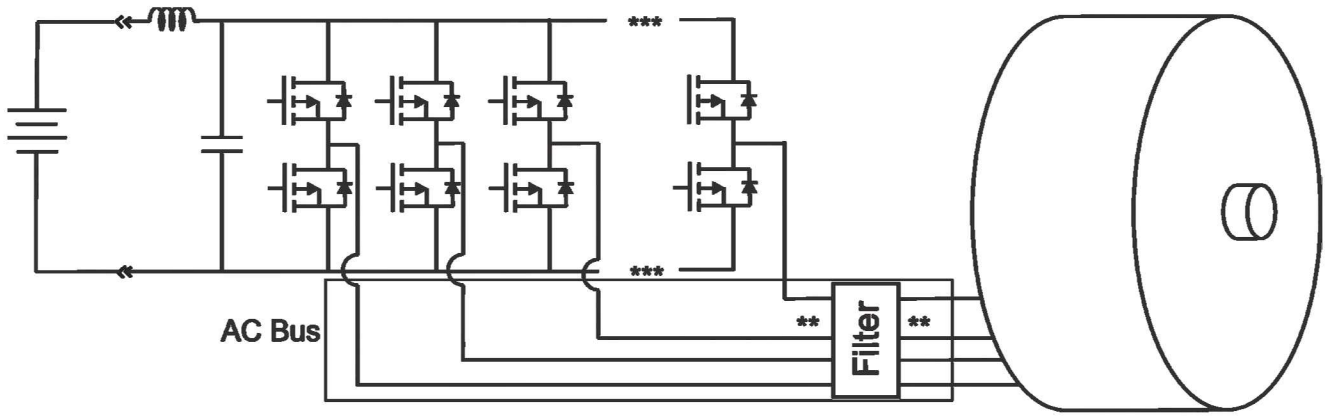


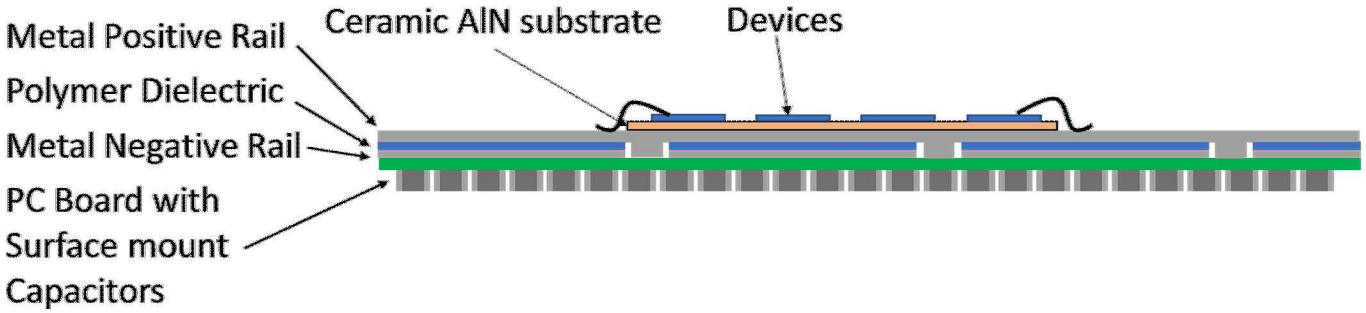




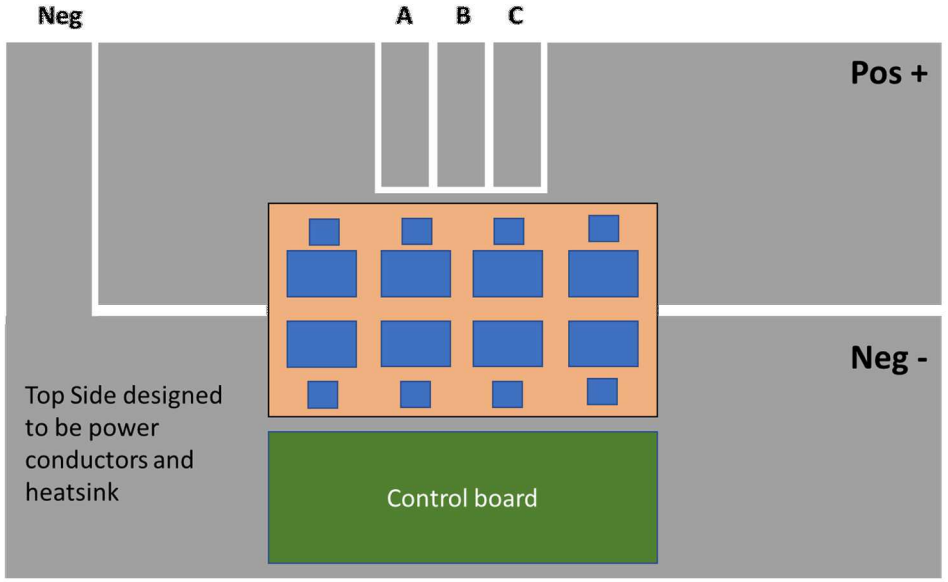
Technical Accomplishments: Novel Inverter Architecture

- An inverter drive architecture was down-selected for optimization
- Design characterized by
  - A multi-phase design [7]
  - Flat Integrated Form Factor may benefit from the energy density and temperature resilience of ceramic capacitors [8]
  - Ceramic heatsink bonded to chassis improves thermal performance [9]





Flat Integrated Form Factor

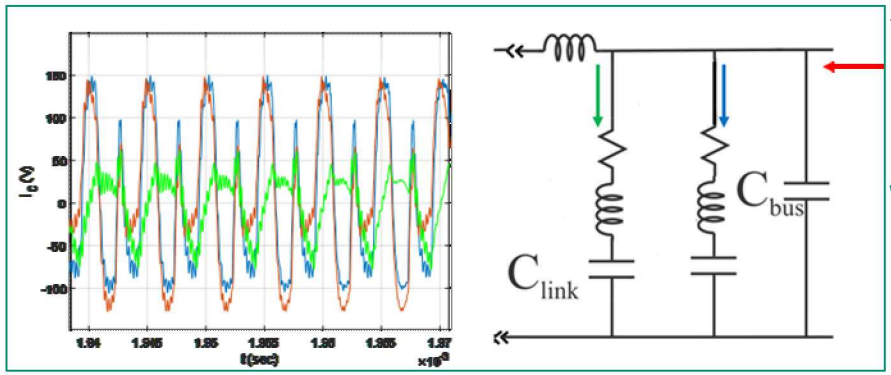


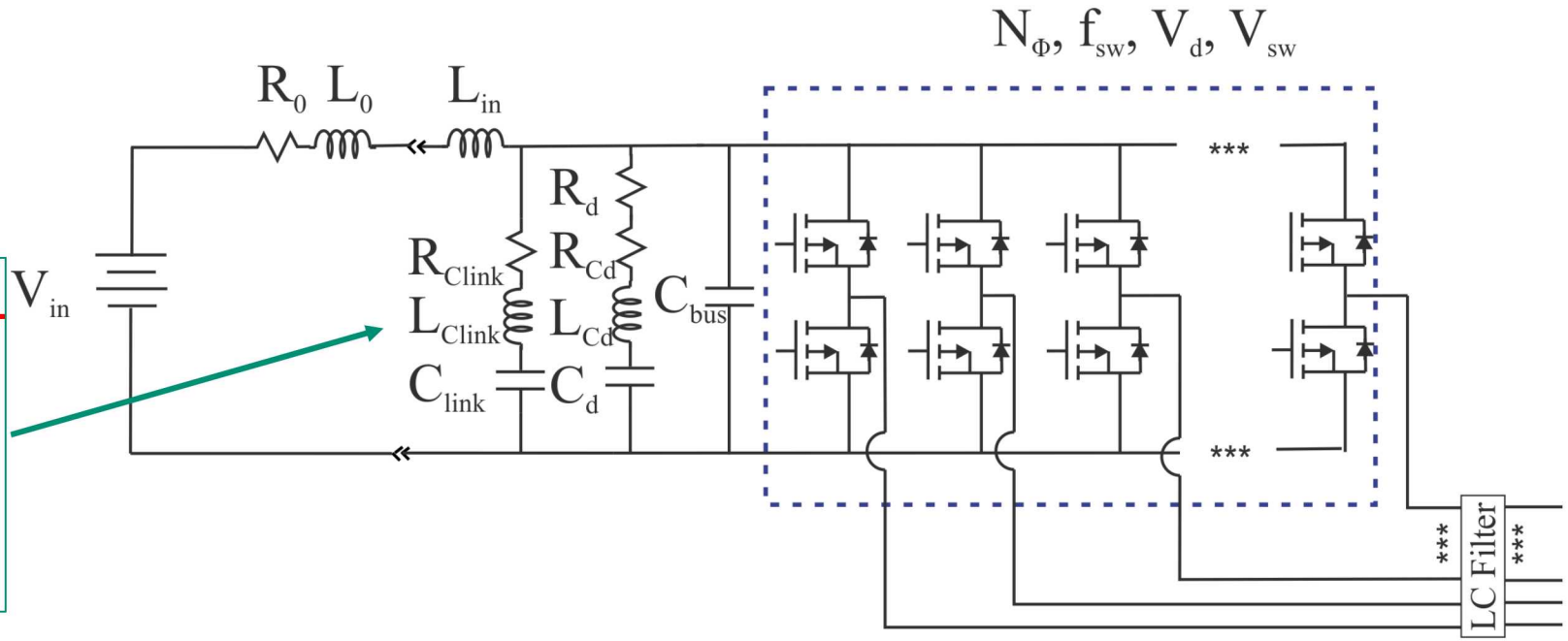
[7] Nie, Zipan; Schofield, Nigel: 'Multi-phase VSI DC-link capacitor considerations', IET Electric Power Applications, 2019, DOI: 10.1049/iet-epa.2019.0062IET Digital Library, https://digital-library.theiet.org/content/journals/10.1049/iet-epa.2019.0062

[8] J. Stewart, J. Neely, J. Delhotal and J. Flicker, "DC link bus design for high frequency, high temperature converters," *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Tampa, FL, 2017, pp. 809-815

[9] S. Yanoet al., “Development of compact power control unit for HEVs,”inProc. IEEE Energy Convers. Congr. Expo. (ECCE), Cincinnati, OH,USA, Oct. 2017, pp. 584–588..

Technical Accomplishments: High Fidelity Circuit Model was Developed for Inverter Drive





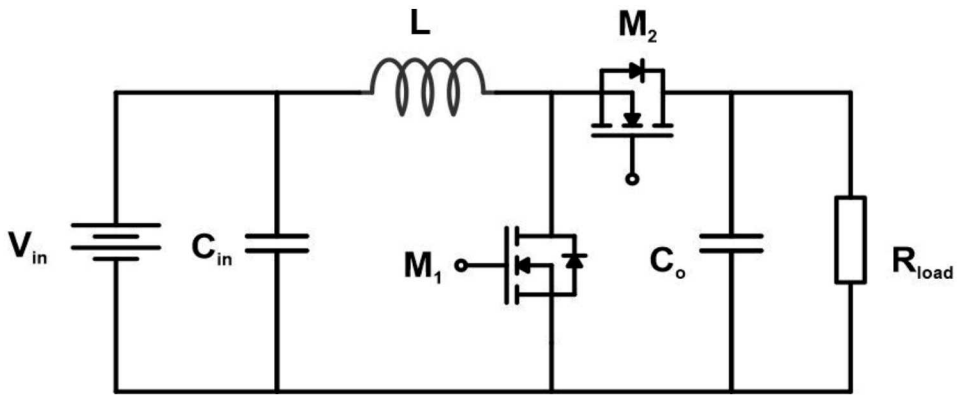
- Input parameters include:
  - Electrical frequency (speed of motor)
  - Switching frequency
  - DC link capacitance
  - DC damper capacitance and resistance
  - Input voltage
  - Number of phases

Performance metrics include:

- RMS voltage ripple (as a percentage of input voltage)
- Voltage ripple amplitude
- RMS capacitor current ripples
- Input current ripple
- Loss
- Volume and power density

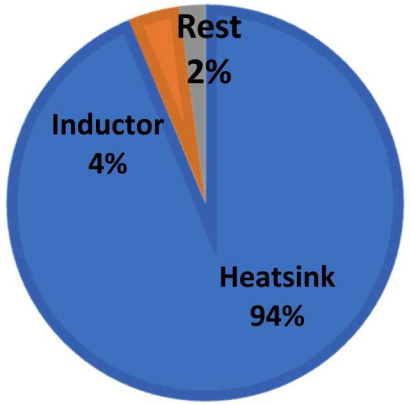
Technical Accomplishments: Boost Converter Optimization Results

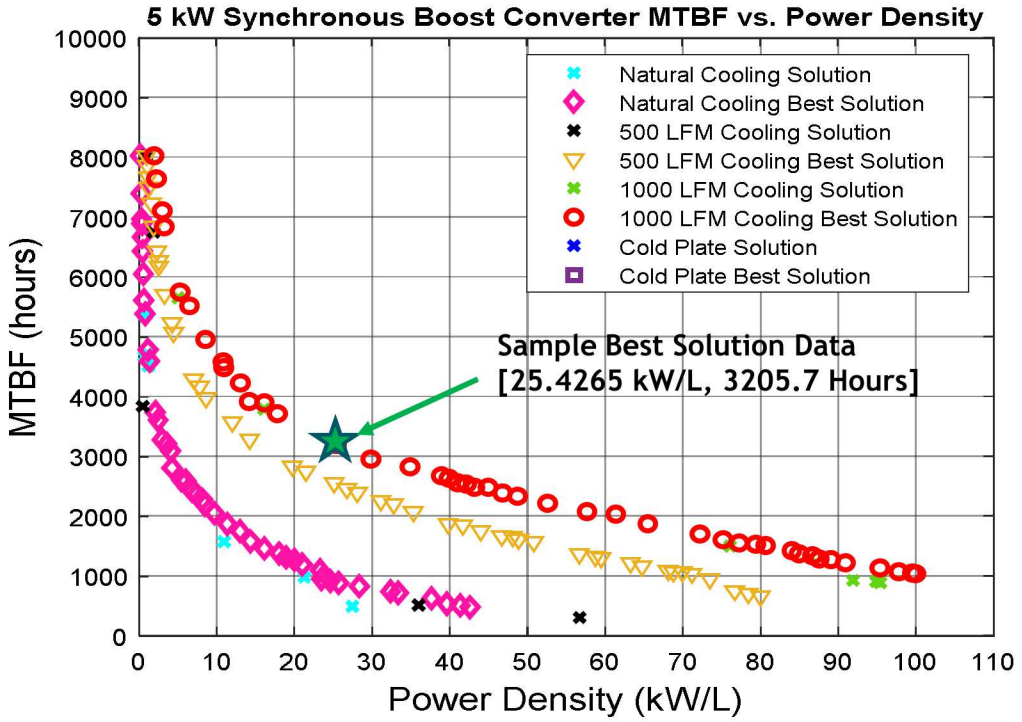
- Genetic optimization was applied to a boost converter to evaluate the trade-off between Power Density and MTBF; shown here assuming MLCCs and varying thermal management approaches
- Example design indicates 154.1 kHz switching frequency, use of SiC MOSFETs, boost from 400V to 500.2V, and forced air cooling, resulting in a power density of 25.43 kW/L, 95.12% conversion efficiency, and MTBF of 3205.7 hours
- The relatively short MTBF is largely attributed to the shorter MTBF of Multilayer Ceramic Capacitors (MLCCs) and the large number of them in the design



Parameter Selection	Specifications	Loss
Core	C058894A2HT19	65.67 W
Winding	33 AWG, 40 Strains	14.28 W
HS Transistor	C3M1020090D	107.677 W
LS Transistor	C3M1020090D	52.074 W
Input Capacitor	1 nF (1 X 1nF of '0603')	-
Output Capacitor	3.4 µF (34 X 0.1 µF of '1808')	-
Heatsink	1000 LFM	-
Efficiency	-	95.12%

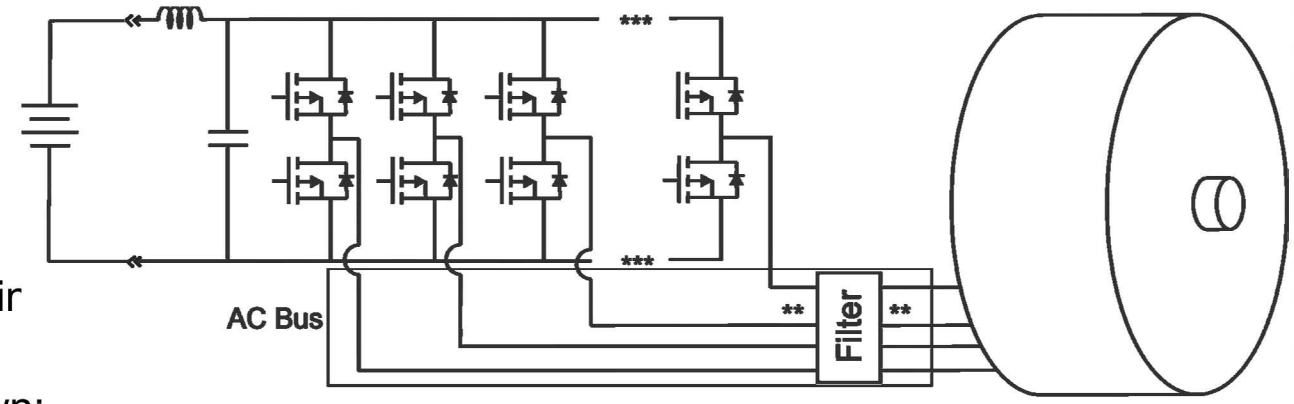
Total Volume Breakdown of 0.197L

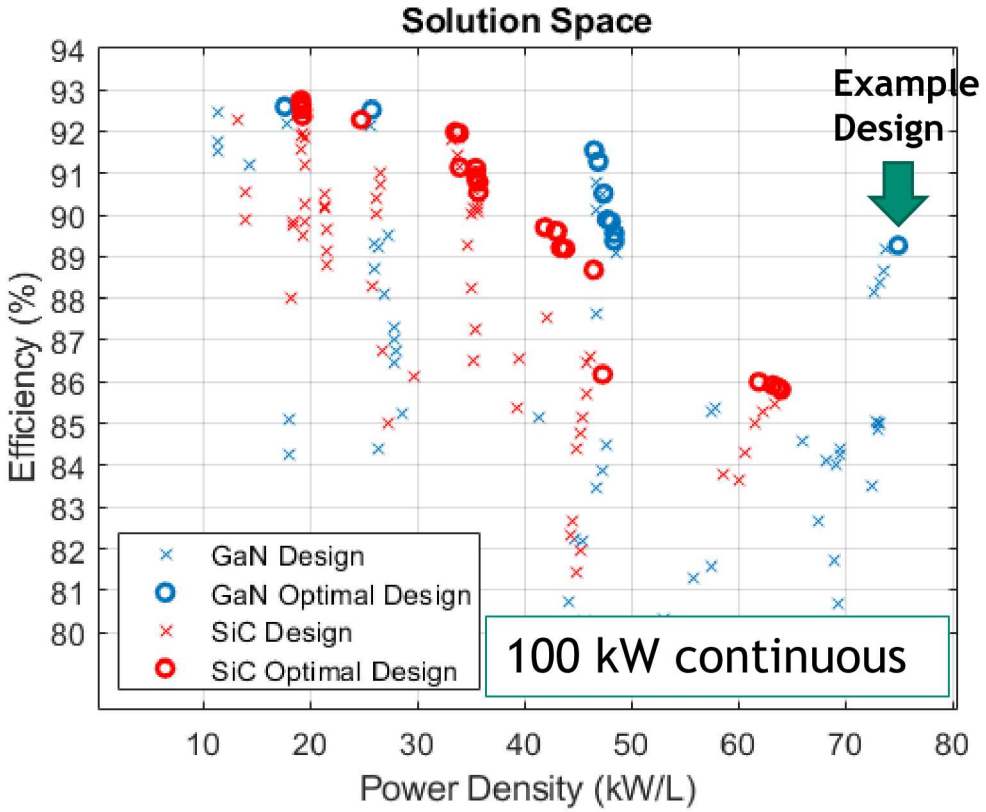




Technical Accomplishments: Inverter Drive Optimization Results

- Genetic optimization was applied to the inverter to evaluate the trade-off between Power Density and Efficiency
- Optimization has been performed for systems based on commercially available SiC MOSFETS and lateral GaN extrapolated from theoretical behavior. Vertical GaN model ir progress.
- Examining the parameter values some tendencies are shown:
  - 800-1000 V input
  - ≥200 kHz switching
  - 250-400 capacitors on circuit board
- Example design indicates use of GaN devices, 3 Phases, a 915 Vdc link voltage, 320 ceramic capacitors, 340 kHz switching, is 89.3% efficient at 100 kW, and has 74.9 kW/L power density; component volume is given by:





Component	Volume (L)	% of total	Loss (kW)	% of total
Module	0.010	0.557	0.387	23.95
Capacitor	0.208	11.60	0.001	0.0082
Input Inductor	0	0	0	0
Filter Inductor	1.512	84.33	1.228	76.04
Cooling System	0.063	3.517	N/A	N/A

Responses to Previous Year Reviewers' Comments

This project was reviewed at the 2019 AMR

There were three main concerns regarding (1) the value, progress, and details of the testbed, (2) the level of detail captured in the model, and (3) clarity on the advancement over the state-of-the-art

Question 1, Reviewer 1 - "This reviewer said … More information on the test-bed(s) (planned or existing) and its capabilities would be appreciated..."

Question 2, Reviewer 3 – "This reviewer said that some progress was shown in design tradeoffs. No progress was shown in the development of the custom test bed."

Response: We appreciate the reviewers' comments. Since the last AMR, the testbed has been constructed and will be deployed to evaluate custom devices, SiC and GaN. The testbed was designed as a reduced scale inverter, capable of operating at a variety of switching frequencies, fundamental frequencies, and voltages up to 1000V. Details of the testbed are on slide 10.

This FY, additional hardware prototypes will also be built, but these initial prototypes will use COTS SiC devices and are primarily intended to validate the optimization codes. In contrast, the Testbed is intended to evaluate new devices.

Responses to Previous Year Reviewers' Comments

This project was reviewed at the 2019 AMR

There were three main concerns regarding (1) the value, progress, and details of the testbed, (2) the level of detail captured in the model, and (3) clarity on the advancement over the state-of-the-art

Question 1, Reviewer 1 - "This reviewer said … Additional detail about the level of detail captured by the reduced-order metamodels would also be appreciated."

Question 2, Reviewer 2 - "This reviewer suggested ... [s]ome of the performance of the power converter is very much going to depend on the layout of the devices and the converter. The reviewer asked if this level of detail will be captured."

Response:

A meta-model is currently used for computing the cooling plate volume assuming a flat single-sided interface and uniform heating of the substrate. The machine model used in the simulations is currently a permanent magnet machine model, specified for 20 krpm and adjusted for phase number. The machine design will be lead by Purdue University; see elt248

The size of the devices is accounted for based on peak current and material current density, and the spacing is accounted for based on peak voltage, and creepage and clearance requirements. A similar approach is taken for the layout of the ceramic capacitors. Models that capture the impact of layout on the ESL in each capacitor are under development as this effects the current distribution. Details of the device and other component models are provided in more detail throughout the Approach and Accomplishments sections.

Responses to Previous Year Reviewers' Comments

This project was reviewed at the 2019 AMR

There were three main concerns regarding (1) the value, progress, and details of the testbed, (2) the level of detail captured in the model, and (3) clarity on the advancement over the state-of-the-art

Question 1, Reviewer 3 – "This reviewer said that it is not clear how this approach is an advancement from the current state-of-the-art. The reviewer asked what new techniques or technologies will be investigated ..."

Response: This project is intended to interface strongly with 5 other projects:

- A Sandia-led project to develop GaN diodes and transistors, elt210
- A Sandia-led project to develop methods to improve MLCC reliability, elt222
- A Sandia-led project to develop low-loss magnetic materials, elt216
- A SUNY Poly-led effort to develop advanced SiC devices
- A Purdue-led effort to develop a first-of-its-kind electric machine, elt248

The testing, modeling, integration and optimization efforts employed in this project help to reveal how different state-of-the-art technologies and in-development technologies may be combined to realize a first-of-its-kind drive system that meets DOE's drivetrain performance goals.

Collaboration

Purdue University/Sonrisa Research, Inc. (Scott Sudhoff) – Working with Sandia to co-optimize motor and drive

Lehigh University (Jon Wierer) – Working with Sandia for design/simulation/modeling of GaN JBS diodes.

State University of New York (SUNY) (Woongie Sung) – Fabricating SiC JBS diode integrated with MOSFETs

Remaining Challenges and Barriers

- Identifying AC Bus filter designs with reduced volume
  - Current designs indicate that the volume is dominated by the AC filter volume
  - This development will be included for next Fiscal Year

- Improving the reliability of Multilayer Ceramic Capacitors (MLCCs) to aid in identifying inverter designs that can achieve 300,000 miles
  - To establish a range of 300,000 miles (DOE target); assuming 13,456 miles/year average [10] and 435 hours/year in vehicle [11], this becomes 22.3 years reliability (roadmap indicates 15 years [1]), and **9702** hours of operation
  - Thus far, boost converter optimization indicates MTBFs < 9000 hours, largely due to the shorter MTBF of MLCCs; the inverter will have more of these than were considered for the boost converter, see MLCC reliability improvement efforts in elt222

[10] US Department of Transportation Federal Highway Administration driving statistics; URL: https://www.fhwa.dot.gov/ohim/onh00/bar8.htm

[11] Sean Szymkowski; Study: Americans spend 18 days in their car per year, forge close bonds with a vehicle; April 2019; URL: https://www.thecarconnection.com/news/1122782_study-americans-spend-18-days-in-their-car-per-year-forge-close-bonds-with-a-vehicle

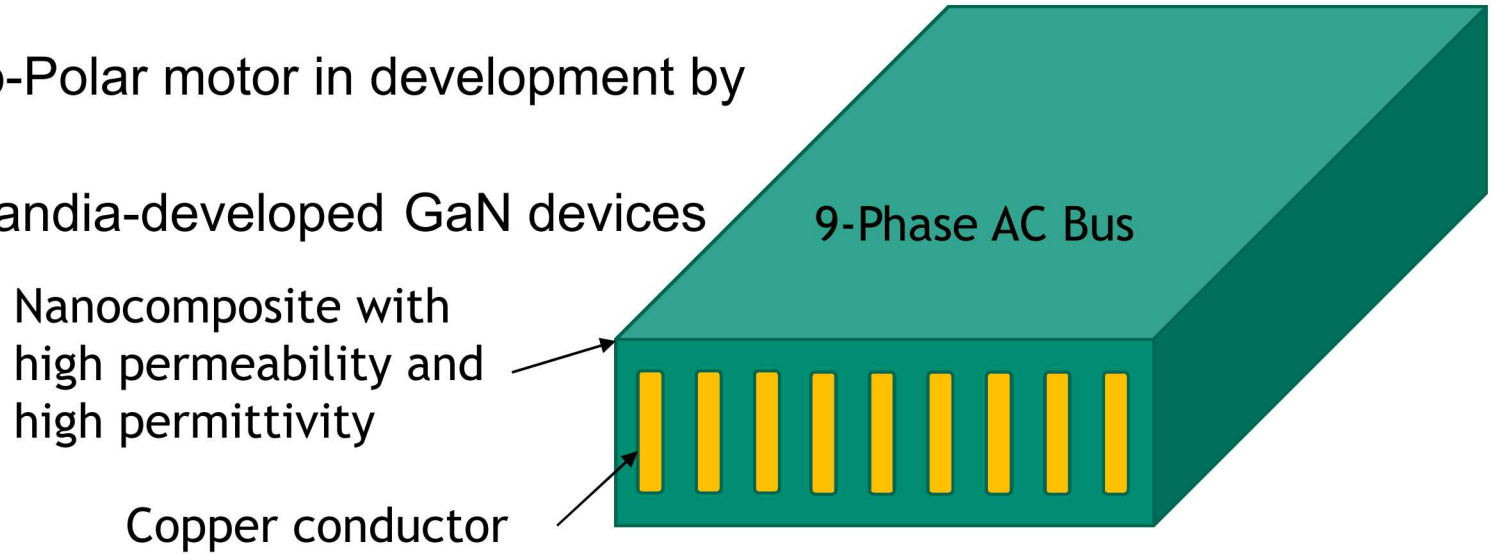
Proposed Future Research

Remaining FY20 Tasks

- Update Optimization to optimize for 100 kW peak, 55 kW continuous
- Building and Testing Reduced Scale Prototypes
  - 5 kW Boost Converter
  - 10 kW peak (5.5 kW continuous) Inverter Drive

Research in FY21 and Beyond

- Develop advanced distributed AC Filter concept to substantially reduce AC bus/filter volume
- Co-Optimize inverter and Homo-Polar motor in development by Purdue University
- Build inverter exemplar using Sandia-developed GaN devices



* Any proposed future work is subject to change based on funding levels

Summary

- A research approach is identified to test, model and simulate power components and to optimize a power train design using multi-objective optimization tools
- This optimization approach enables a holistic-approach to the drive design
  - Design codes will first be developed to optimize candidate power electronic and motor designs separately; these will then be merged to co-optimize these two components
  - Each year, hardware prototypes will be developed to verify designs and recalibrate models
  - Sandia is working closely with Purdue; Purdue is focusing on the machine optimization
- Progress has been made on the development of modeling tools and advanced performance evaluation methods, i.e. MTBF calculation
- Candidate designs are being down-selected and will be built + tested this FY
- Hardware test results will be used to demonstrate design ideas and calibrate models

Reviewer-Only Slides

Publications and Presentations

- **Publications**
  - L. Rashkin, J. Neely, J. Flicker, R. Darbali; “Optimal Power Module Design for High Power Density Traction Drive System”; *IEEE Transportation Electrification Conference* (ITEC2020); Chicago, IL; June 24-26 2020.
  - L. Gill, J. Neely, L. Rashkin, J. Flicker and R. Kaplar; "Co-Optimization of Boost Converter Reliability and Volumetric Power Density Using Genetic Algorithm“; *2020 IEEE Energy Conversion Congress and Exposition* (ECCE2020); Detroit, MI; Oct 11-15, 2020.

- **Presentations**
  - J. Neely, G. Pickrell, J. Flicker, L. Rashkin, R. Kaplar ; “The Case for Vertical Gallium Nitride Devices in Electric Vehicle Drives"; *2020 IEEE Applied Power Electronics Conference* (APEC2020); Industry Session: Vehicle Electrification II, Delayed Virtual Event

Critical Assumptions and Issues

- Power density targets are based on the combined volume of all power electronic modules and machines (whether there be one centralized drive with motor or 4 in-wheel drives with motors) needed to achieve total power

- DOE targets pertaining to reliability can be established using limited laboratory testing that is scaled using reliability models.