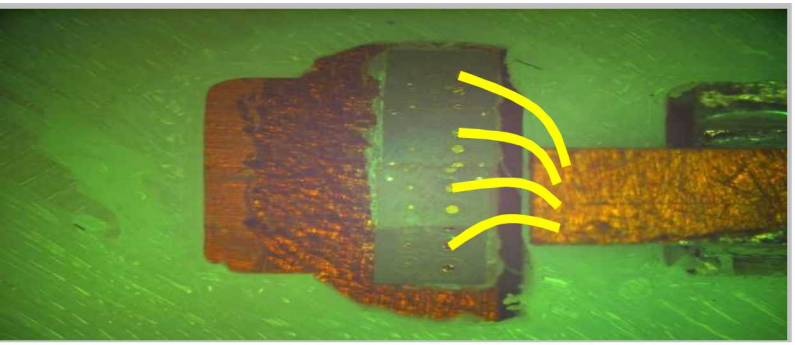
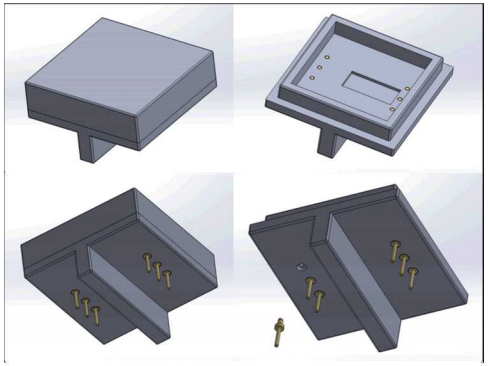
This paper describes objective technical results and analysis. Any subjective views or opinions that might be expressed in the paper do not necessarily represent the views of the U.S. Department of Energy or the United States Government.

SAND2020-3651C





Module-Level Paralleling of Vertical GaN PiN Diodes

Jack Flicker, Robert Brocato, Jarod Delhotal, Jason Neely, Bjorn Sumner, Jeramy Dickerson, and Robert Kaplar

Sandia National Laboratories

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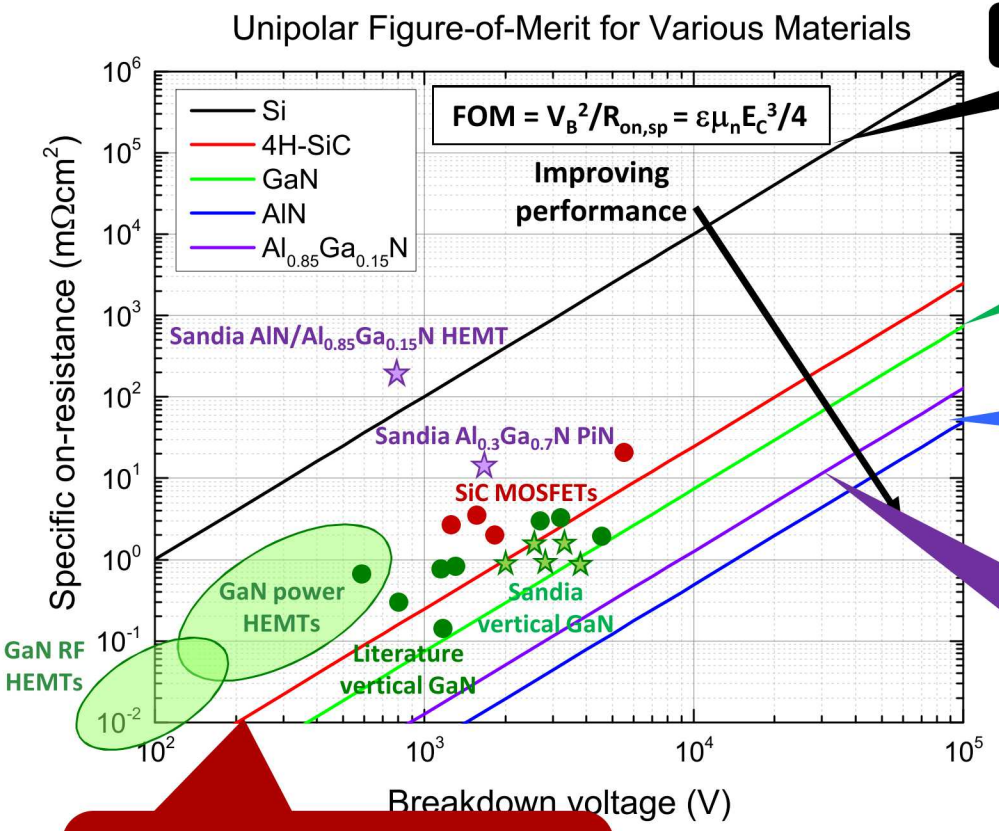
Generation-After-Next Power Electronics

- GaN is emerging as the next power electronics material system
- unipolar Figure of Merit (FOM) surpassing that of Silicon Carbide (SiC).
- Rapid progress in growth and fabrication of vertical GaN devices



Si – Today's standard

GaN
Lateral devices fairly mature
Vertical devices emerging

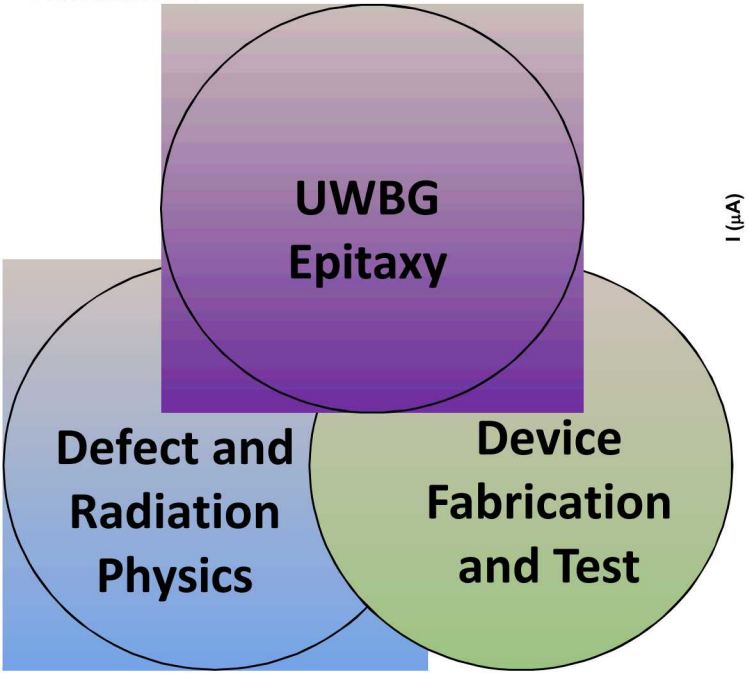
AlN
Unexplored space
Unprecedented performance

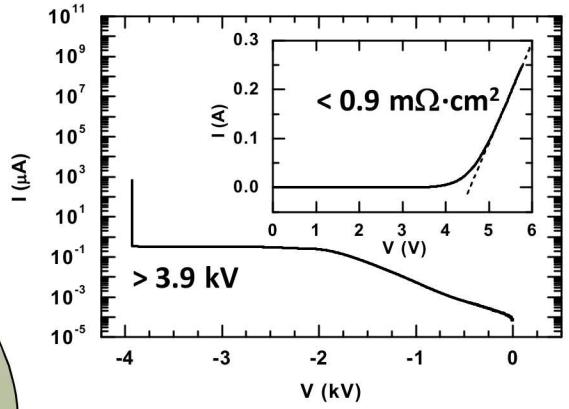
AlGaN
Unexplored space
Unprecedented performance
Heterostructures are available

SiC
Many commercial devices now available

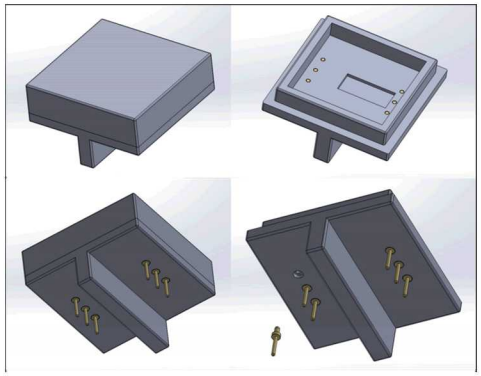
Official Use Only

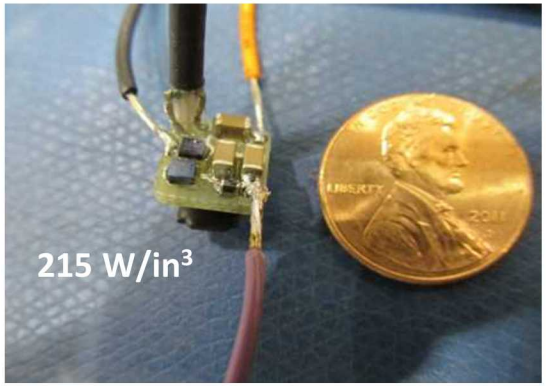
Generation-After-Next Power Electronics

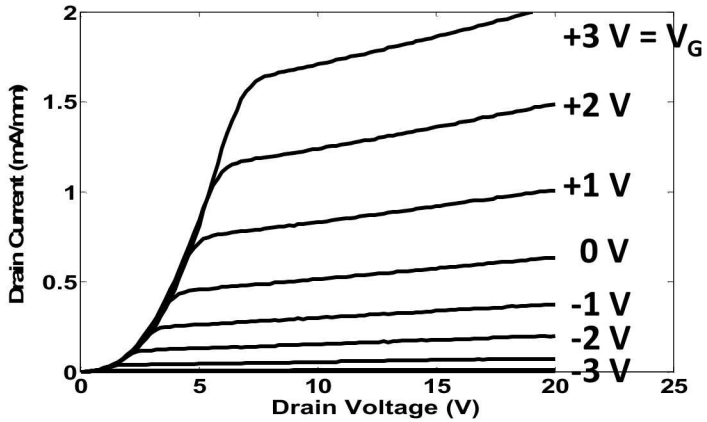




v-GaN PiN diode
$V_B^2/R_{on,sp}$ = 18 GW/cm²







3D Printed HV Package
200°C, > 15kV
5nH at 1GHz

DC/DC Point-of-Load Converter
Size is < 0.04 in³
92 V, ~92 mA => 8.5W,
215W/in³, 1 MHz

85% AlGaN Lateral Transistor

Official Use Only

v-GaN Power Devices

Sandia National Laboratories

Vertical device (15 kV)

- **Current flow and voltage drop perpendicular to surface**
- **Architecture is better-suited to high voltage devices**
- **But requires native substrates and low doping**
    - **Non-trivial materials issues**

- **v-GaN materials are still relative immature technology**
    - **die areas have tended to be small**
        - **→ limits current handling ability**
        - **→ limits usage in realistic power electronic systems**

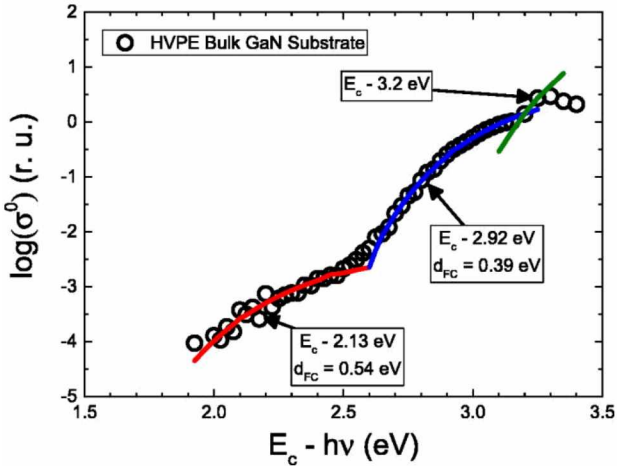
- **Sandia is pursuing two pathways to v-GaN implementation**

v-GaN Power Devices

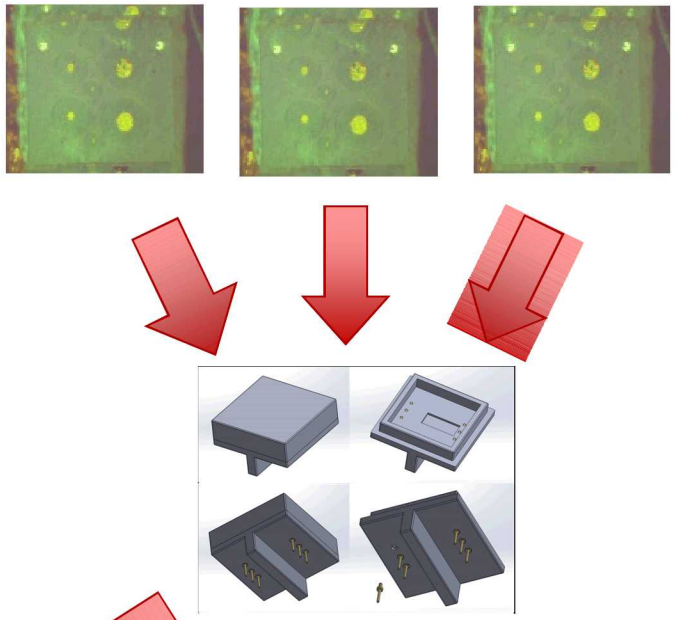
- **Sandia is pursuing two pathways to v-GaN implementation**

Identification and elimination of defects during growth

- DLOS, DLTS, CV



Paralleling of small-area die into power modules



Implementation into realistic power systems

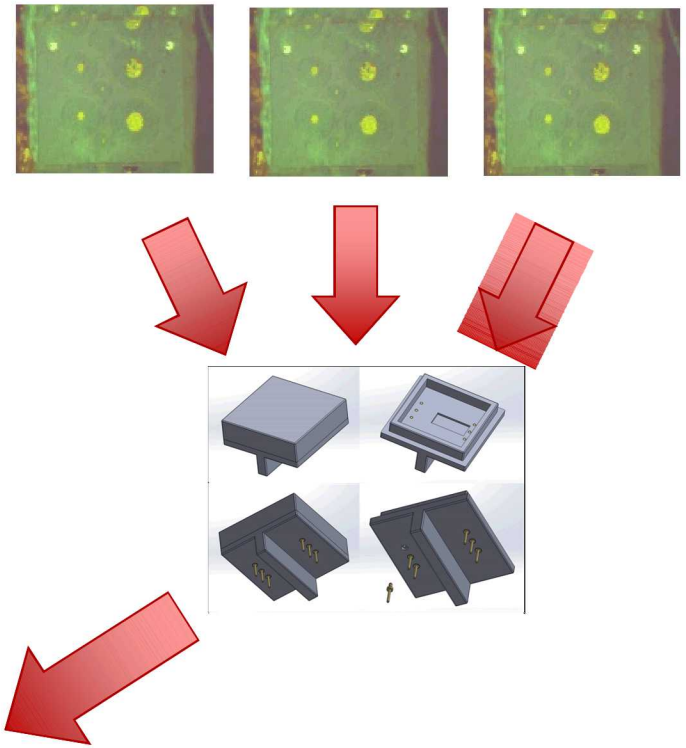
v-GaN Power Devices

- **Sandia is pursuing two pathways to v-GaN implementation**

For power module to operate at sum of its parts

- **Equitable current sharing is required**
- **Tight device binning may be necessary**
  - **Not just device parameters**
    - **Leakage**
    - **Turn-on voltage**
  - **Parasitic inductance and capacitance must be considered**
    - **Especially at high frequencies**

Paralleling of small-area die into power modules



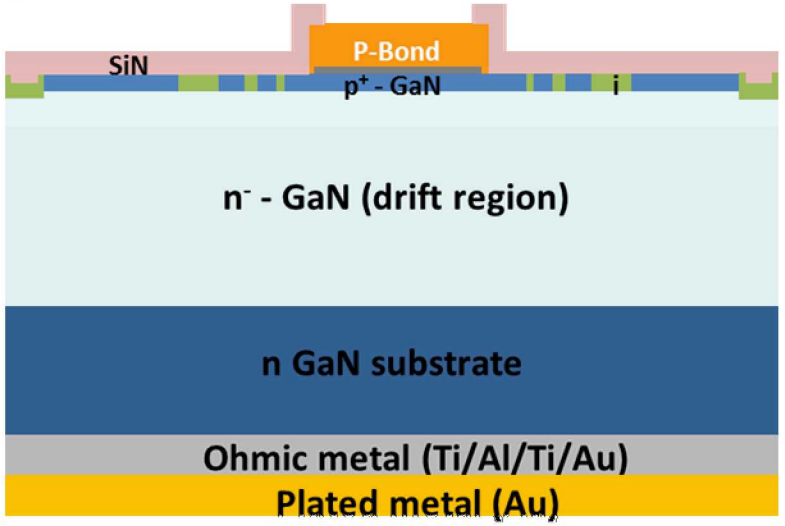
How does device variation affect power module performance?

Implementation into realistic power systems

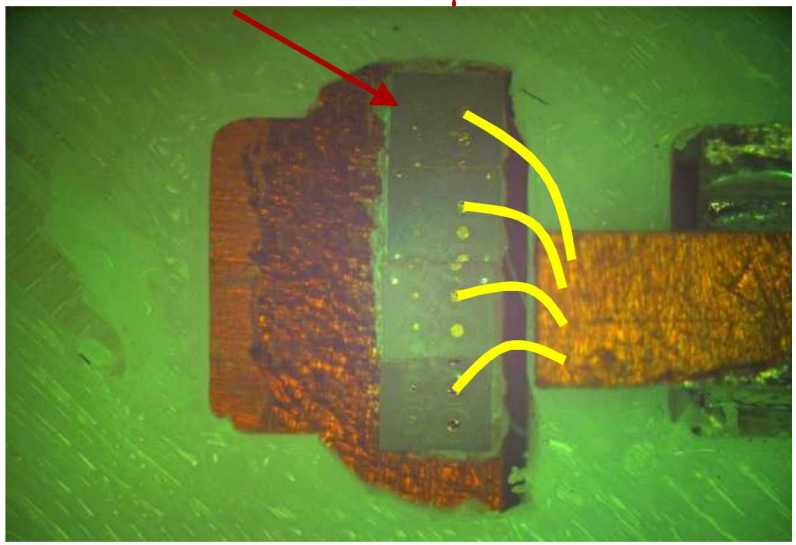
L. Rashkin, R. Brocato, J. Neely, J. Delhotal, J. Flicker, L. Fang, *et al.*, "Miniature High Voltage, High Temperature Component Package Development," presented at the IEEE Power Modulator and High Voltage Conference, San Francisco, CA, 2016 (*In Press*).

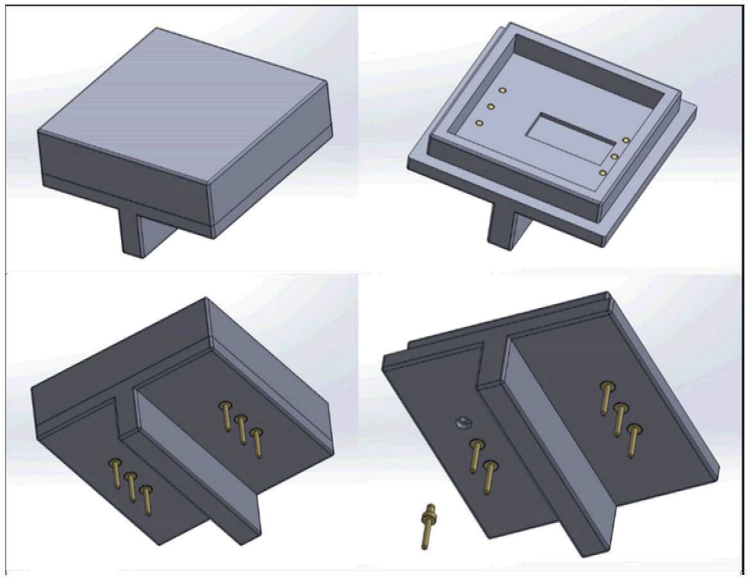
Paralleling of Diodes -- Experimental

- **v-GaN diodes**
  - **10 μm drift by MOCVD**
  - **150 μm contacts**
  - **600-1kV hold-off**
- **Closely matched IV curves power sharing**
  - **20% deviation at 3.4V**
- **Packaged in parallel via wire bond in 3D printed package**



Single chip has 4 isolated devices of sizes from 30 to 300 μm

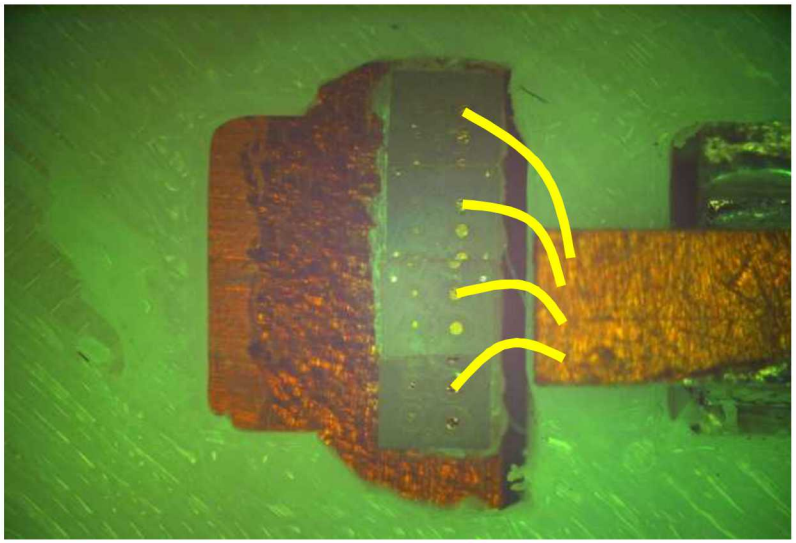


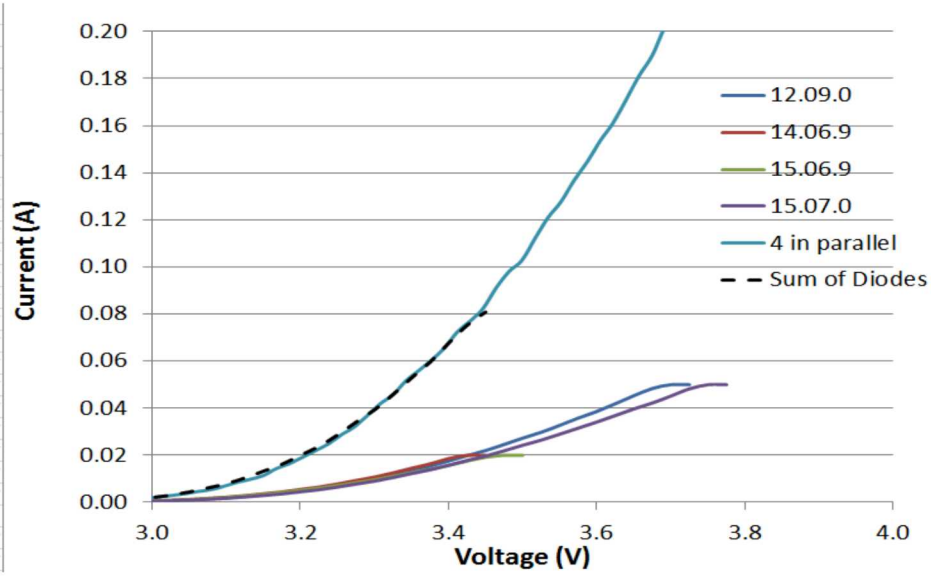


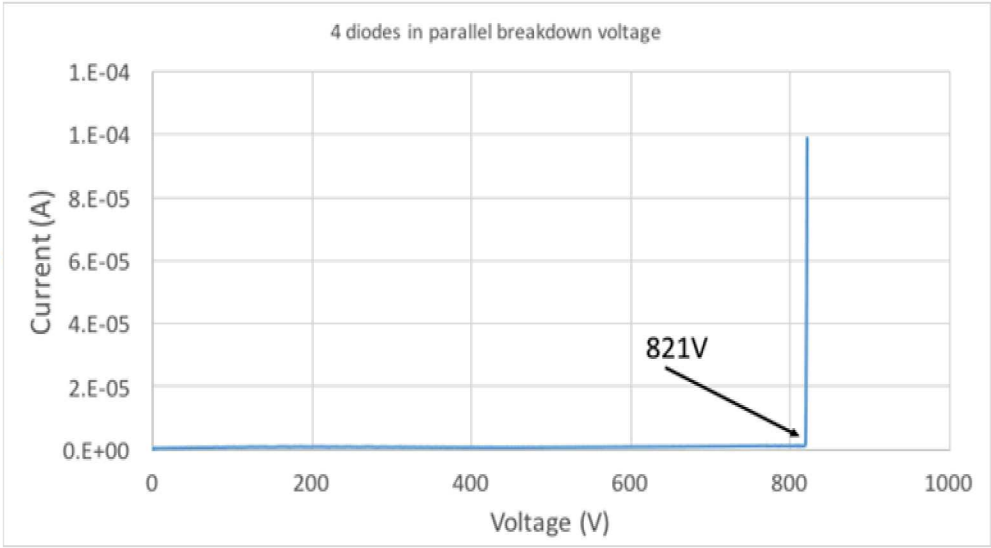
A. M. Armstrong, A. A. Allerman, A. J. Fischer, M. P. King, M. S. v. Heukelom, M. W. Moseley, *et al.*, "High voltage and high current density vertical GaN power diodes," *Electronics Letters*, vol. 52, pp. 1170-1171, 2016.

Paralleling of Diodes -- Experimental

- **Closely matched IV curves power sharing**
  - **20% deviation at 3.4V**
  - **Forward current of module is sum of diodes**
    - **indicates proper functioning of paralleled diodes**
  - **Module reverse breakdown of 820 V**



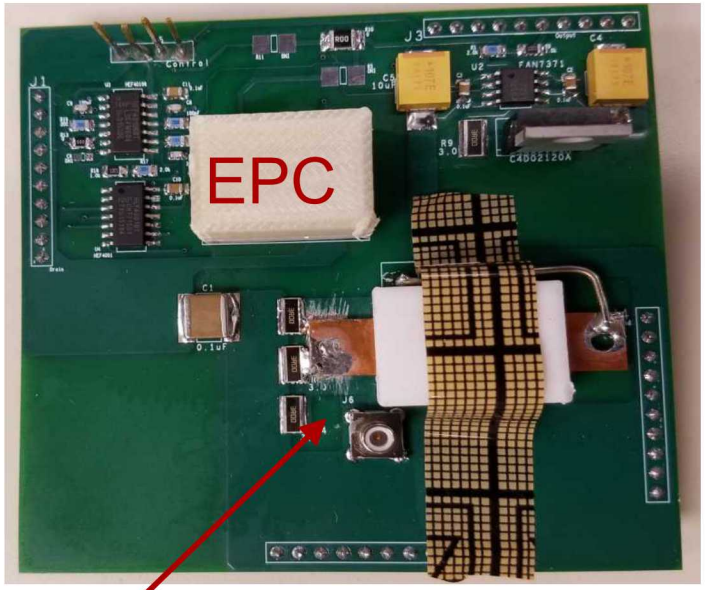




Paralleling of Diodes -- Experimental

- **Test the dynamic switching and current-carrying capabilities of the parallel diodes**
  - **Relevant power electronics circuit**
  - **buck converter test setup utilized**

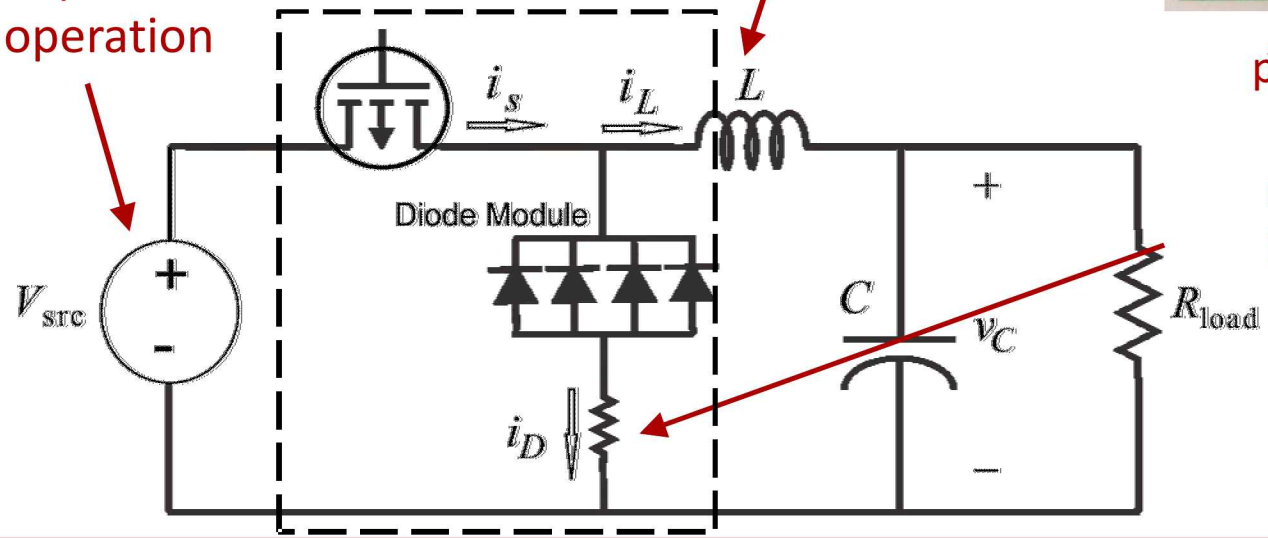
- **Paralleled v-GaN diodes packaged together with EPC GaN HEMT (300 V, 6 A)**



paralleled diode module

Large to characterize low current parts

Capable of 1200V operation

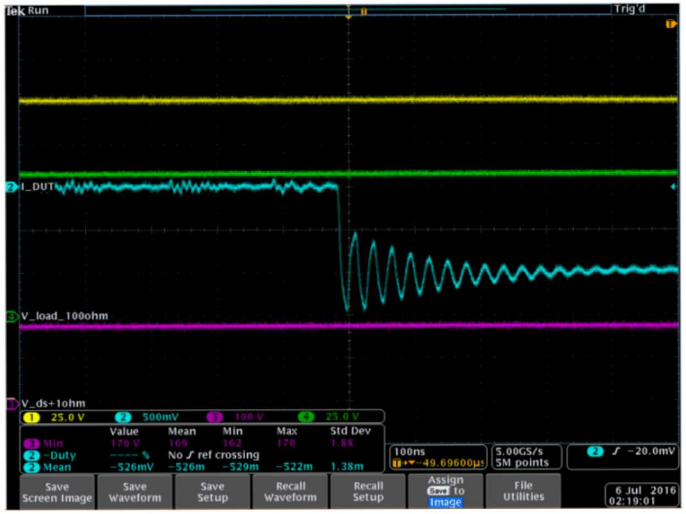


easured using a precision inductance 1Ω sense resistor

Efficiency Power Conversion (EPC), "eGaN FET Datasheet: EPC2015 - Enhancement Mode Power Transistor," Available: http://epc-co.com/epc/Portals/0/epc/documents/datasheets/EPC2025_datasheet.pdf Accessed: 09/29/2106.

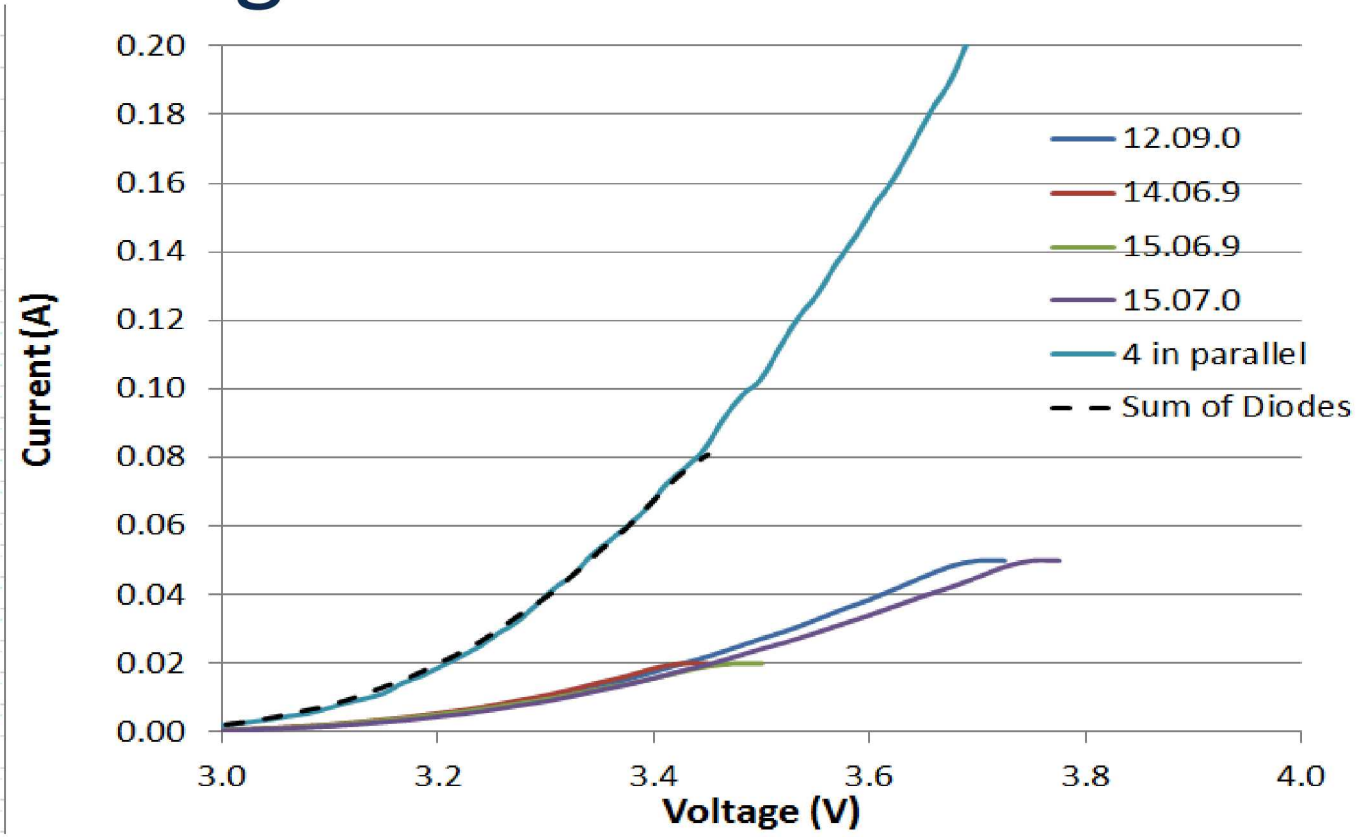
Paralleling of Diodes -- Experimental

- Buck converter operated at 15 kHz
- V_{src} = 240 V (limited by the HEMT)
- Continuous operation of the composite part with a peak current of 1.3 A (792 mA_{rms})
  - limited by the current rating of inductor
- Demonstrates non-negligible current handling by small-area v-GaN devices



Peak current (mA)	Average Current (mA)	RMS current (mA)	Duty Cycle (%)	Switching Freq (kHz)	Drain Voltage (V)	Power (W)
1000	413	423	49.7	15	179	62

Paralleling of Diodes -- Simulation

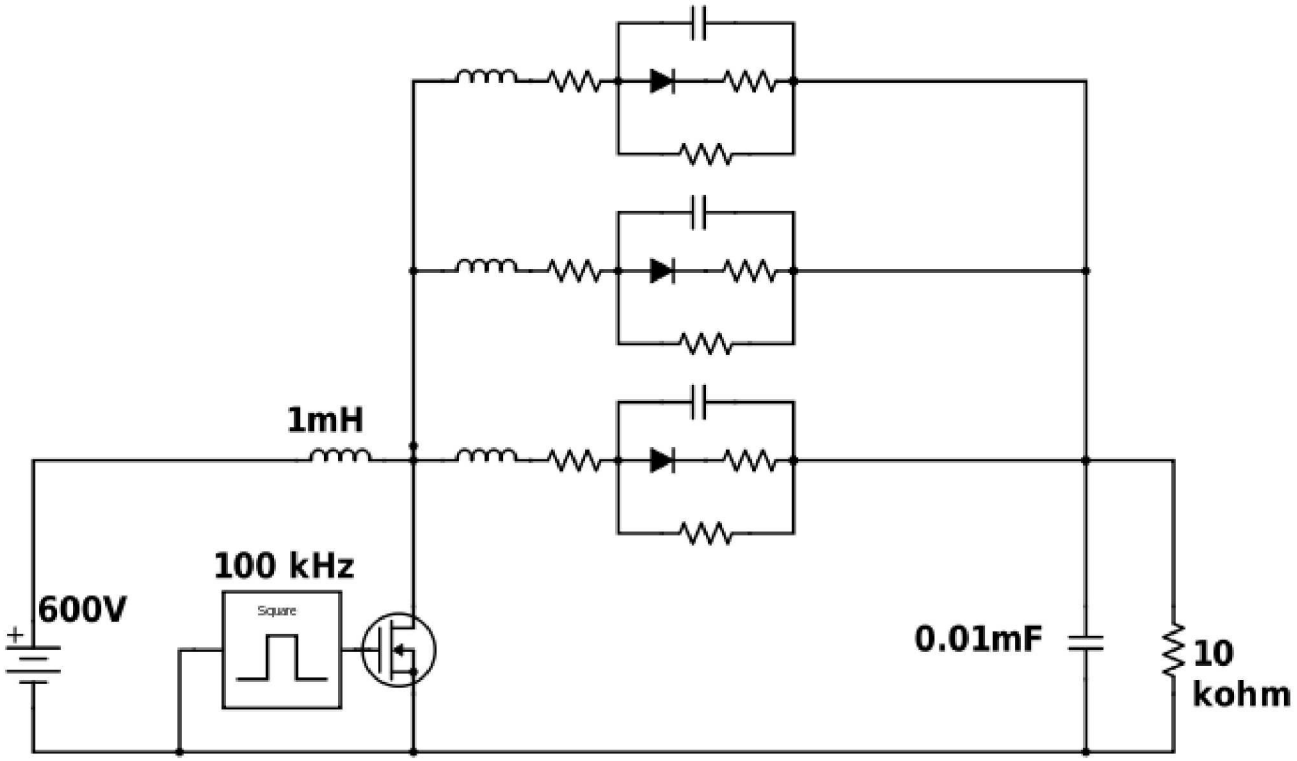


Significant work into screening and binning devices to match device parameters
Device matching necessary to ensure optimal current sharing
→ maximize system performance and reliability

How does device variation propagate to system performance?
What amount of binning is necessary for certain system performance?

Paralleling of Diodes -- Simulation

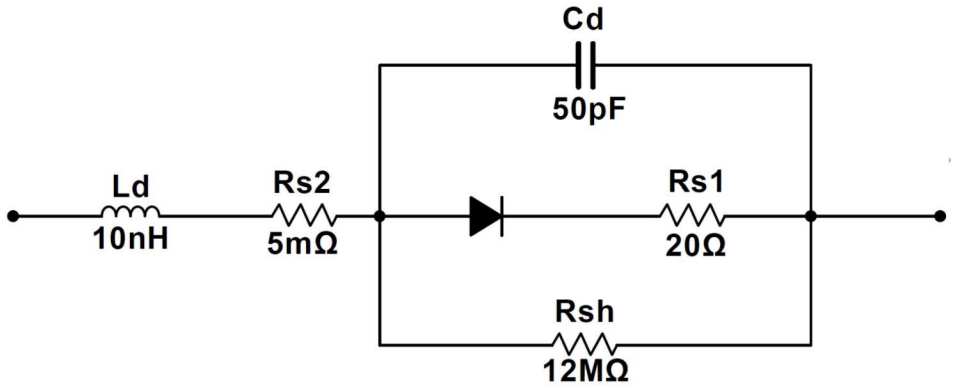
- To understand how parameter variation in diodes affects efficient current sharing
  → how closely devices must be binned in order to ensure system performance
- SPICE simulation was created
  - 600 V to 3 kV boost converter
  - operating at 3 kW and 100 kHz
- The conducting diode in this boost converter utilized 3 sets of parallel diode models



Paralleling of Diodes -- Simulation

- **The conducting diode in this boost converter utilized 3 sets of parallel diode models**
- **Parasitic values for resistance, inductance, and capacitance included**
  - **“Nominal” parasitic values from device measurements or calculated from materials properties**
- **Forward IV sweep carried out for diodes**
  - **T=25°C to 150°C in 25°C increments.**
  - **Parameters of the default SPICE model altered to best match measured IV curves for all measured temperatures**

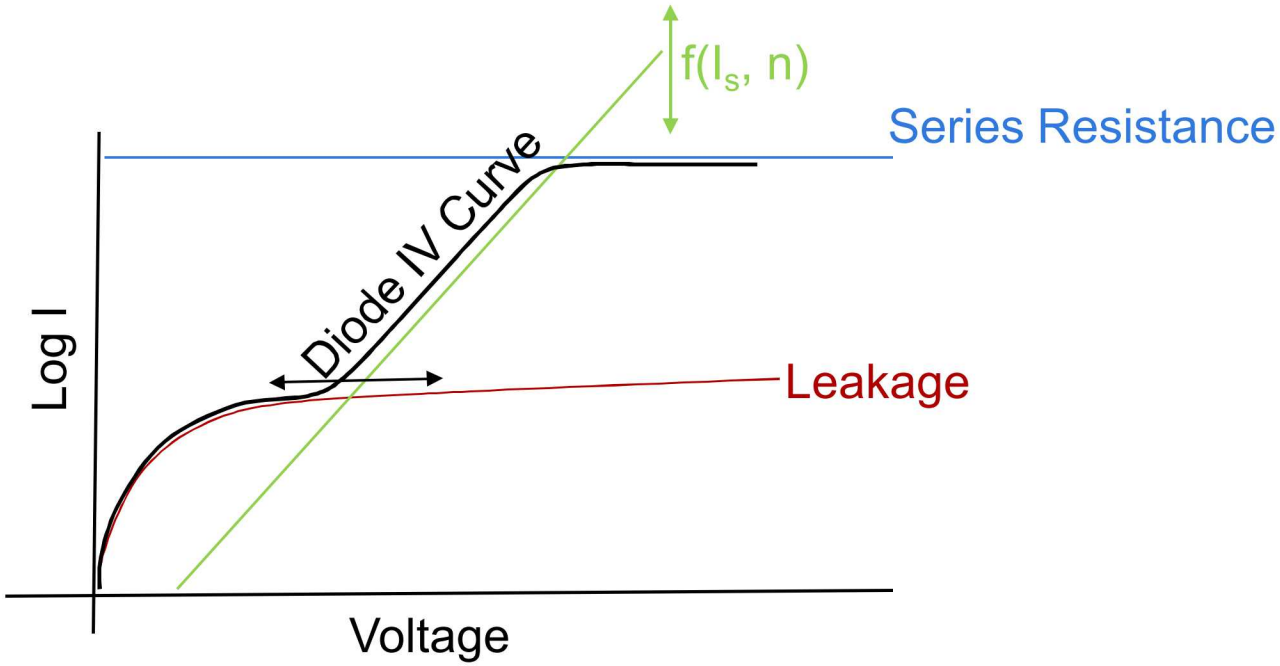
Parameter	Name	Value	unit
Ld	Inductance	10	nH
Cd	Capacitance	50	pF
Rs = Rs1 + Rs2	Series Resistance	20.05	W
Rsh	Shunt Resistance	12	MW



Paralleling of Diodes -- Simulation

- **Developed SPICE models for Sandia diodes**
  - **Offer good qualitative match at temperatures from 25-125°C**
  - **Best fit, not physics-based**
- **SPICE is designed for Si**
- **SPICE model for a diode based on ideal Shockley diode equation**

$$I = I_s \cdot (e^{(Vd)/n*Vt} - 1)$$



W. Shockley, "The Theory of p-n Junctions in Semiconductors and p-n Junction Transistors," *Bell System Technical Journal*, vol. 28, pp. 435-489, 1949.

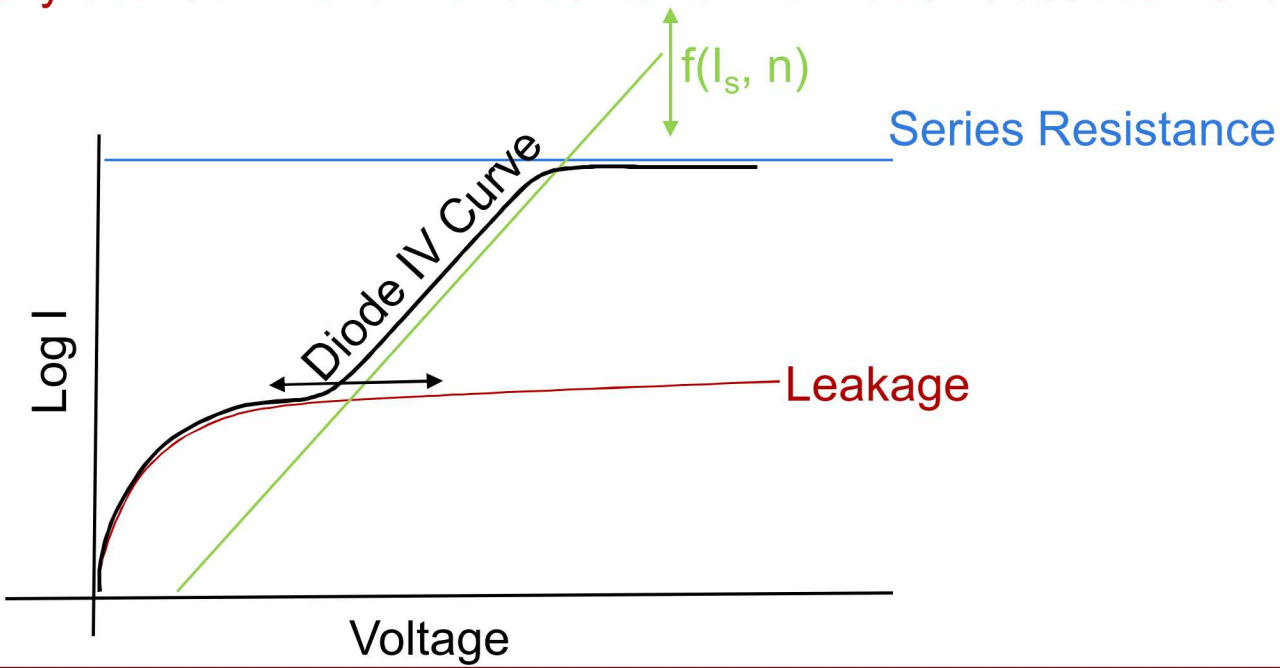
Paralleling of Diodes -- Simulation

- Standard Si p/n diode and has a turn-on voltage in the vicinity of 0.7 V
  - Match the GaN diode voltage turn-on >3V
    - Two methods of increasing the turn-on voltage:
      - Alter Saturation Current (I_s) or the emission coefficient value (n)

- I_s for GaN LED is in the region of 10^{-29} to 10^{-34} A
  - Most SPICE implementations only recognize $I_s > 10^{-30}$ A

  → may not be sufficient to describe the elevated voltage turn-on of WBG devices

- Both I_s and n had to be increased above the default Si values
  - n is typically between 1 and 2 and contains information about carrier transport



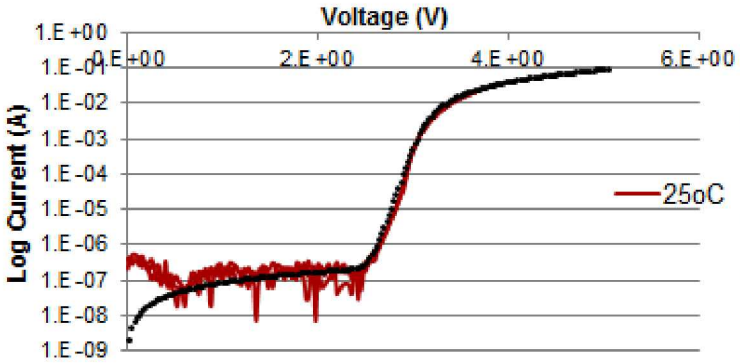
M. Xu, Q. Mu, L. Xiao, Q. Zhou, H. Wang, Z. Ji, *et al.*, "Temperature dependent current-voltage curves studey of GaN-based blue light-emitting diode," *Materials Express,* vol. 6, pp. 205-209, 2016.

Paralleling of Diodes -- Simulation

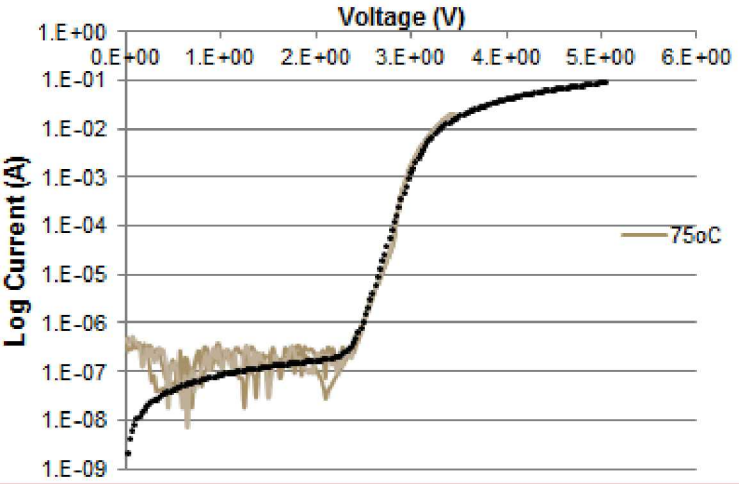
- **SPICE model matches with experimental data for all the measured temperatures**
- **Noticeable change in slope in the experimental curves**
  - **most likely due to a significant change in the diode emission coefficient (n)**

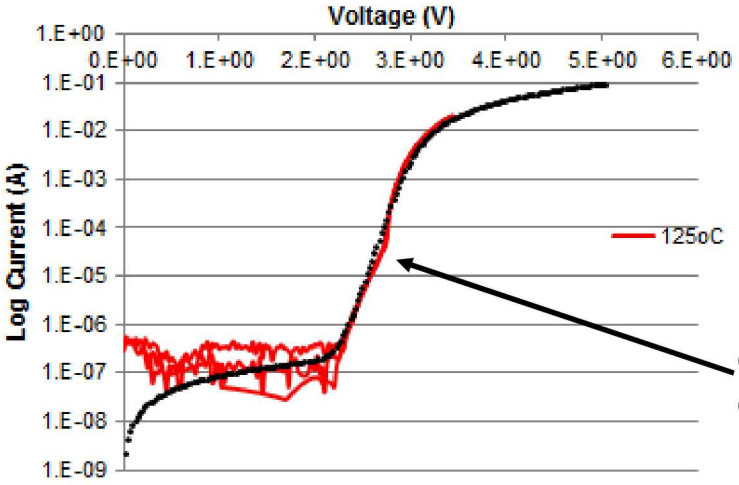
  → primary carrier transport from diffusion-dominated to recombination-dominated

  → not easily replicated in a single-diode model with a constant value for n



Parameter	Name	Value	unit
Is	Saturation Current	5E-27	A
Rs	Series Resistance	0	W
N	Emission Coefficient	2.2	-
Vj	Junction Potential	3.75	V
Eg	Bandgap	3.3	eV
XTI	Saturation-current Temp. Exponent	5	-

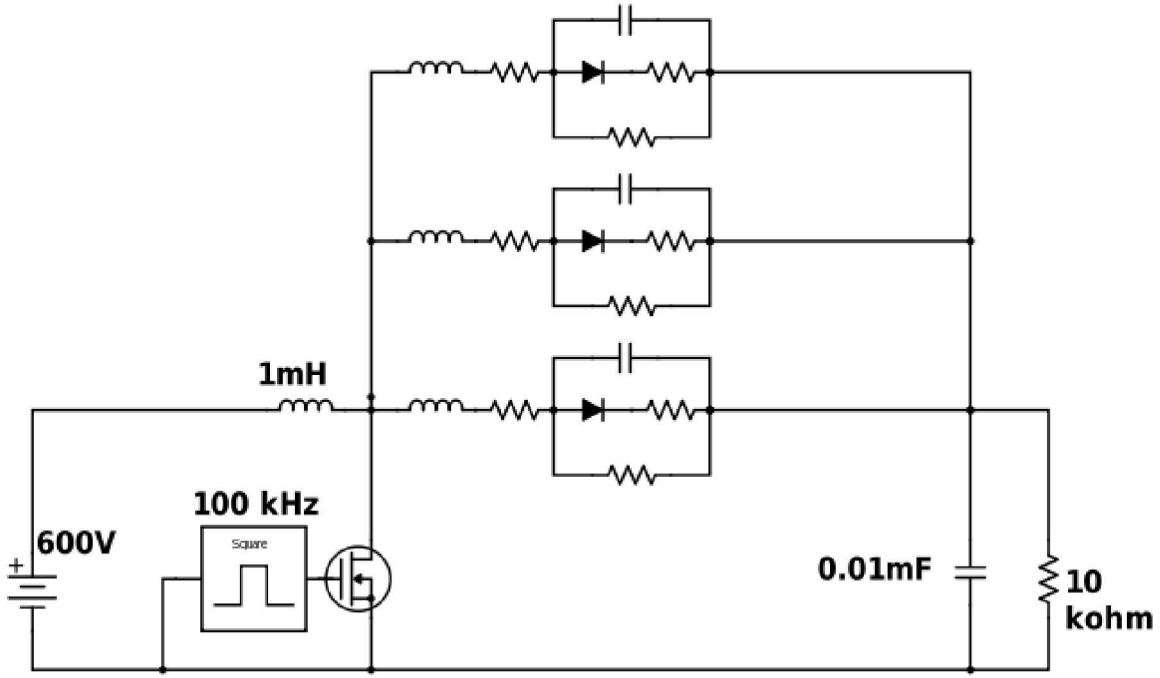




Paralleling of Diodes -- Simulation

- Used Diode Model to carry out Monte Carlo simulations using pSPICE
- Investigated effect of different binning thresholds (parameters within x% of nominal)
- Varied
  - series resistance
  - parasitic LC product
  - turn-on voltage

- Parameters assigned a continuous uniform distribution
- 35 ms of steady state operation of the boost converter (5 ns step sizes)



Paralleling of Diodes -- Simulation

- **The effect of parameter variation on current sharing determined by time average power dissipated in each diode (plus parasitics)**

$$P_i = \frac{\int_{t_1}^{t_2} I_d \cdot V_d}{t_2 - t_1} \quad \text{for i = 1, 2, 3…}$$

- **Fractional amount of power dissipated (F_i) calculated for each diode**

$$F_i = \frac{P_i}{\sum P_i} \quad \text{for i = 1, 2, 3…}$$

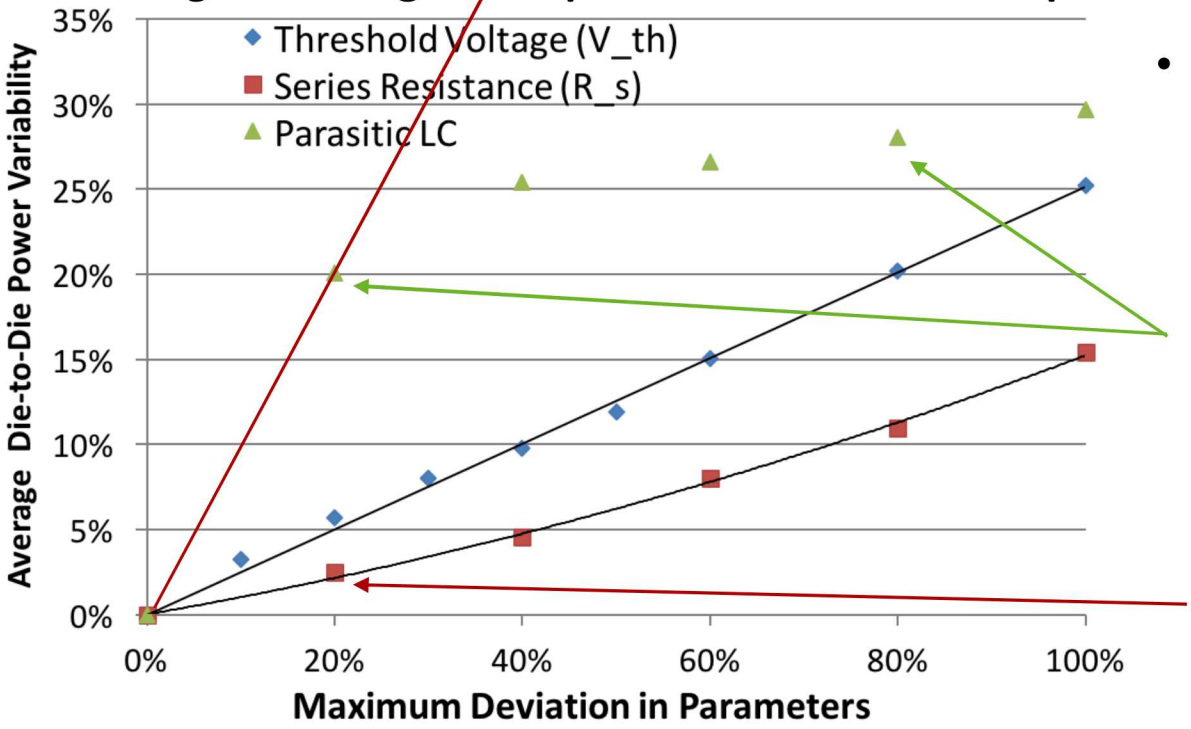
- **Current balance in the system for each run quantified by**

$$F_{max} - F_{min}$$

- **The average of this die-to-die power variation was calculated for all runs**

Paralleling of Diodes -- Simulation

- **Average maximum variation of power sharing vs. binning envelope of parameters**
  - ***e.g.* a binning envelope of 20% --> maximum parameter variation of 10% from nominal**



- **parasitic variation on power dissipation variability is sublinear**

LC product linear for small variations (< 20%), but for >20%

R_s: 20% deviation in devices <2.5% in average power dissipation

- **Sublinear relationship between device parasitics and power dissipation indicates power modules should be relatively robust to device variations**
- **Final systems can operate with relatively liberal variations in parasitics**
  - **due to by manufacturing variations or binning requirements**
- **Important for the future use of WBG devices as it may allow many devices to be paralleled regardless of the specific parasitics**

Summary

Sandia National Laboratories

- Constructed power module of four v-GaN diodes wired in parallel
  - Demonstrated current sharing with both static and dynamic measurements
  - Operating the diode power module in a 240-to-100V buck converter
    - 15 kHz and 50% duty cycle.
    - Peak current of 1.3 A (782 mA_{rms}) without failure

- Examined effect binning individual parts has on total module operation
  - Developed SPICE model for GaN diodes operating in a boost converter
  - Carried out Monte Carlo simulations measuring variability in die-to-die power handling
    - turn-on voltage
    - parasitic LC product
    - series resistance

- Parameter variation has a sublinear relationship with average die-to-die power variation
  - Variations in parameters up to 100% result in < 30% die-to-die power variation
  - Indicates power module is relatively insensitive to individual device parasitics
    - Device parasitics need not be perfectly matched for high performance modules

Acknowledgements

Sandia National Laboratories is a multi-mission laboratory managed and operated by Sandia Corporation, a wholly owned subsidiary of Lockheed Martin Corporation, for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.

The contribution of the entire UWBG Grand Challenge team and the support of the Sandia LDRD office are gratefully acknowledged

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