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Total Ionizing Dose Effect Study on Radiation-Hard Power MOSFET Device

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Abstract

TID study on radiation-hardened power MOSFET was carried out as a function of total dose, dose-rate, device state, and annealing time. Experimental data was correlated to interface trap and oxide charge density using TCAD simulations.

Introduction

- Commercially available, radiation-hardened, planar, vertical double-diffused power MOSFETs continue to be used pervasively for space and strategic applications.[1]
- Despite the engineered radiation hardness, these devices are susceptible to TID effects. The primary degradation mode due to ionizing radiation exposure is a shift in the threshold voltage (ΔV_T).
- This work examines and compares post-irradiation test data and simulation results for transistors exhibiting significant defect growth and annealing effects due to TID.

Experimental Details

Radiation Sources & Dosimetry:

- GIF: Co-60 source at 250 rad(Si)/s with total measurement uncertainty < 10%
- LINAC: Nominal electron energy 20 MeV; dose-rate 1.1e10 and 1.1e11 rad(Si)/s with pulse width ranging from 9 µs – 36 µs. Measurement accuracy ±10%

Devices & Measurement:

- International Rectifier's NMOS power MOSFETs IRHNJ53130 with "moderate" TID hardness of 300 krad (Si).
- GIF: V_{GS} = -6V (off-state), +6V (on-state), and 0V with V_{DS} = 28V. Samples accumulated TID from 100 krad to 1Mrad with intermittent I–V measurements
- LINAC: V_{GS} = -6V (off-state), +6V (on-state) with V_{DS} = 28V. Individual devices exposed to 100, 200, 500, and 1000 krad(Si). [No dose accumulation as in GIF case.]
- Pre- and post-irradiation I_D–V_{GS} and I_D-V_D sweeps using Keysight B1505A parametric analyzer

Simulation Set Up

- 2D TCAD simulations of power MOSFET devices were performed using CHARON.
- A normal-environment device calibration was performed by modifying junction doping and its placement, SD parasitic resistance, mobility, and saturation velocity parameters

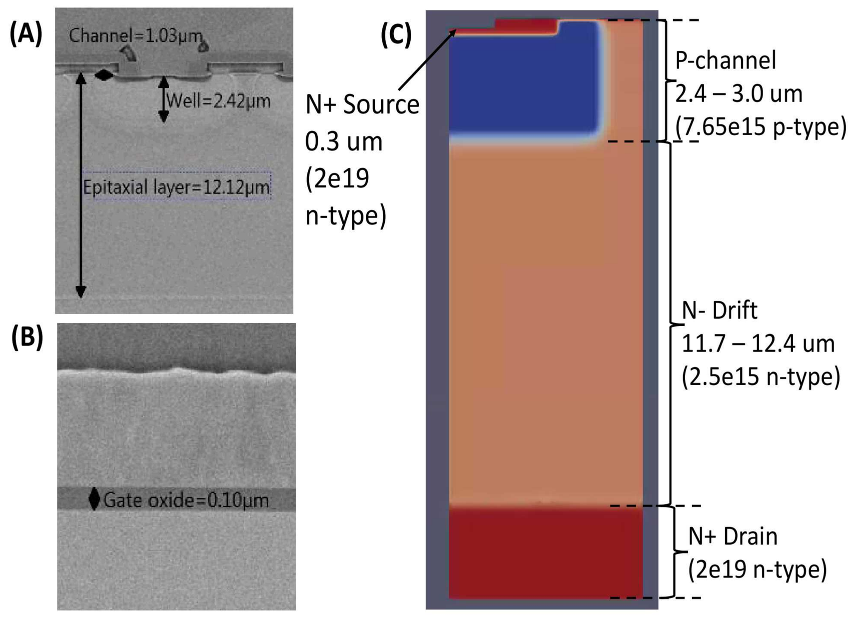

Fig. 1 Cross-sectional SEM of NMOS power MOSFET device showing (A) junction depths, channel length and (B) gate oxide thickness. (C) Junction doping and placement used for TCAD calibration.

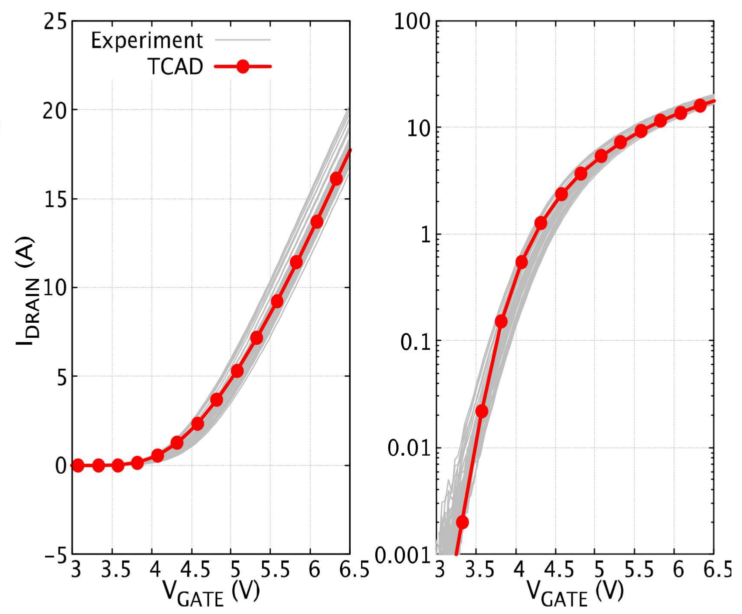

Fig. 2 I_D—V_{GS} plot showing match between experimental data (gray lines) and TCAD simulation (red) on linear (left panel) and semi-log (right panel) scales.

Results & Discussion

Time-Dependent Response:

- ΔV_T shows Log(t) recovery rate irrespective of V_G and dose-rate [2,3]
- Annealing rate [slope of ΔV_T versus log(t)] is lower for -V_{GS} condition than for +V_{GS} condition explained by tunneling of electrons from silicon into the oxide traps. [4]
- For –$V_{GS,}$ charge centroid near gate; for +V_{GS} charge centroid near silicon channel; Capture cross-section decreases exponentially with distance from the channel interface [5]

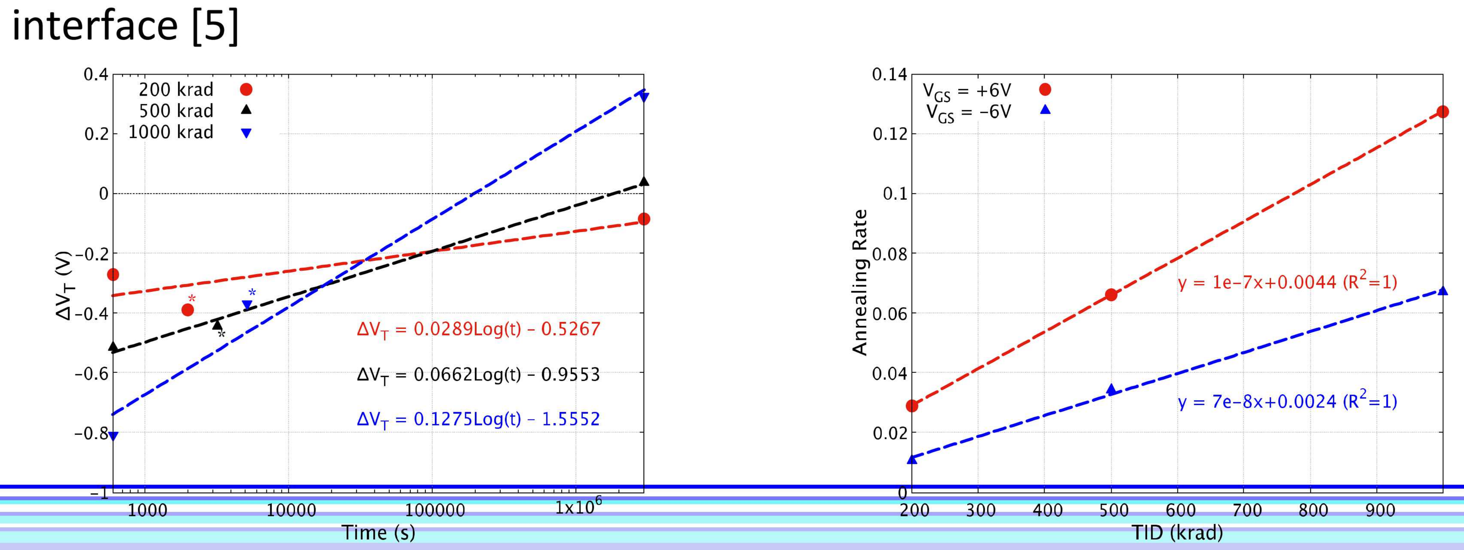

Fig. 3 (Left) ΔV_T as a function of post-irradiation annealing time; devices were irradiated at V_{GS} = 6V. (Right) annealing rate as a function of TID for V_{GS} = +6 and -6V.

Threshold Voltage v/s TID Response:

- For a given V_{GS}, max. ΔV_T for GIF devices is half compared to that for LINAC devices. This is due to longer exposure time (low dose-rate) and longer measurement delay at GIF facility leading to longer sample annealing time.
- GIF data as a function of TID reveals larger ΔV_T for +V_{GS} conditions relative to the -V_{GS} condition. This is related to oxide charge centroid location (Fig. 5, left panel).

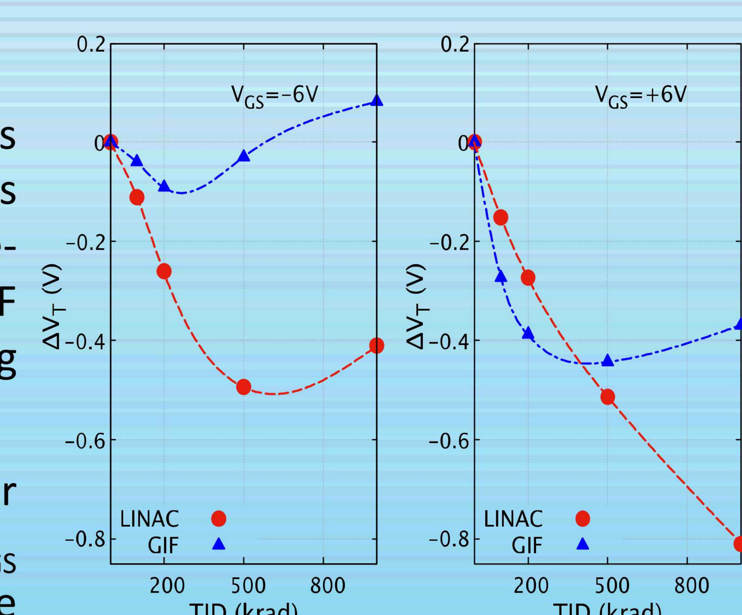

Fig. 4 ΔV_T vs. TID for LINAC and GIF samples with V_{GS} = -6V (left panel) and V_{GS} = +6V (right panel) during irradiation.

- GIF V_{GS} = -6V condition at 1 Mrad shows V_T rebound of about 100 mV indicative of buildup of radiation-induced acceptor-type trap states at the Si/SiO2 interface.
- TCAD results of ΔV_T as a function of interface trap density (Fig. 5, right panel) indicate an interface trap density of 3–4x10^{10}/cm^2 for 100mV ΔV_T. [6]
- ΔV_T for LINAC samples (red curves, Fig. 4) is nearly the same up to 500 krad TID for both V_{GS} cases and needs further investigation.

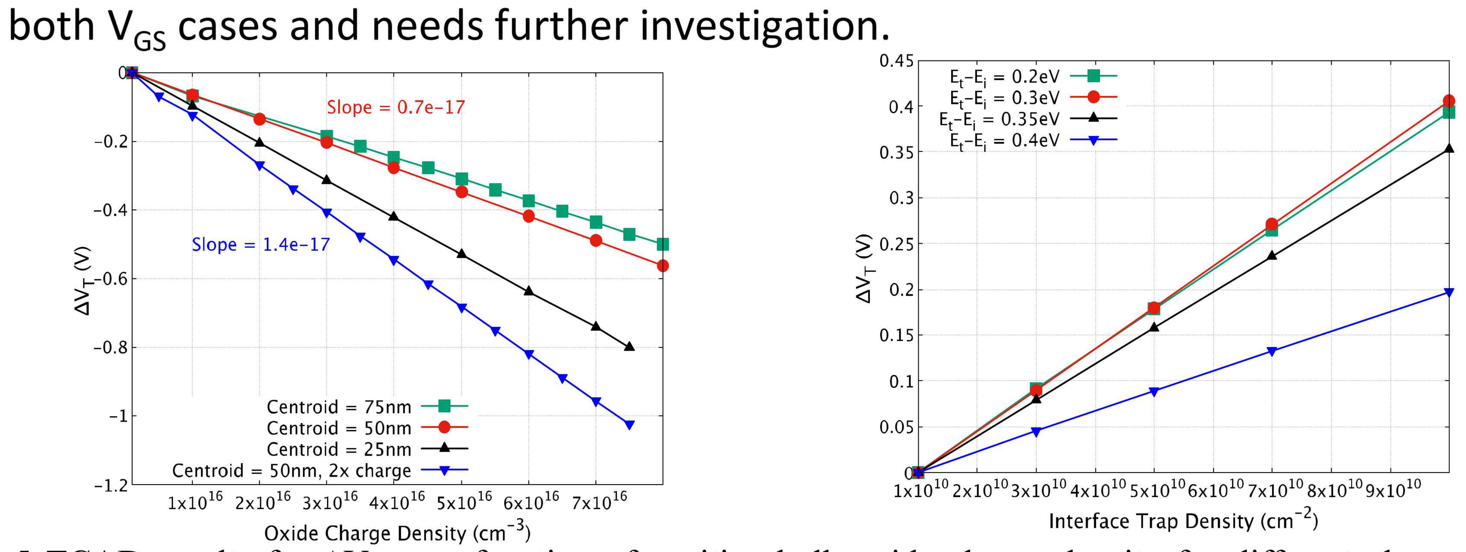

Fig. 5 TCAD results for ΔV_T as a function of positive bulk oxide charge density for different charge centroid locations (left) and interface trap density for various energy locations in the band-gap (right).

V_{GS} = 0V During Irradiation at GIF:

- V_T recovery slightly above 200 krad and a strong rebound for higher TID levels. ΔV_T rebound of 300 mV at 500 krad suggests an interface trap density of ~ 8x10^{10}/cm^2 (Fig. 5)
- At the 1 Mrad condition, a ~350mV positive shift in I_D–V_{GS} curve attributable to negative bulk oxide[7] charge and accounts for nearly all of the rebound effect w.r.t the 500 krad sample

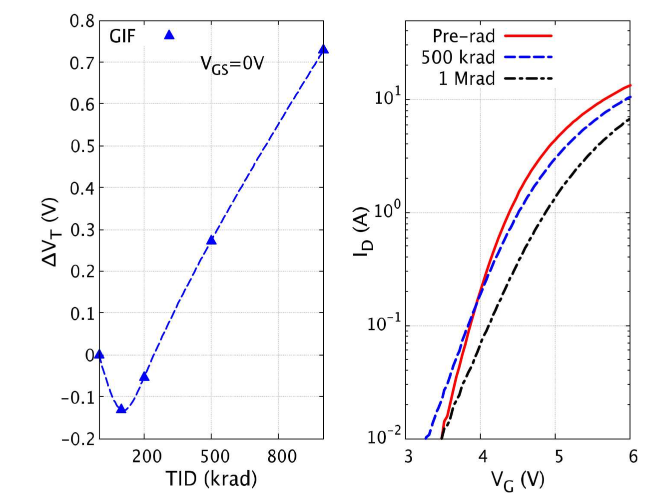

Fig. 6 ΔV_T versus TID for V_{GS} = 0V sample irradiated at GIF (left panel), and corresponding I_D–V_{GS} measurements (right panel).

Conclusions & Future Work

- RT annealing indicate ΔV_T recovery rate of NMOS power MOSFET devices linear with TID up to 1 Mrad, independent of dose rate.
- For V_{GS} ≠ 0 GIF samples, ΔV_T versus TID trends consistent with the TCAD results for various charge-centroid locations and acceptor-type interface traps
- For LINAC samples, however, the ΔV_T magnitudes were the same (up to 500 krad TID) irrespective of gate bias during exposure and require further verification/assessment
- GIF V_{GS}=0V sample exhibited strong V_T rebound for TID > 200 krad. Post-TID I_D–V_{GS} characterization reveals formation of acceptor-type interface traps and formation of negative bulk oxide charge.

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