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Electro-thermal Simulation and Performance Comparison of 1.2 kV, 10 A Vertical GaN MOSFETs

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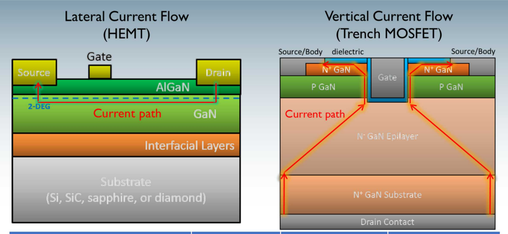
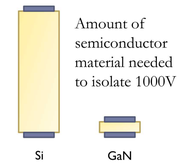
Introduction – Need for Vertical GaN

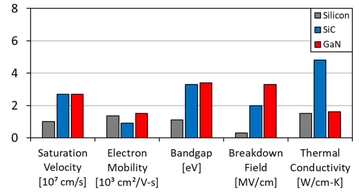
Gallium Nitride (GaN) as compared to Si, SiC and GaAs has been shown to exhibit superior material properties attractive to semiconductors, especially relating to high-power applications. Traditionally, GaN has been used to develop lateral high electron mobility transistors (HEMTs) built on non-native substrates, however, these substrates can limit device performance. It is only recently that the prospect of vertical GaN devices through the development of bulk GaN substrates has become possible.



10x Improvement!

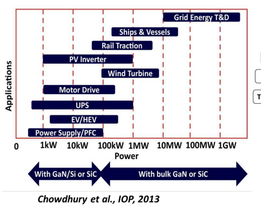


Amount of semiconductor material needed to isolate 1000V

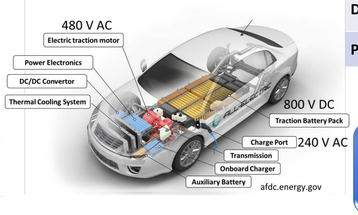


Attributes	GaN-on-Si	GaN-on-SiC	GaN-on-GaN
Defect Density (cm^{-2})	10^9	10^8	10^3 to 10^6
Lattice Mismatch %	17	3.5	0
CTE Mismatch %	54	25	0
Breakdown Voltage (V)	< 1000	< 2000	> 5000
Capable of Avalanche	No	No	Yes
Device Types	Lateral	Lateral	Vertical and Lateral
Production Cost	Low	High	Highest

I.C. Kizilyalli *et al.* / Microelectronics Reliability 55 (2015) 1654-1661



Chowdhury et al., IOP, 2013



100 kW Electric Traction Drive System

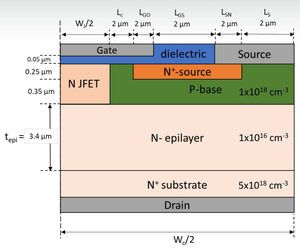
Power density of 33 kW/L (10X improvement)

Cost of $6/kW (50% cost reduction)

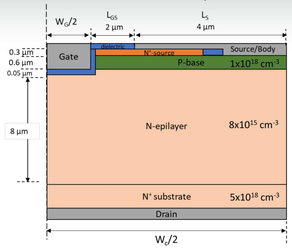
Operational life of 300,000 miles (2X improvement)

Device Design & Simulation Model

Double-well MOSFET Cell Width = 22 µm



Trench MOSFET Cell Width = 14 µm



Larger cell width in DMOS = Increased specific on-resistance.

GaN Simulation Parameters and Values

Symbol	Quantity	Value
E_g	Bandgap	3.44 eV
ε_s	Relative Permittivity	9.7
T	Temperature	300 K
μ_p	Hole Mobility	11 cm^2/Vs
μ_n	Electron Mobility	1200 cm^2/Vs
k	Thermal Conductivity	$1.3\left(\frac{T}{300K}\right)^{-0.28} \frac{W}{cm \cdot K}$
R_{J-C}	Junction-to-Case Thermal Resistance	5 °C/W

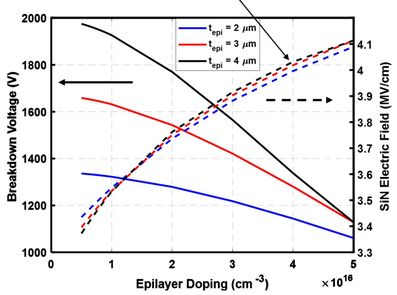
	SiN	SiO_2	Al_2O_3	AlN
Dielectric Constant	7.5	3.9	9.3	8.5
Dielectric Breakdown (MV/cm)	7-10	10	4-8	3-6

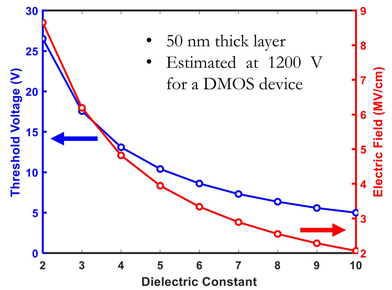
Must design in a factor of safety for dielectric breakdown
E-field SiN ≤ 4 MV/cm

Punch through device

- Electric field in the nitride is only a function of doping
- Thickness of drift layer has strong impact on breakdown at low doping

Dielectric E-field limit occurs at 4e16 cm^{-3} doping



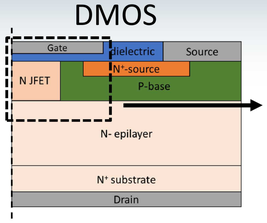


SILVACO

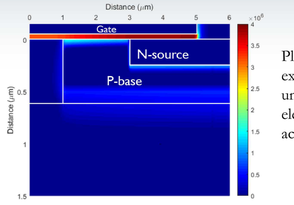
Results & Discussion

Electric Field Management

DMOS



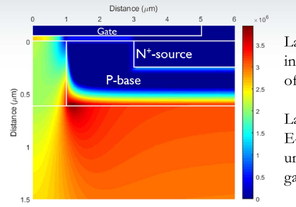
On-State



Planar device exhibits uniform electric field according to:

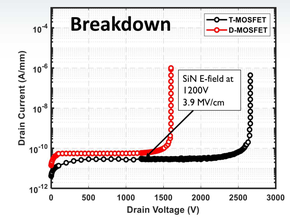
$$E = \frac{V}{d}$$

Off-State

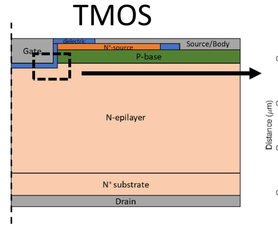


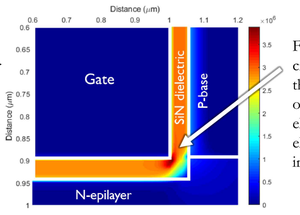
Large field occurs in GaN at corner of JFET region

Largest dielectric E-field occurs under center of gate

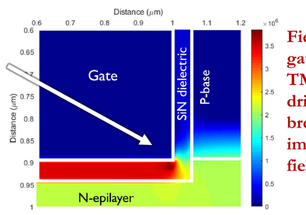


TMOS

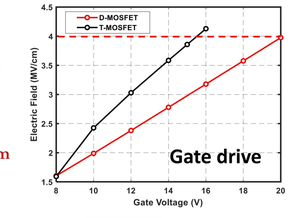




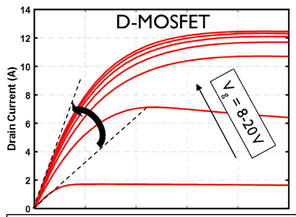
Field crowding at the corner of the gate elevates electric field in dielectric



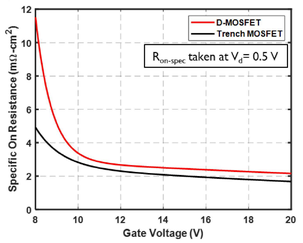
Field crowding at the gate corner in the TMOS limits the gate drive voltage and the breakdown based on imposed dielectric E-field limit of 4 MV/cm



On-Resistance

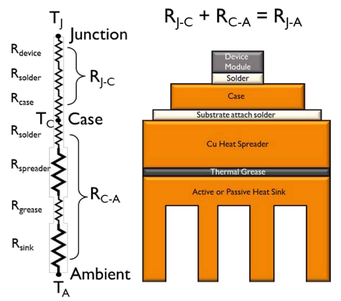


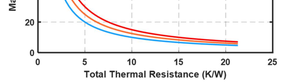
Higher gate voltages reduce on-resistance, but increase electric field

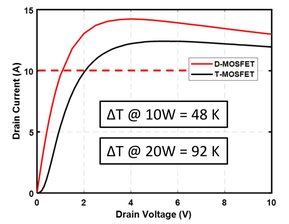


Thermal Design

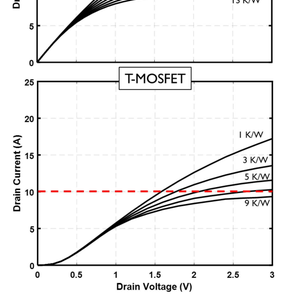
Determine temperature of operating environment and maximum allowable junction temperature







TMOS dissipates twice as much power in order to achieve 10 A operation!



Increasing thermal resistance significantly reduces electrical performance due to enhanced carrier scattering and reduced mobility

Conclusions

- Both devices are capable of achieving 1.2 kV blocking and 10 A current capacity
- T-MOSFET breakdown must be over designed in order to compensate for field crowding
- D-MOSFET design allows for reduced power dissipation for a given gate width
- From a thermal and power handling capability it appears the D-MOSFET performs better
- The D-MOSFET requires a difficult etch and regrowth or double implantation to fab, whereas the T-MOSFET does not
- Device fabrication and test structures to determine dielectric breakdown and channel mobility are currently underway

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