Dynamic Model of Active Front-End Converters with 2DOF-PI Controllers for DC Bus Voltage Control

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***Abstract*—In most of the research, a conventional one degree-of-freedom type proportional-integral controller (1DOF-PI) is used for the regulation of the dc bus voltage in an Active Front-End Converter (AFEC). This paper proposes a two degree-of-freedom type proportional-integral controller (2DOF-PI) for the regulation of dc bus voltage in an AFEC. Such a controller eliminates the left-half plane (LHP) zero in the command-to-output transfer function for dc bus voltage regulation that is inherent to the conventional 1DOF-PI for this application. The dynamic model of an AFEC in the synchronous reference frame (SRF) is presented. An inner current control and outer dc voltage control loop is built for controlling the AFEC. Vector-control scheme is employed to achieve decoupled control of *direct*-axis and *quadrature*-axis currents. The outer dc voltage control loop is designed with a 2DOF-PI to complete the control system. Transfer function (TF) of the controller is derived based on the presented model and used to calculate the controller gains. Transient and steady state performance of the designed controllers are investigated in MATLAB/Simulink and results presented.**

Keywords—degree-of-freedom, 2DOF-PI, Active Front-End Converter (AFEC)

I. Introduction

The degree of freedom of a control system is the number of closed-loop transfer functions which can be adjusted independently [1]. When designing control systems, the design engineer must satisfy several objective functions to obtain optimum plant performance, therefore higher degree-of-freedom systems are naturally desired [2]. Proportional-integral controllers are ubiquitous in the control industry and they are often the controller of choice in power electronic applications too. Because of the simplicity of design and ease of implement, PI-controllers have been used for several different applications in all power ranges for decades. Unsurprisingly, they are also the most popular controller in active front-end converters (AFEC) and active rectifiers where they are used for both ac current control and dc voltage control in the synchronous reference frame (SRF) [3-8].

The conventional proportional-integral (PI) controllers, also referred to as the one degree-of-freedom PI controllers (1DOF-PI), are of the structure shown in Fig. 1(a) where *r(s)* denotes the reference input, *y(s)* denotes the system output, $G_p(s)$ denotes the plant transfer function and *u(s)* denotes the controller output. The control output *u(s)* of the 1DOF-PI is given by equation (1) where K_p is the proportional gain and K_i the integral gain. These types of 1DOF-PI are by far the most popular compensators used today as they can solve a wide range of control problems and are easy to design and implement [2]. However, there are limitations to this PI control structures; one of which is that the set-point response and the disturbance response cannot be independently optimized [9]. During step change in reference input, although zero steady-state error may be achieved, the transient performance can be degraded due to compromised disturbance rejection capability. A two degree-of-freedom type PI controller (2DOF-PI) can overcome this issue by allowing the design engineer with added freedom of attenuating the sensitivity function in low-frequency range while not affecting the tracking performance [9].

$$u(s) = (K_p + \frac{K_i}{s})(r(s) - y(s)) \tag{1}$$

$$u(s) = \frac{K_i}{s} r(s) - \left(K_p + \frac{K_i}{s}\right) y(s) \tag{2}$$

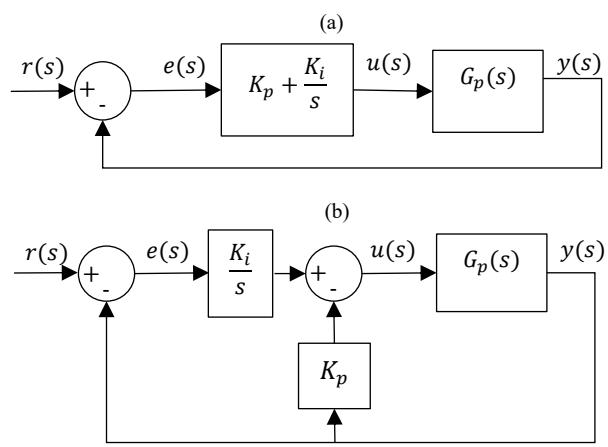

Fig. 1. Controller Block diagram for (a) one degree-of-freedom type PI (1DOF-PI) controller, and (b) two degree-of-freedom type PI (2DOF-PI) controller

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Fig. 1(b) shows the structure of a 2DOF-PI where the integral path with gain K_i/s forms the serial compensator and the proportional path with gain K_p forms the feedback compensator. While there are several equivalent transformations of the 2DOF-PI [9], the one depicted in Fig. 1(b) is the feedback-type and is preferred in this paper due to its simplicity and design proximity to the 1DOF-PI of Fig. 1(a). Output *u(s)* of the 2DOF-PI in terms of its proportional gain K_p, integral gain K_i, reference *r(s),* and output *y(s)* is given by equation (2). The controller given in Fig. 2(b) is said to have two degrees of freedom (2DOF) because the signal path from reference *r(s)* to control *u(s)* is different from the signal path from output *y(s)* to *u(s)* [2]. Compared to the 1DOF-PI, the use of 2DOF-PI is rarely seen in literature or in the industry. In [11], a 2DOF-PI was used for current control of a voltage source converter as a means for deadtime compensation. In [5], a robust 2DOF feedforward control scheme was used to regulate the load voltage irrespective of the load dynamic in an islanded microgrid.

Of all the PI-controllers applied in power electronics a vast majority are of the 1DOF-PI type [3-9][14-15]. Despite its popularity, the 1DOF-PI when applied to the outer voltage control loop of an AFEC introduces a left half plane (LHP) zero in the command-to-output transfer function at the location K_p/K_i [6][10]. The resulting response of the closed loop system is dependent on the natural frequency and the damping ratio [13], but is also dependent on the LHP zero that introduces an over- or undershoot in the output dc voltage for a step change in reference input [2]. While all three quantities – natural frequency, damping ratio and LHP zero - impact the systems responses, all three are a function of the two controller gains, K_p and K_i, of the 1DOF-PI, as will be shown later in this paper. This is a major limitation of the 1DOF-PI for dc bus voltage regulation, as the design engineer does not have the freedom to place the two poles and the single zero of the system arbitrarily. In [7], the LHP zero is ignored altogether while in [10], the pole-zero cancellation technique has been used to compensate for its effects. However, in the pole-zero cancellation technique the speed of the dynamic response may be limited by the location of the LHP and the method introduces further design complexity. The work presented in this paper shows that when a 2DOF-PI of the structure shown in Fig. 1(b) is used, the LHP zero is eliminated from the closed-loop transfer function, thus improving the system response during step change in dc bus voltage reference, while also providing the same dynamic response and steady state performance as the 1DOF-PI counterpart in all other cases. To the best of the author's knowledge, 2DOF-PI for dc bus voltage regulation has only been used in [15]. Although the presence of the overshoots in the 1DOF-PI and its absence in the 2DOF-PI has been mentioned in [15], no further analysis was presented, and neither is the LHP zero discussed. Further in [15], the fictitious reference iterative tuning (FRIT) is implemented as an offline tuning method based upon particle swarm optimization (PSO) which is complicated to implement and does not take the transfer function of the closed-loop system into account.

The purpose of this paper is to propose a 2DOF-PI as an alternative to the convention 1DOF-PI in an AFEC applications for dc voltage regulation. A detailed analysis of the open and closed-loop transfer function is presented and mathematical equations for the controller gain selection is derived based on the transfer functions. A dynamic model of a three-phase grid-tied AFEC in the SRF with an inductive output filter is presented in the next section. While the concepts presented are applicable to any topology, a two-level three-phase converter is chosen due to its simplicity and popularity.

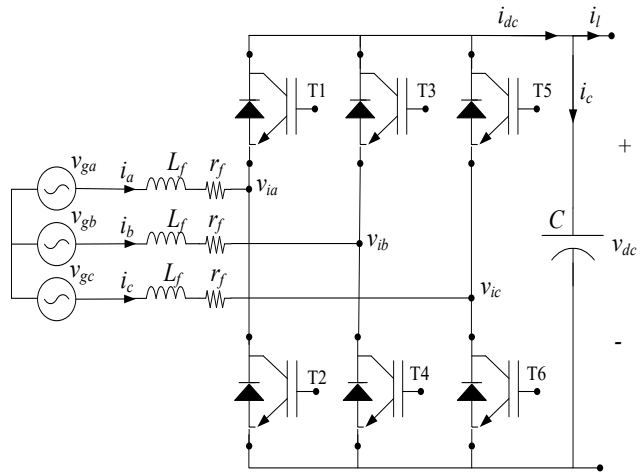

Fig. 2. Circuit diagram of a two-level three-phase active front-end converter (AFEC)

II. Dynamic Model of AFEC

A. Circuit Description

The electrical circuit diagram of a two-level three-phase AFEC is shown in Fig. 2. In the figure, the inverter is connected to the grid through an inductive filter with inductance L_f and internal resistance r_f. The circuit presented is a three-wire system without a neutral wire therefore *zero*-sequence current cannot flow in the circuit regardless of the applied three-phase voltages. The absence of *zero*-sequence currents justifies the omission of the analysis of *zero*-sequence components in the system study [3]. The three grid phase voltages ($v_{ga,}\, v_{gb,}\, v_{gc}$) are sensed on the grid sides of the *L*-filters and the three line currents ($i_{a,}\, i_{b,}\, i_c$) through the filters are also sensed along with the dc link voltage (v_{dc}) and dc load current (i_l). dc Capacitor with capacitance C is present on the dc bus to filter out the high frequency component from the dc current. The connected dc load is not shown in the circuit; however, the dc load current is shown as positive flowing out of the positive node of the dc bus. The sensed voltages and currents are fed to the controller and used to determine the PWM gate signals ($T_1 - T_6$) that are used to modulate the six IGBT switches as shown in the figure.

Applying KVL to the circuit shown in Fig. 2 and rearranging yields equation (3) where the quantities $[v_{ia}\ v_{ib}\ v_{ic}]^{\mathrm{T}}$ indicate the phases voltages at the inverter terminal, $[v_{ga}\ v_{gb}\ v_{gc}]^{\mathrm{T}}$ indicate the phase voltage at the grid terminal, and $[i_a\ i_b\ i_c]^{\mathrm{T}}$ indicate the line currents flowing into the inverter.

$$\begin{bmatrix} v_{ia} \\ v_{ib} \\ v_{ic} \end{bmatrix} = \begin{bmatrix} v_{ga} \\ v_{gb} \\ v_{gc} \end{bmatrix} - \left(r_f + L_f \frac{d}{dt}\right) \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{3}$$

B. Synchronous Reference Frame Equivalent Circuit

Under balanced grid conditions with negligible harmonic content, it can be shown that the three-phase voltages and currents are dc quantities in the SRF [12]. Changing the variables form *abc* to the SRF is therefore highly desired. Further, in a three-wire three-phase system without a neutral wire for *zero*-sequence current to flow, the equations in the SRF reduce to just two *direct*-axis (*d*-axis) and *quadrature*-axis (*q*-axis) equations. The change of variables from the *abc* to the *dq*-axis in the SRF is obtained using the transformation matrix in (4), where θ is the instantaneous grid angle.

$$[K_{dq}^{\theta}] = \frac{2}{3}\begin{bmatrix} cos(\theta) & cos\left(\theta - \frac{2\pi}{3}\right) & cos\left(\theta + \frac{2\pi}{3}\right) \\ -sin(\theta) & -sin\left(\theta - \frac{2\pi}{3}\right) & -sin\left(\theta + \frac{2\pi}{3}\right) \end{bmatrix} \quad (4)$$

Transforming (3) to the SRF by pre-multiplying both sides by K_{dq}^{θ} and neglecting *zero*-sequence components yields (5), where ω_e is the grid frequency in *rads/sec* obtained from a phase-locked loop (PLL) and subscripts *d* and *q* indicate the *d*-axis and *q*-axis quantities respectively.

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \frac{1}{L_f}\left(\begin{bmatrix} v_{gd} - v_{id} \\ v_{gq} - v_{iq} \end{bmatrix} - r_f \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \omega_e L_f \begin{bmatrix} i_q \\ -i_d \end{bmatrix}\right) \quad (5)$$

The equivalent circuit of the AFEC in the SRF, corresponding to equation (5), is shown in Fig. 3. The last terms on the right-hand side of equation (5) indicate that the *d*- and *q*-axis components are coupled. To decouple the two current components a new variable maybe defined as:

$$v_d' = v_{gd} - v_{id} + \omega_e L_f i_q \quad (6)$$

$$v_q' = v_{gq} - v_{iq} - \omega_e L_f i_d \quad (7)$$

Substituting equations (6) and (7), in (5), rearranging and applying Laplace transform yields the plant transfer function for *d*-axis and *q*-axis current control in *s*-domain, and are given by equations (8) and (9) respectively. It is worth noting that the transfer functions for both *d*- and *q*-axis current control are identical.

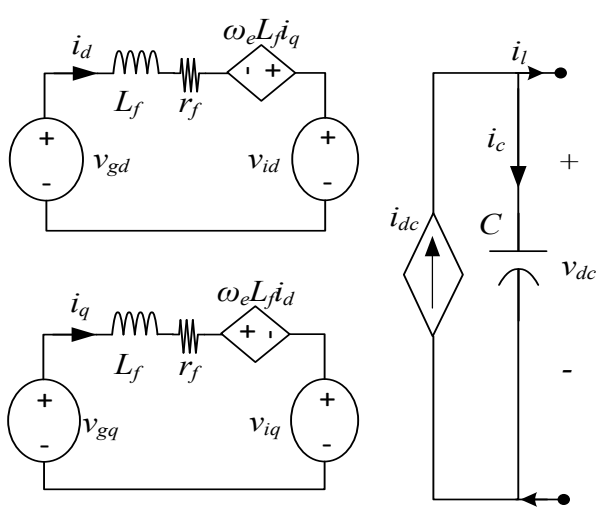

Fig. 3. Equivalent circuit diagram of the active front-end converter in the synchronous reference frame

In the SRF where the *d*-axis voltage v_{gd} is locked to the voltage space vector by a well-designed PLL, the *q*-axis grid voltage v_{gq} is equal to zero [12]. The dc and ac side circuits of the AFEC are thus related through the approximate instantaneous power balance equation as given by (10) [3]. Applying KCL on the dc side circuit, equation (11) is obtained where i_l is the dc load current, i_c the dc link capacitor current and i_{dc} the total dc current. Neglecting capacitor *ESR*, the plant transfer function for dc bus control is given by (12).

$$G_{id}(s) = \frac{i_d(s)}{v_d'(s)} = \frac{1}{r_f + L_f s} \quad (8)$$

$$G_{iq}(s) = \frac{i_q(s)}{v_q'(s)} = \frac{1}{r_f + L_f s} \quad (9)$$

$$i_{dc} = \frac{3}{2}\frac{v_{gd} i_d}{v_{dc}} \quad (10)$$

$$i_c = i_{dc} - i_l \quad (11)$$

$$G_{vp}(s) = \frac{v_{dc}(s)}{i_c(s)} = \frac{1}{Cs} \quad (12)$$

III. AC Current Controller Design

While the main purpose of this paper is the design of dc bus voltage compensator, inner current controller design is also discussed in this section for completeness. The overall block diagram for the control of the AFEC converter with ac current controllers and dc voltage controller is shown in Fig. 4.

The current plant transfer function along with the desired controller bandwidth ω_i are used to derive the gains for the PI controller. As previously noted, the plant transfer functions for both *d*- and *q*-axis currents are identical and of the first order. Therefore, the corresponding PI controllers will also have the same gains. Each PI current controller processes the current error ($i_{d_ref} - i_d$) and ($i_{q_ref} - i_q$) to produce v_d' and v_q' respectively. The PI outputs are subtracted from the feed-forward terms v_{gd} and v_{gq} and the cross-coupling terms $\omega_e L_f i_q$ and $-\omega_e L_f i_d$ are added to generate the reference voltage as seen in Fig. 4. The PI controller as defined by equation (1), and the plant transfer functions in (8) and (9), yields the closed loop command-to-output transfer functions given by (13) and (14). Choosing the proportional gain $K_{p_i} = \omega_i L_f$ and the integral gain $K_{i_i} = \omega_i r_f$ for both direct and quadrature current controller yields (15) and (16) respectively, where ω_i is the current control bandwidth in radians per seconds.

$$G_{cl_d}(s) = \frac{i_d(s)}{i_{d_ref}(s)} = \frac{PI(s)G_{id}(s)}{1 + PI(s)G_{id}(s)} \quad (13)$$

$$G_{cl_q}(s) = \frac{i_q(s)}{i_{q_ref}(s)} = \frac{PI(s)G_{iq}(s)}{1 + PI(s)G_{iq}(s)} \quad (14)$$

$$\frac{i_d(s)}{i_{d_ref}(s)} = \frac{1}{1 + s/\omega_i} \quad (15)$$

$$\frac{i_q(s)}{i_{q_ref}(s)} = \frac{1}{1 + s/\omega_i} \quad (16)$$

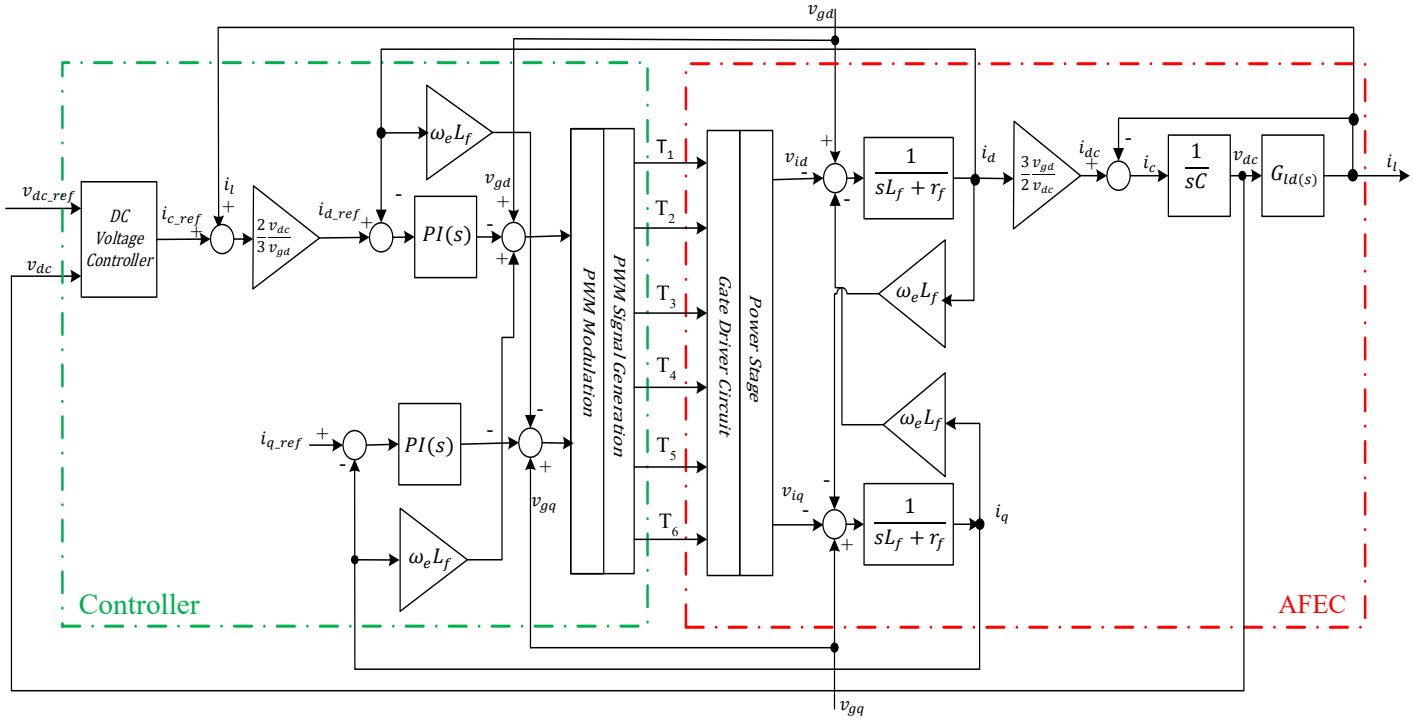

Fig. 4. Block diagram of the active front-end converter (AFEC) and the control architecture based on the dynamic model in the synchronous reference frame

The current controller bandwidth ω_i is chosen based on the dynamic response requirements of the system, but must also be high enough to mitigate the effects of parameter mismatch in the estimated and effective value of L_f and r_f [10]. An outer loop for dc bus voltage control is then built around the d-axis current controller to complete the control system. The q-axis current maybe regulated at 0 Amps for unity power factor application or at any arbitrary value based on dynamic reactive power requirements. The design of the dc voltage controller is detailed in the next section.

IV. DC Voltage Controller Design

The dc voltage compensator for AFEC applications is discussed in this section and the two types of PI controllers– 1DOF-PI and 2DOF-PI are considered and compared. The relationship between the ac current command and the output ac current in a well-designed AFEC control system in the SRF is a unity-gain low pass filter given by (15) and (16). The dc voltage in an AFEC is controlled using the d-axis current component. A compensator is synthesized that processes the dc voltage error $(v_{dc_ref} - v_{dc})$ and produces capacitor current reference i_{c_ref} to which the dc load current i_l is added as the feed-forward term. The equated dc current is scaled to calculate the required d-axis reference current i_{d_ref} for the d-axis current controller discussed in the previous section. The dc voltage control scheme is shown in detail in Fig. 4, where the generic dc voltage controller shown maybe replaced with a 1DOF-PI or a 2DOF-PI. As seen the dc bus controller forms the outer loop while the current controller forms the inner loop of the control scheme. As such, the control bandwidth of the outer loop (ω_n) is chosen well-below the current control bandwidth ω_i such that $\omega_n \ll \omega_i$ [13]. As the outer loop has a much slower response than the inner current control, the closed loop current dynamics is approximated by a simplified unity gain system and is thus neglected for dc controller design considerations [7]. Hence the dc voltage plant transfer function given by (12) is valid for a simplified system. In this section the 1DOF-PI and the 2DOF-PI is discussed, closed-loop transfer functions derived and compared.

A. 1DOF-PI Controller for DC Voltage Control

Fig. 5(a) shows the simplified control block diagram for the regulation of dc voltage using a 1DOF-PI. The closed loop command-to-output transfer function $G_{v1_cl}(s)$ for the shown system is given by (17). This is a second order transfer function with natural frequency ω_n, damping ratios ζ and a LHP zero ω_z, given by (18), (19) and (20) respectively. If the relationship $\omega_n \ll \omega_i$ is maintained, the poles of the system in (17) can be placed arbitrarily by choosing the parameters K_p and K_i

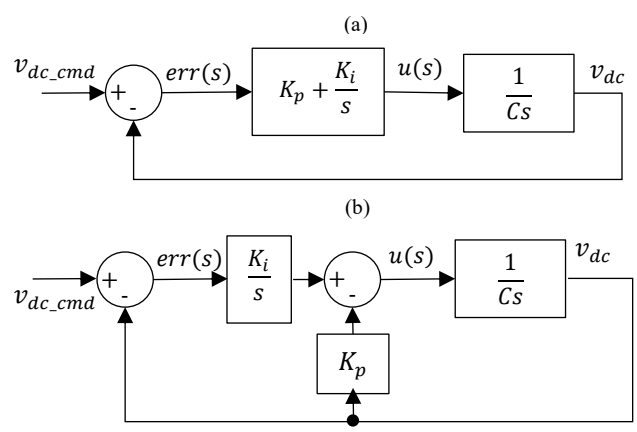

Fig. 5. Simplified dc bus control block diagram using (a) 1DOF-PI controller, and (b) 2DOF-PI controller

accordingly. However, the LHP zero of the system at ω_z, given by (20), cannot be arbitrarily placed as it is dependent on K_p and K_i as well. This is the limitation of the 1DOF-PI when applied for voltage regulation as only two of the parameters that govern the dynamic system response can be selected but not all three.

$$G_{v1_cl}(s) = \frac{v_{dc_ref}(s)}{v_{dc}(s)} = \frac{\frac{K_p}{C}s+\frac{K_i}{C}}{s^2+\frac{K_p}{C}s+\frac{K_i}{C}} \tag{17}$$

$$natural\ frequency, \omega_n = \sqrt{\frac{K_i}{C}} \tag{18}$$

$$damping\ ratio, \zeta = \frac{K_p}{2\sqrt{K_i C}} \tag{19}$$

$$LHP\ zero, \omega_z = \frac{K_i}{K_p} \tag{20}$$

B. 2DOF-PI Controller for DC Voltage Control

A 2DOF-PI type controller of the form given in Fig. 5(b) eliminates the LHP zero from the command-to-output transfer function for the dc-bus voltage control loop. Using equation (12) as the plant transfer function in 2DOF-PI structure of Fig 2 (b), the command-to-output transfer function $G_{v2_cl}(s)$ is obtained as:

$$G_{v2_cl}(s) = \frac{v_{dc_ref}(s)}{v_{dc}(s)} = \frac{\frac{K_i}{C}}{s^2+\frac{K_p}{C}s+\frac{K_i}{C}} \tag{21}$$

The transfer function in (21) has the form of a normalized general second order transfer function [2]. Notably, the LHP zero is no longer present which is highly desired. Elimination of LHP zero implies that the system response for the closed loop is governed only by the natural frequency and the damping ratio. Further comparing equation (21) to equation (17) shows that the characteristic equations of the command-to-output transfer functions with 1DOF-PI and 2DOF-PI are identical, therefore equations (18) and (19) apply to both. This shows that when a 2DOF-PI is used the full system dynamics can be arbitrarily optimized by calculating the controller gains, K_p and K_i, using equations (18) and (19). For a properly designed system the condition $\omega_n \ll \omega_i$ must be satisfied as well.

Control systems characterized by a general second-order transfer function with no zeroes will not have overshoots in the response when the damping ratio is smaller than 1 ($\zeta < 1$) [2]. Over-damped or critically damped responses are usually preferred in control system design due to the absence of overshoots or ringing during step responses.

V. Simulation Results

To demonstrate the effectiveness of the proposed 2DOF-PI and to compare its performance against the conventional 1DOF-PI, a switching model of an AFEC was constructed in MATLAB/Simulink. The electrical circuit of the simulated AFEC was identical to the circuit diagram shown in Fig. 2 and the controller structure was identical to Fig. 4. The parameters selected for the simulation of the converter are listed in Table I. Simulations were performed with both types of controllers for dc voltage regulation; however, the inner current control loops were identical for both cases. Finally, the results obtained with 1DOF-PI and 2DOF-PI were compared.

TABLE I. Parameters for Simulation

Fundamental frequency, ω_e	60 Hz
PWM carrier frequency, F_{sw}	5 kHz
Nominal line-to-line voltage, $V_{ll,rms}$	480 V
Filter inductance, L_f	500 µH
Filter resistance, r_f	75 mΩ
DC capacitance, C	3200 µF

For the inner current PI regulator, the proportional gain K_{p_i} and integral gain K_{i_i} were selected as 0.94 and 141.37 respectively for a closed loop current control bandwidth (ω_i) of 300 Hz. For the outer voltage control loop the natural frequency (ω_n) of 30 Hz and the damping ratio (ζ) of 1 were selected. Using equations (18) and (19) the corresponding values for proportional (K_p) and integral (K_i) gains were calculated as 1.32 and 124.36 respectively. The same gain values were used in both 1DOF-PI and 2DOF-PI for regulation of the dc voltage due to reasons discussed earlier.

Fig. 6(a) shows the response of the switching model of AFEC with 1DOF-PI to a step change in dc voltage reference from 750 V to 1000 V at 0.3 secs. Fig. 6(b) shows the step response for the same AFEC with the 2DOF-PI controller. Further comparing the two figures, a 9% voltage overshoot due to the LHP zero in the 1DOF-PI type controller can be seen in Fig. 6(a) whereas there is no overshoot observed in Fig. 6(b),

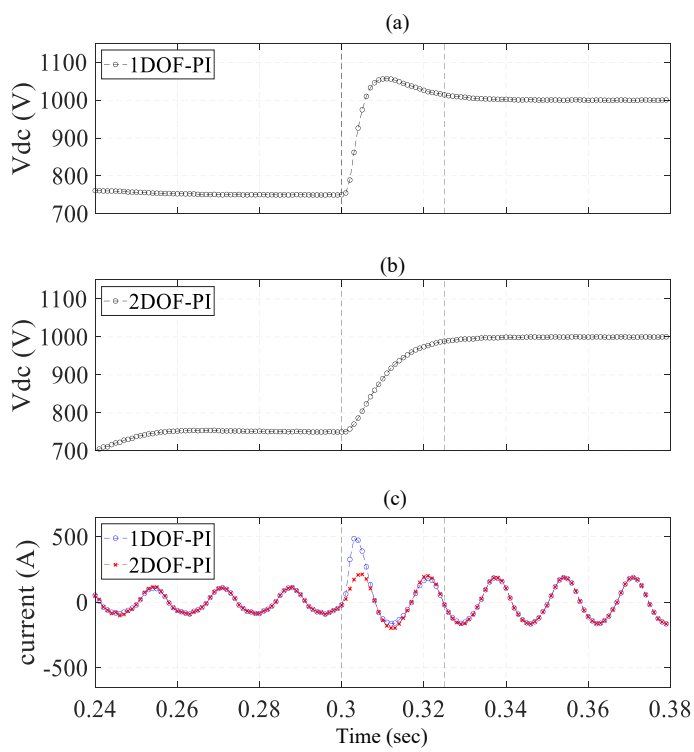

Fig. 6. Step response of AFEC for change of reference voltage from 750 V to 100V at 0.3 secs. (a) observed dc bus voltage with 1DOF-PI controller, (b) observed dc bus voltage with 2DOF-PI controller, and (c) observed ac currents during step response

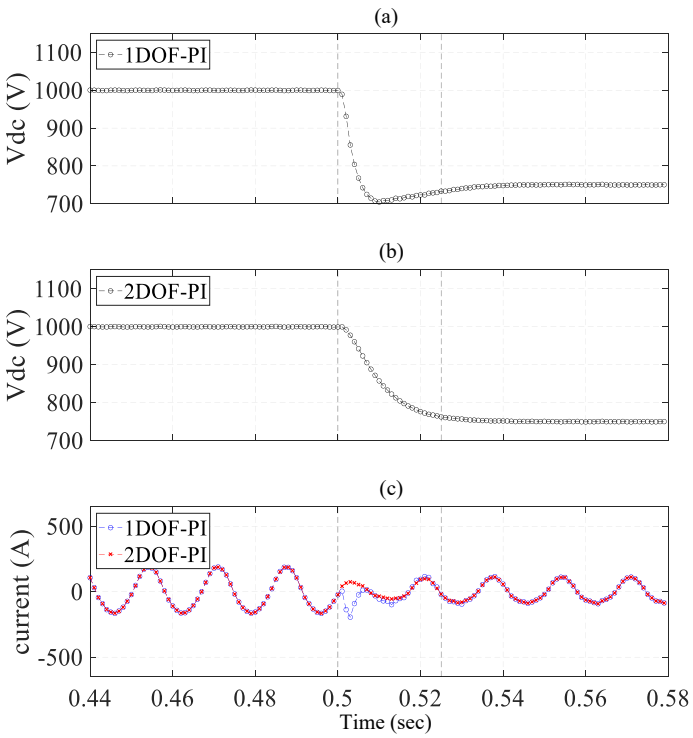

Fig. 7. Step response of AFEC for change of reference voltage from 1000 V to 750 V at 0.5 secs. (a) observed dc bus voltage with 1DOF-PI controller, (b) observed dc bus voltage with 2DOF-PI controller, and (c) observed ac currents during step response

which is expected due to the absence of the LHP zero. It is also worth noting that the responses in Fig. 6(a) and Fig. 6(b) both have setting times equal to 0.026 seconds which corresponds well with the desired outer loop bandwidth of 30 Hz. The observed ac current during the step responses are also plotted in Fig. 6(c) where the current due to the 1DOF-PI shows a 200% overshoot whereas that due to 2DOF-PI does not display any overshoot characteristic. Similarly, the responses of the AFEC for a step change in reference voltage from 1000 V to 750 V is shown in Fig. 7 where the change in reference voltage is applied at 0.5 secs. The observed voltage undershoots seen in Fig. 7(a) is expected and is due to the LHP zero seen in equation (16).

VI. Conclusion

A two degree-of-freedom type PI controller for the regulation of the dc bus voltage of an AFEC was proposed in this paper. A model of the AFEC in the SRF was presented and the current and voltage controller were designed based on the SRF model. The performance of the proposed 2DOF-PI was compared against that of the conventional 1DOF-PI using MATLAB/Simulink. The simulation results show the effect of the LHP zero with the 1DOF-PI and that of its absence with the 2DOF-PI. Further the observed settling time of the step responses validate that the controller gain selection criteria given by equations (17) and (18). This further validates the derived AFEC model in the SRF. The over- and undershoot in the voltage step response was observed in the AFEC with 1DOF-PI and not on that with 2DOF-PI. Further the ac currents in the former showed a much higher current overshoot while the latter did not show overshoots. A two degree-of-freedom type controller can be used to design the dc voltage controller in an AFEC for improved performance for step change in dc bus voltage reference input.

Acknowledgment

This project was supported by Office of Electricity's (OE) Transformer Resilience and Advanced Components (TRAC) program and Buildings Technologies Office under the Department of Energy's (DOE) Grid Modernization Laboratory Consortium (GMLC).

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