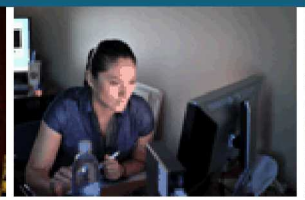
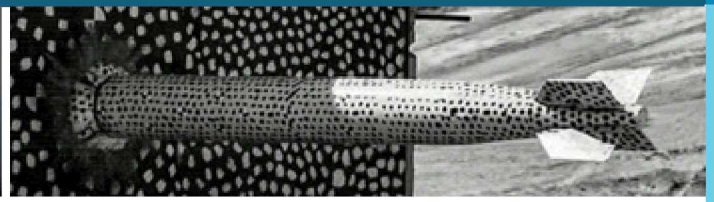
SAND2020-2046PE

SCHOOL OF ENGINEERING

Modeling and Simulation Approaches to Single-Event Effects in Microelectronics





PRESENTED BY

Jeffrey D. Black

Sandia National Laboratories

LABORATORY DIRECTED RESEARCH & DEVELOPMENT

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Outline

Overview of Single Event Effects in Microelectronics

Modeling and Simulation Approach

Case Study #1 – Layout Variations in Sandia National Labs' 0.35 μm SOI (CMOS7) D Flip-Flops

- CMOS7 Process and Transistor Types
- DFF Design and Layout Variations
- TCAD Modeling
- Single Event Upset Test Results
- MRED Modeling
- HBD Implications

Case Study #2 – Multiple Node Charge Collection Mitigation in Global Foundries 32nm SOI Process

- Review of Single Node Charge Collection Hardened Design Options
- Multiple Node Charge Collection Mitigation Designs/Layouts
- Ground-Based Testing Challenges
- Modeling Results

Summary

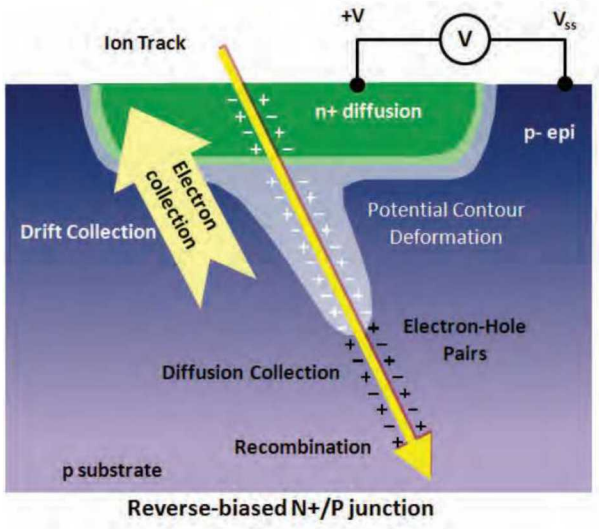
Single Event Effects Mechanisms

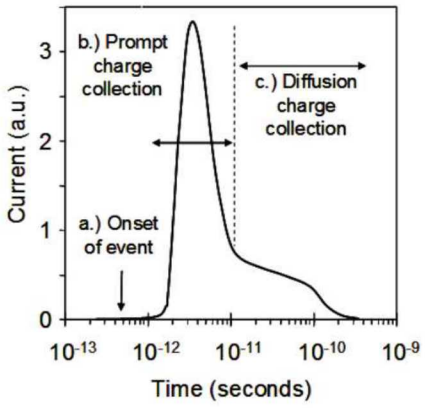
Direct Ionization

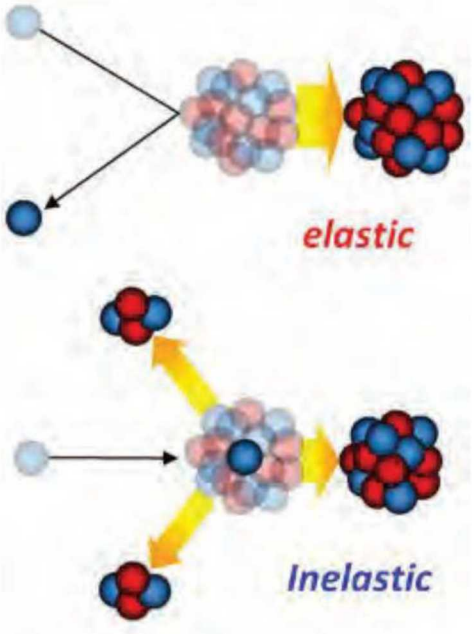
- Charged radiative particle passes through semiconductor, creating a track of electron/hole pairs
  - Amount of electron/hole pairs varies with charged particle type and energy
- Added electrons and holes are governed by drift (move with electric fields) and diffusion (spread away from high densities)
- Electrons and holes will be swept across a P-N junction and appear as current or recombine

Indirect Ionization

- Charged or neutral radiative particle passes through semiconductor materials and interacts with existing atoms, nuclear collision
- Resulting charged particles then directly ionize and create electron/hole pairs







Single Event Effects Description

Basic Effects

- Single Event Transient (SET) – Voltage pulse emanating from P-N junction collecting charge
- Single Event Upset (SEU) – Change in microelectronic memory state due to single event
- Single Event Latchup (SEL) – Parasitic P-N-P-N structure turned into high current draw

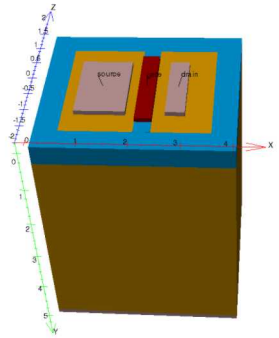
Complex Effects

- Single Event Functional Interrupt (SEFI) – Temporary change in some portion of an integrated circuit where the function of the circuit is altered, e.g. change to the state of a state machine
- Multiple Cell Upset (MCU) – The change of multiple memory cell states due to a single radiative particle, particle might pass through several cells or particle might deposit a lot of charge that diffuses to several cells
- Multiple Bit Upset (MBU) – Similar to MCU except that the bits are in the same digital word, used in discussion of error detection and correction

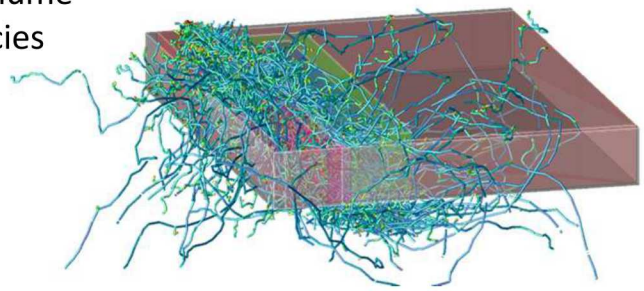
There are many more terms/effects, destructive and non-destructive

Single Event Modeling and Simulation Approach

Simulation tool flow

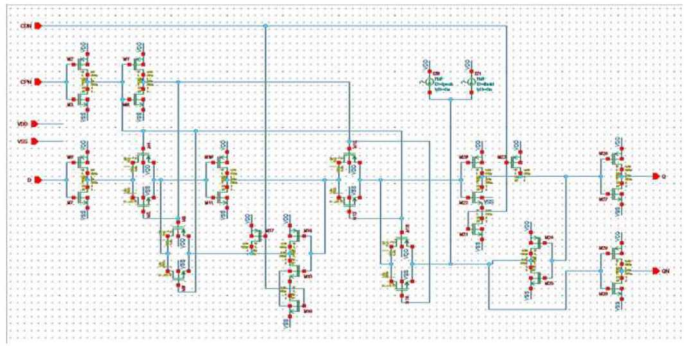


Nested sensitive volume sizes and efficiencies



Collected charge

Critical charge



3D TCAD Simulation

MRED Simulation/Custom Scripts

Circuit Simulation

- SEE implemented as a track of charge
- Drift and diffusion charge transport –> determine sensitive volume sizes, locations, and efficiencies

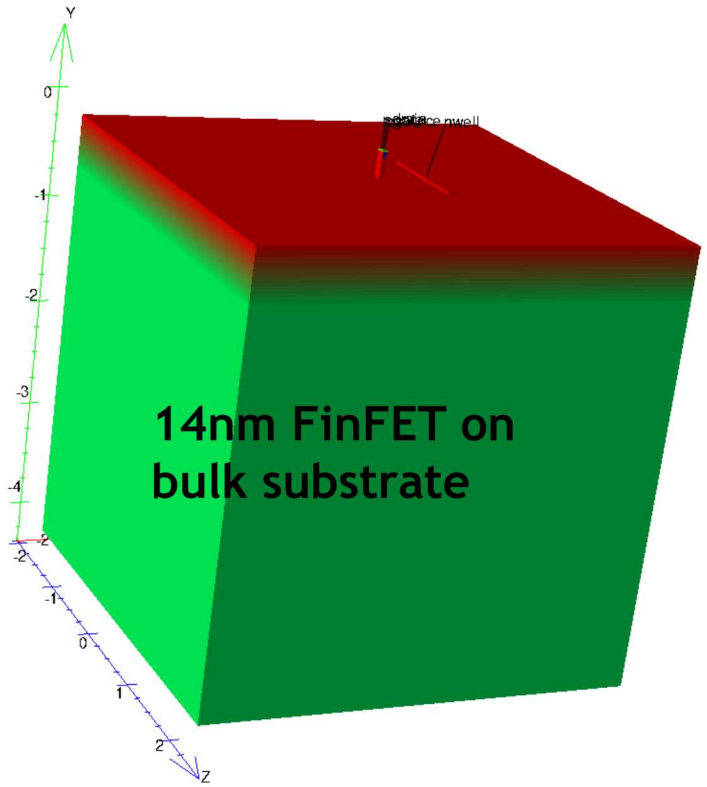
- SEE implemented as radiation particles
- Accurately simulates radiative energy deposition in collection volumes derived from TCAD

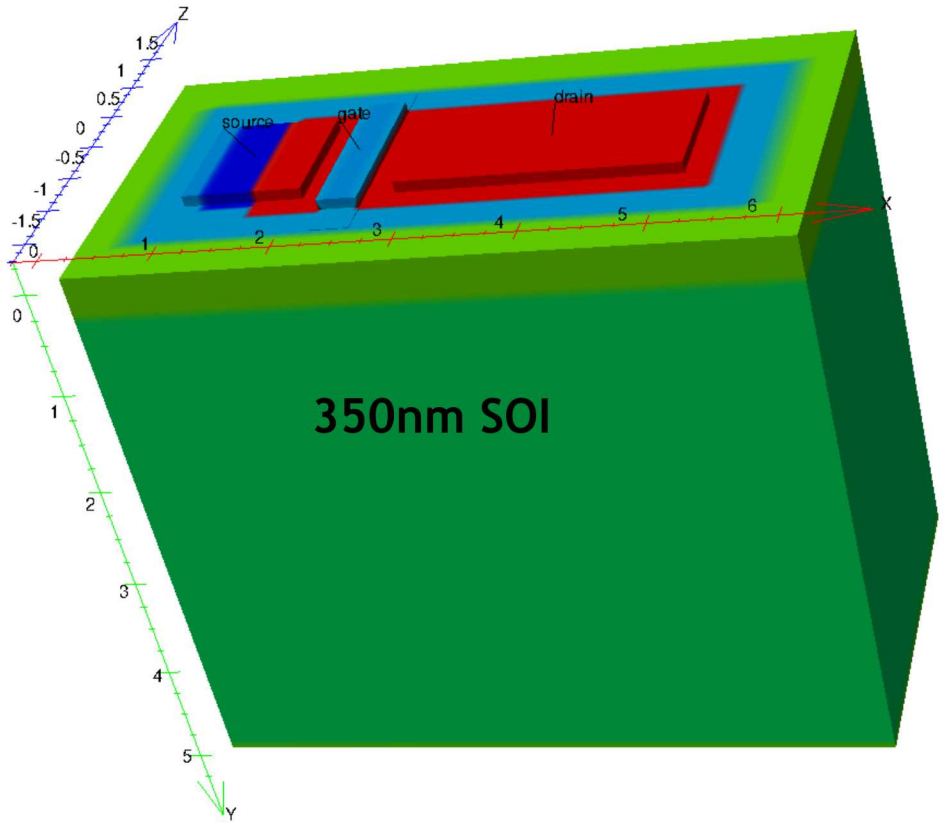
- SEE implemented as current sources
- Simulates circuit effect based upon charge collection determined in MRED scripting

Definitions:

- TCAD – Technology Computer Aided Design
- MRED – Monte Carlo Radiative Energy Deposition

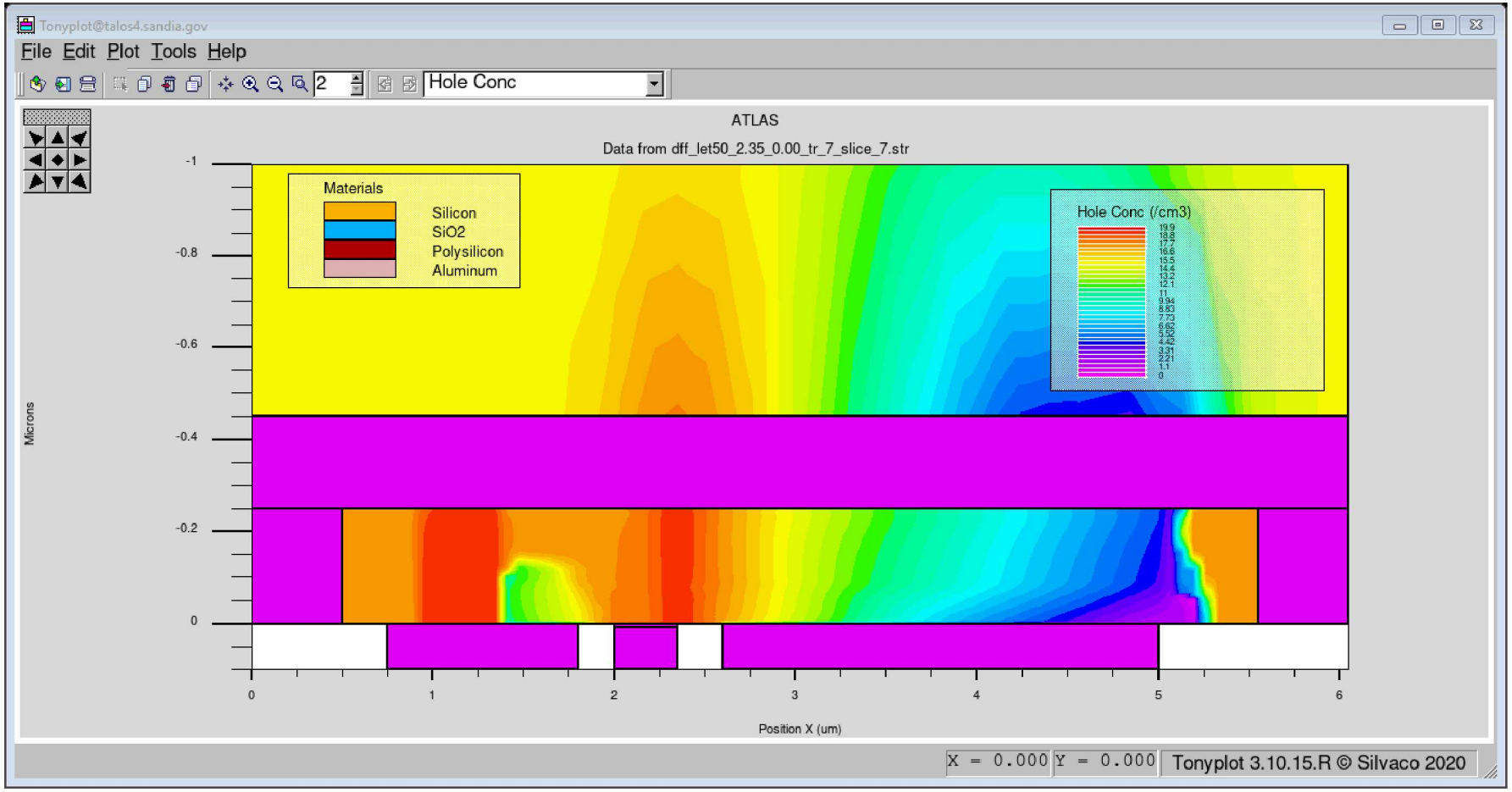
3D TCAD Example Structures



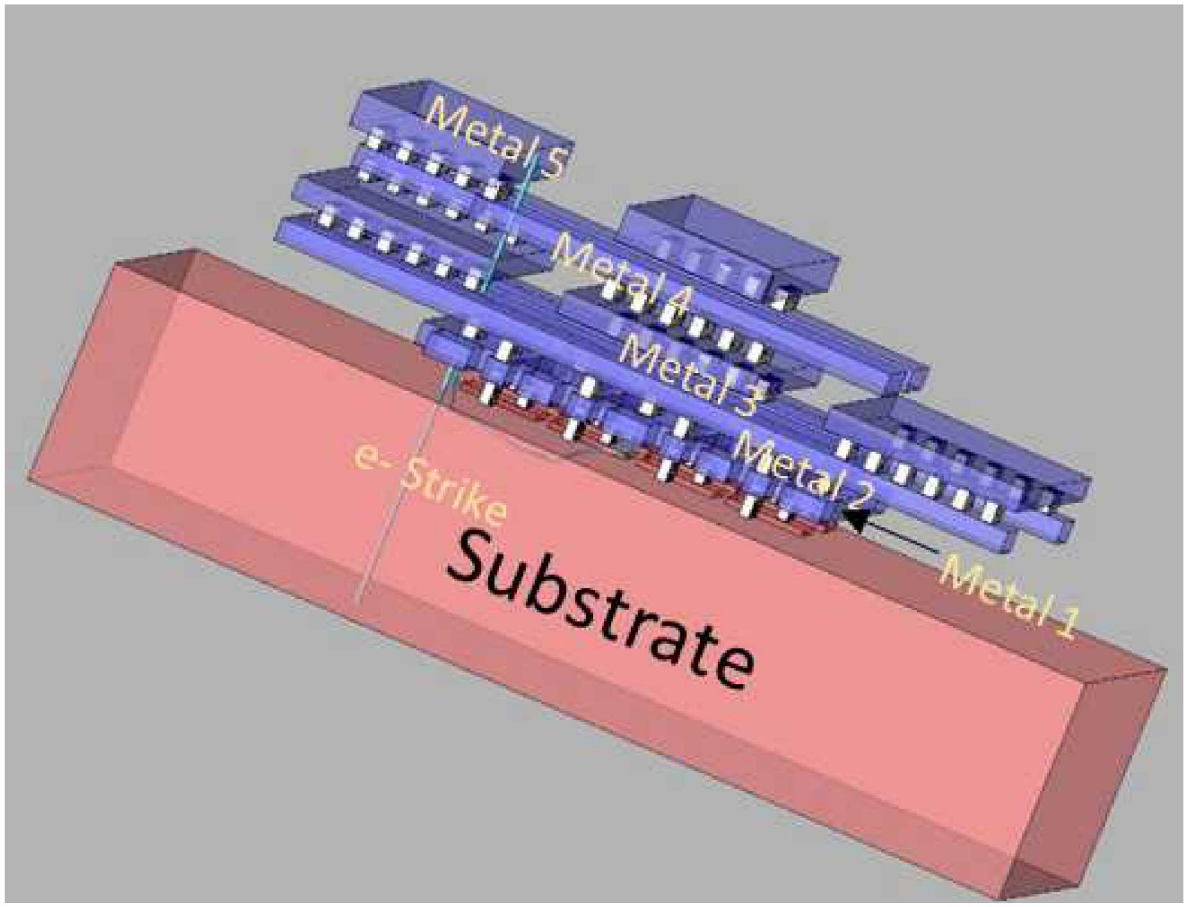


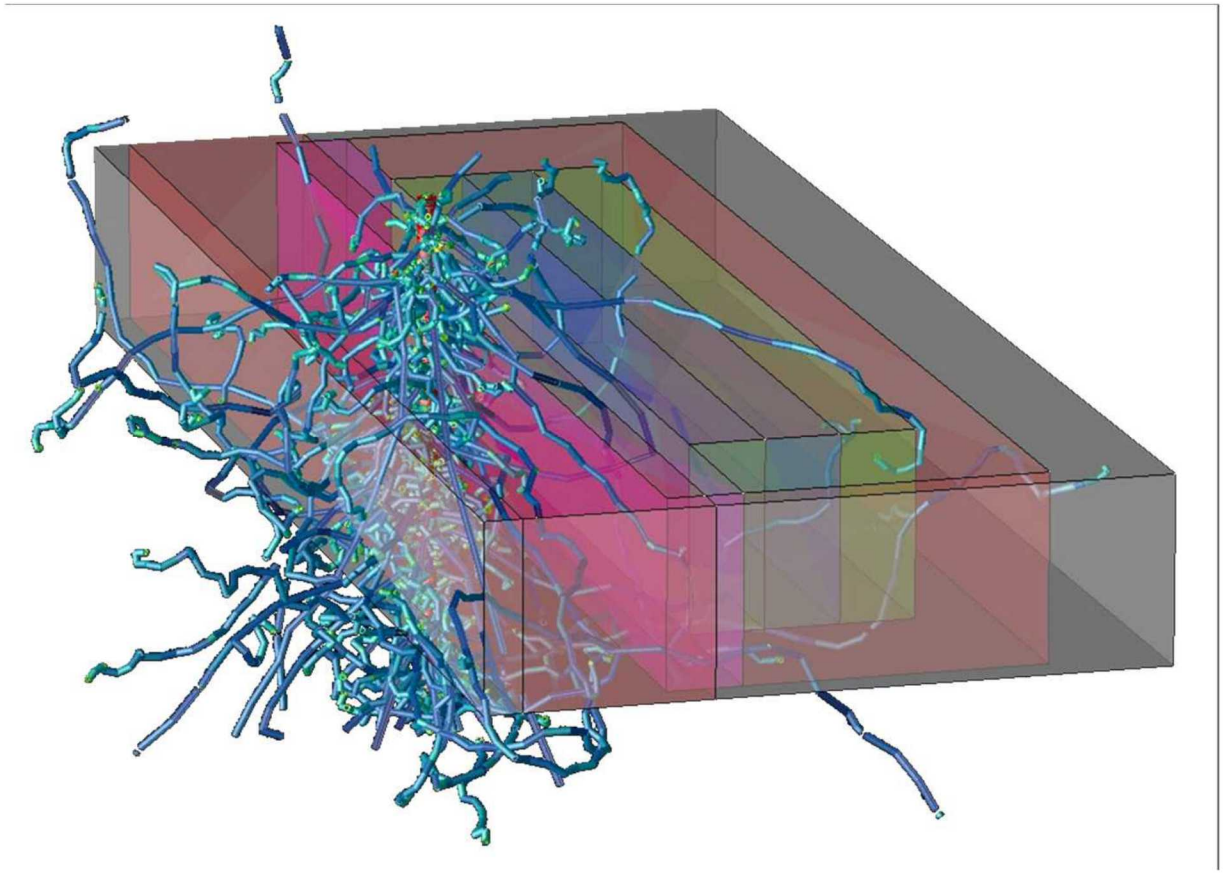
Note that these 3D structures are approximately the same size, even though the technology of the FinFET is ~1/20th of the SOI device – In bulk technologies we have to allow for movement of carriers away from the original single event so that it doesn't reflect back into the device

3D TCAD Single Event Simulation



3D MRED Examples





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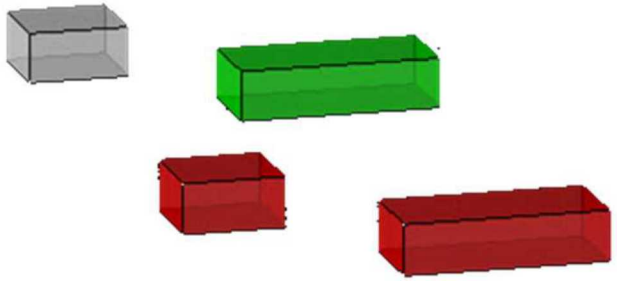

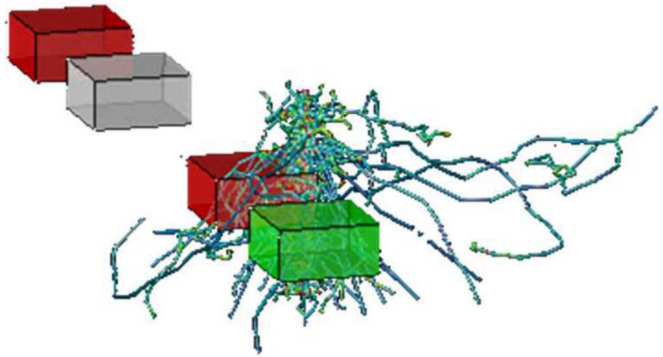

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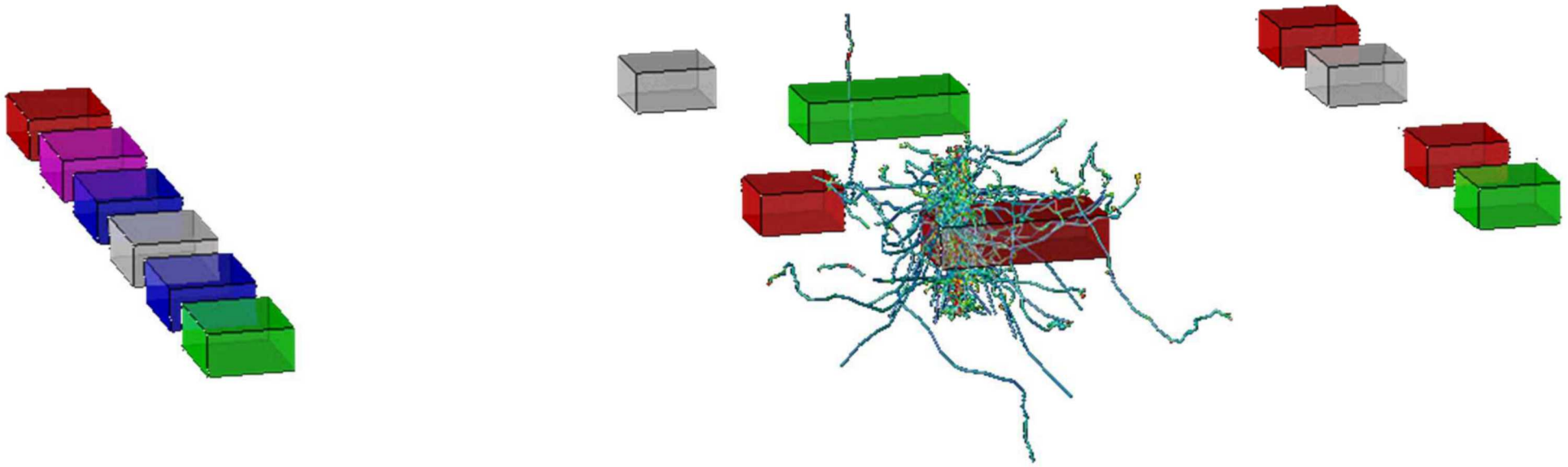

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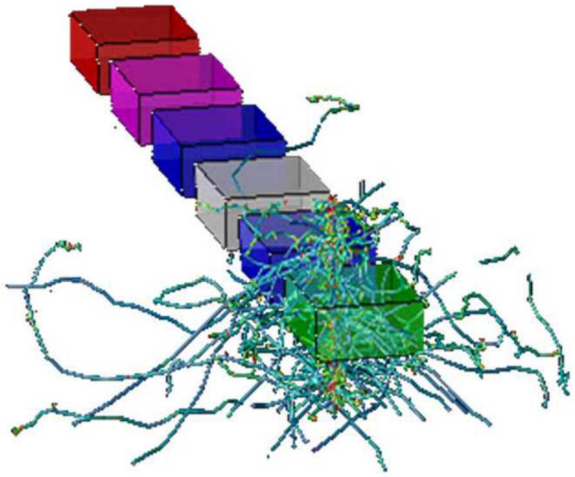

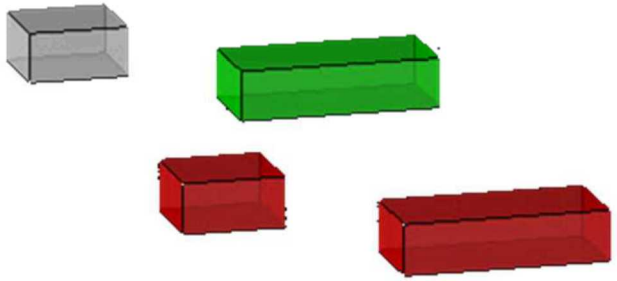

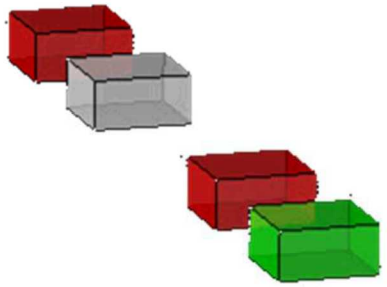

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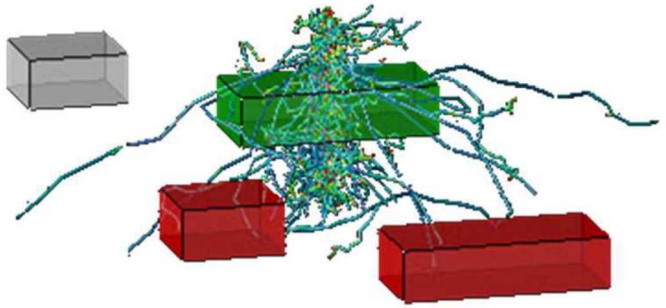

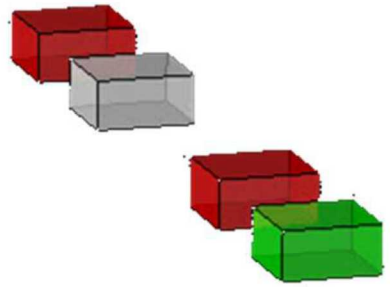

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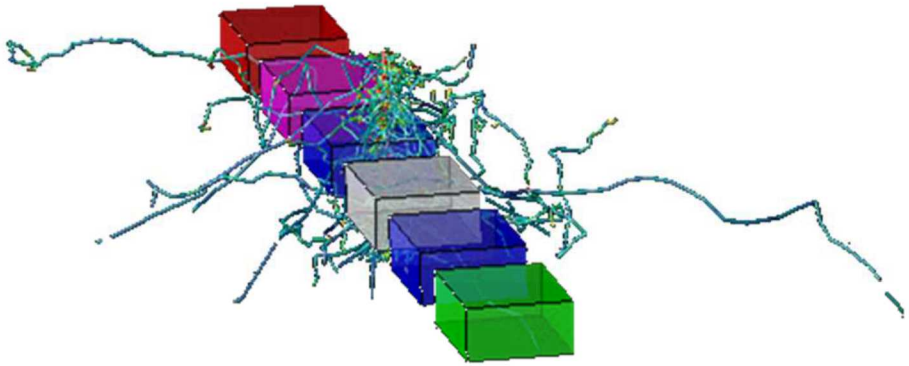

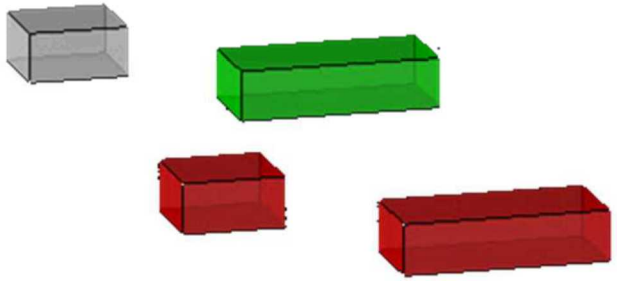

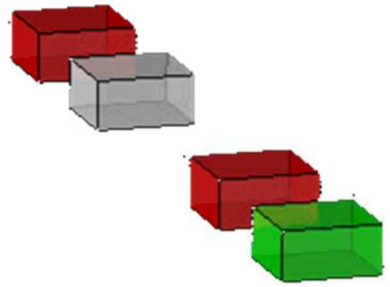

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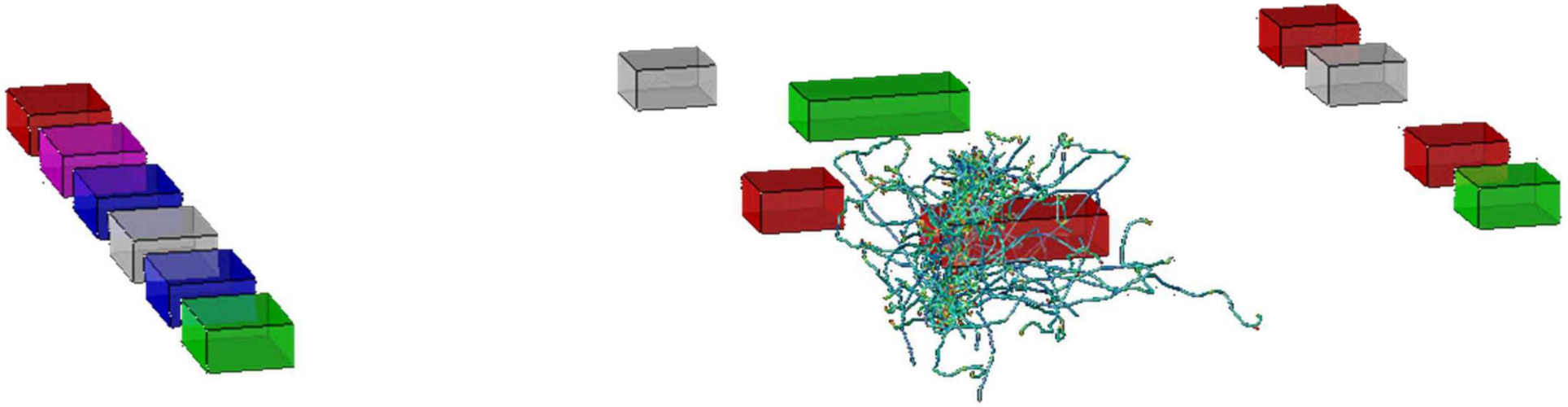

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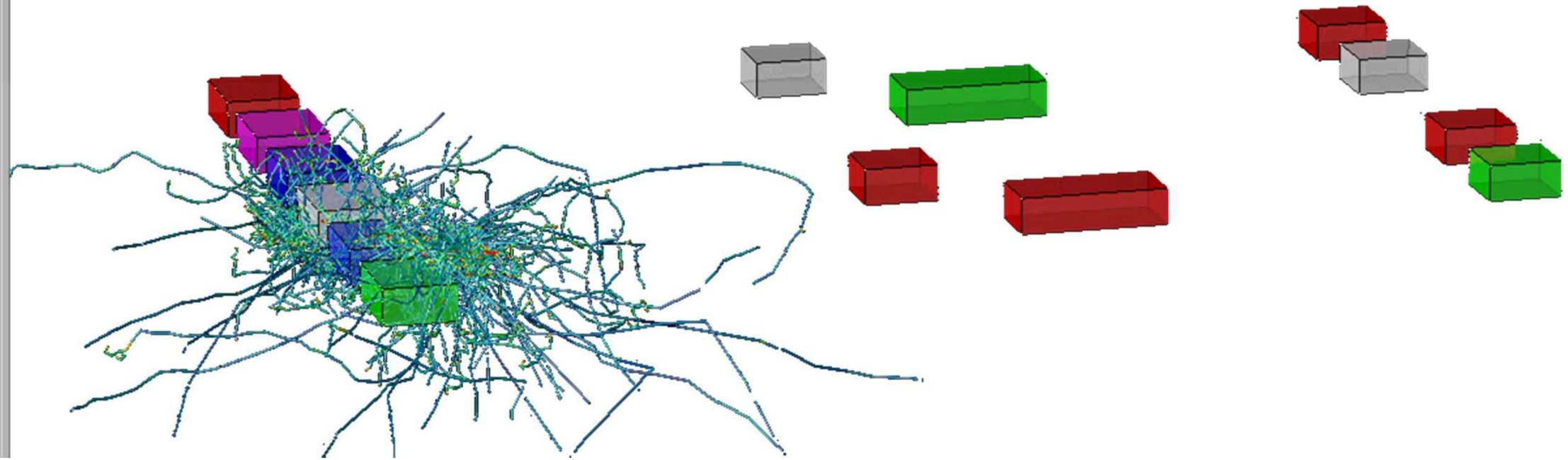

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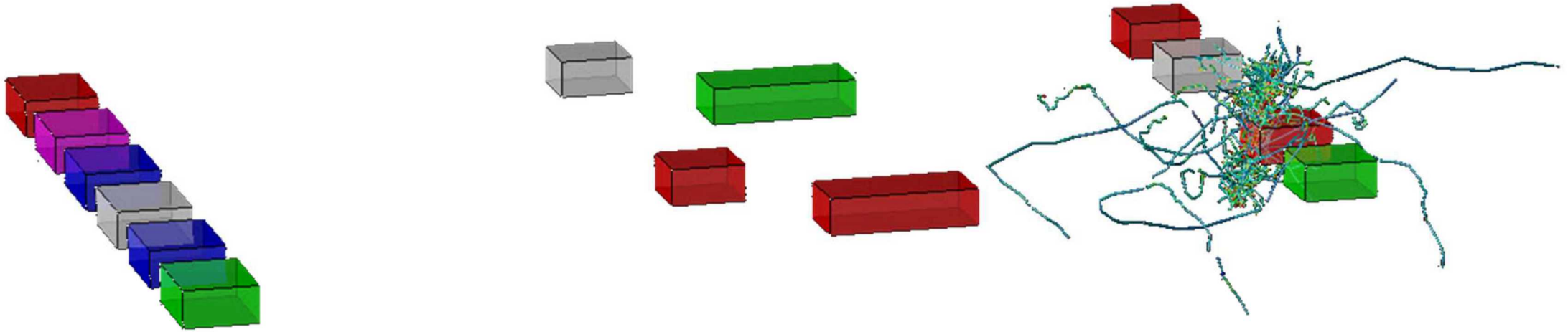

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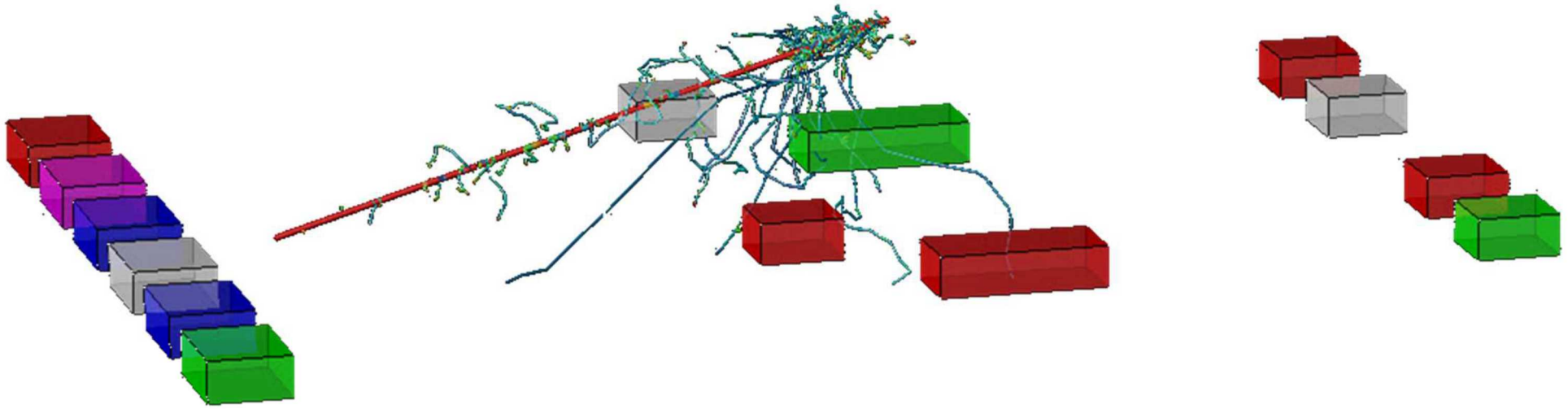

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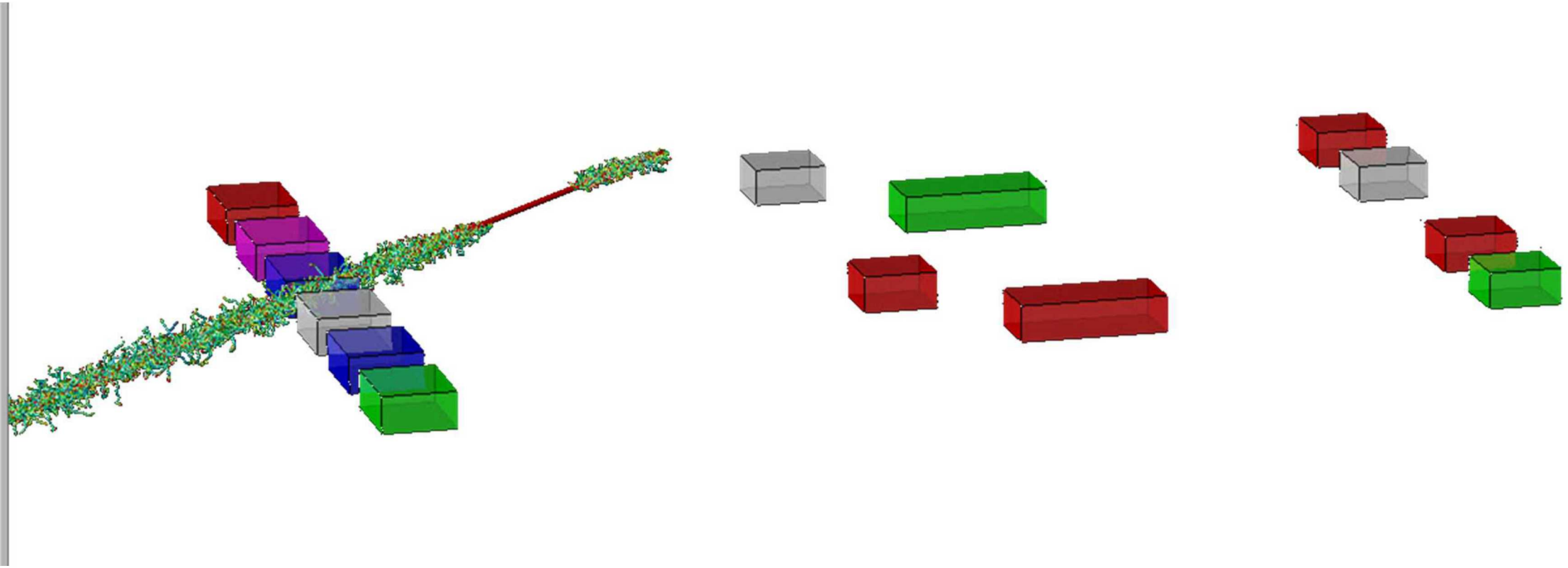

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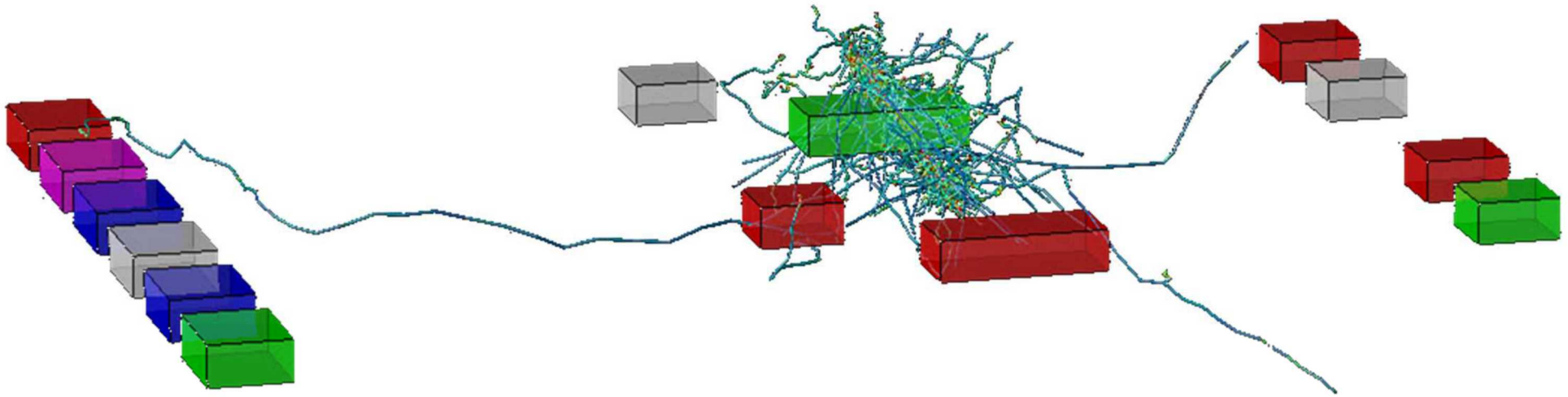
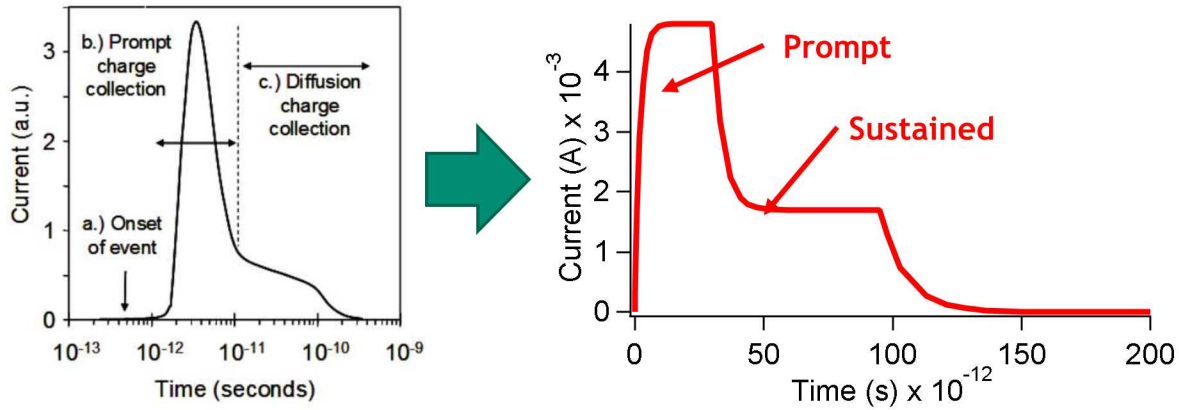
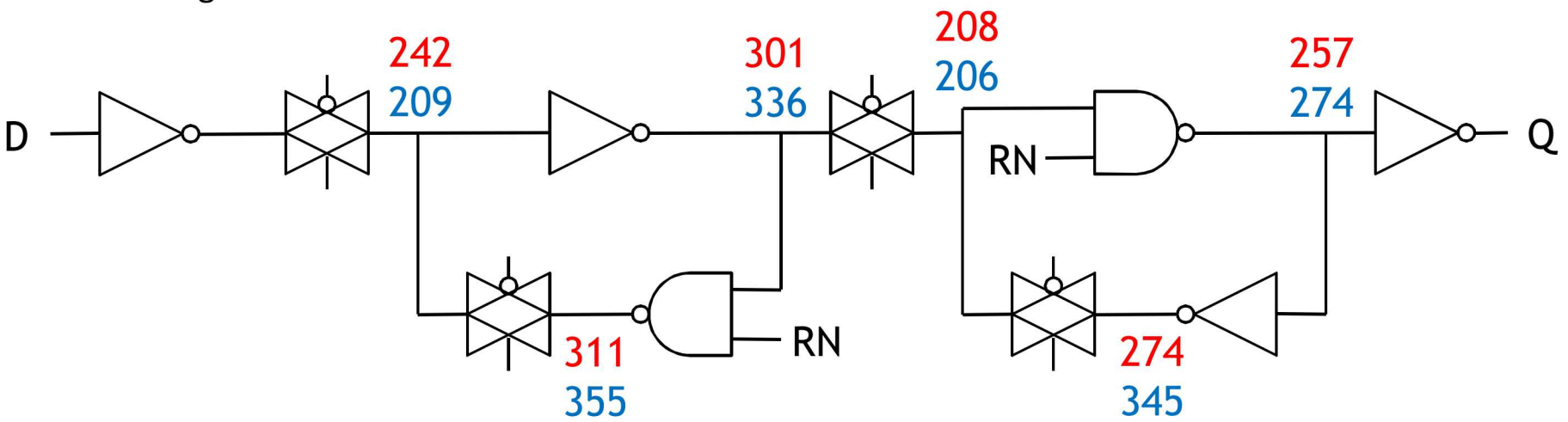


Circuit Single Event Simulation

Dual double-exponential current sources

- Prompt
  - Node voltage switches from 1->0 or 0->1
  - Overcomes node capacitance and restoring current
- Sustained
  - Node voltage remains switched
  - Overcomes restoring current





PHIT Critical Charge (fC)

NHIT Critical Charge (fC)

Case Study #1 – Layout Variations in Sandia National Labs' 0.35 μm SOI (CMOS7) D Flip-Flops

CMOS7 Process and Transistor Types

DFF Design and Layout Variations

TCAD Modeling

Single Event Upset Test Results

MRED Modeling

HBD Implications

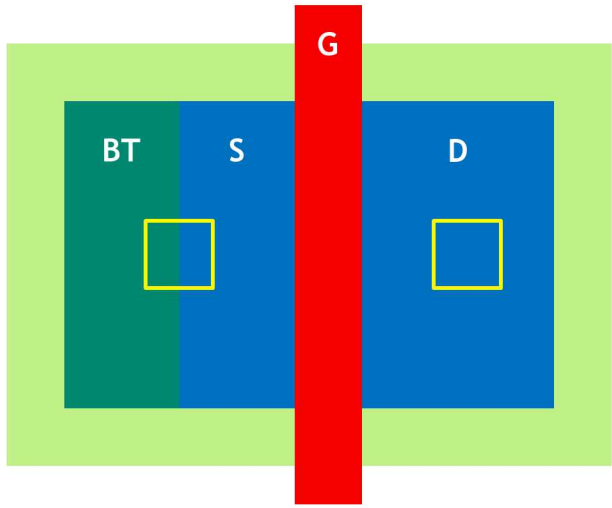
Background - CMOS7 Process and Transistor Types

CMOS7

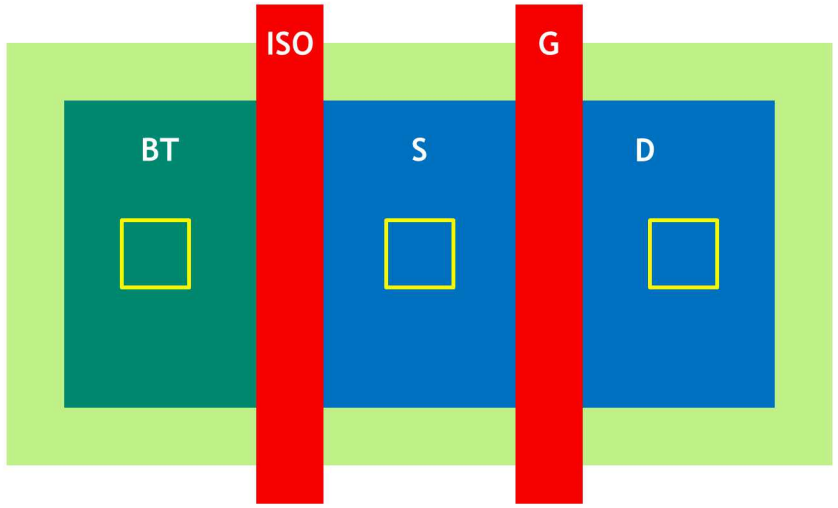
- 0.35 μm
- SOI
  - 250 nm Si
  - 200 nm buried oxide
- 5 metal layers

Transistor Types

- NMOSFET
  - Body-Under-Source FET (BUSFET)
  - Isolation FET (IFET)
  - N+ implant can be fully bottomed (deep) or not fully bottomed (shallow)
- PMOSFET
  - Body-Tied-to-Source FET (BTSFET)
  - IFET
  - P+ implant is only fully bottomed (deep)
- For this experiment, the source/drain implants do not extend to the sidewall oxides (body tie goes around the implants)



BUSFET/BTSFET – Body Tie (BT) and Source (S) Abutted



IFET – Source (S) and Drain (D) can be Switched

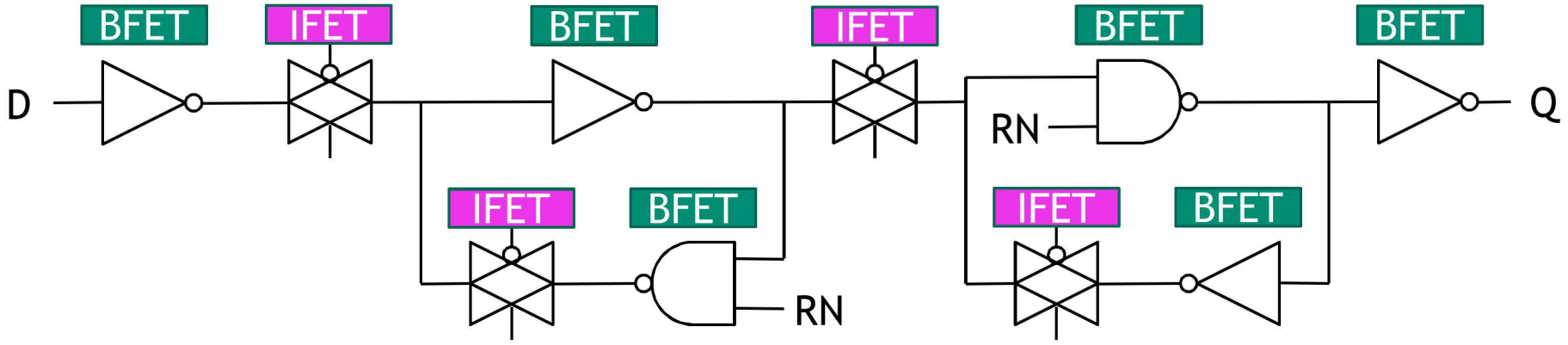
DFF Design

Schematic shows master and slave stage of DFF with all loading

- PMOSFET W/L = 3.2μm/0.45μm, NMOSFET W/L = 1.6μm/0.35μm
- Clock distribution not shown, no significant clock dependent SEUs in this technology
- BUSFET and BTSFET layouts indicated by BFET
- IFET indicated by IFET

Simulated and tested in clocking alternating data

- Master/slave probability of upset (0.5)
- High/low probability of upset (0.5)
- Each transistor simulated with a probability of upset of 0.25

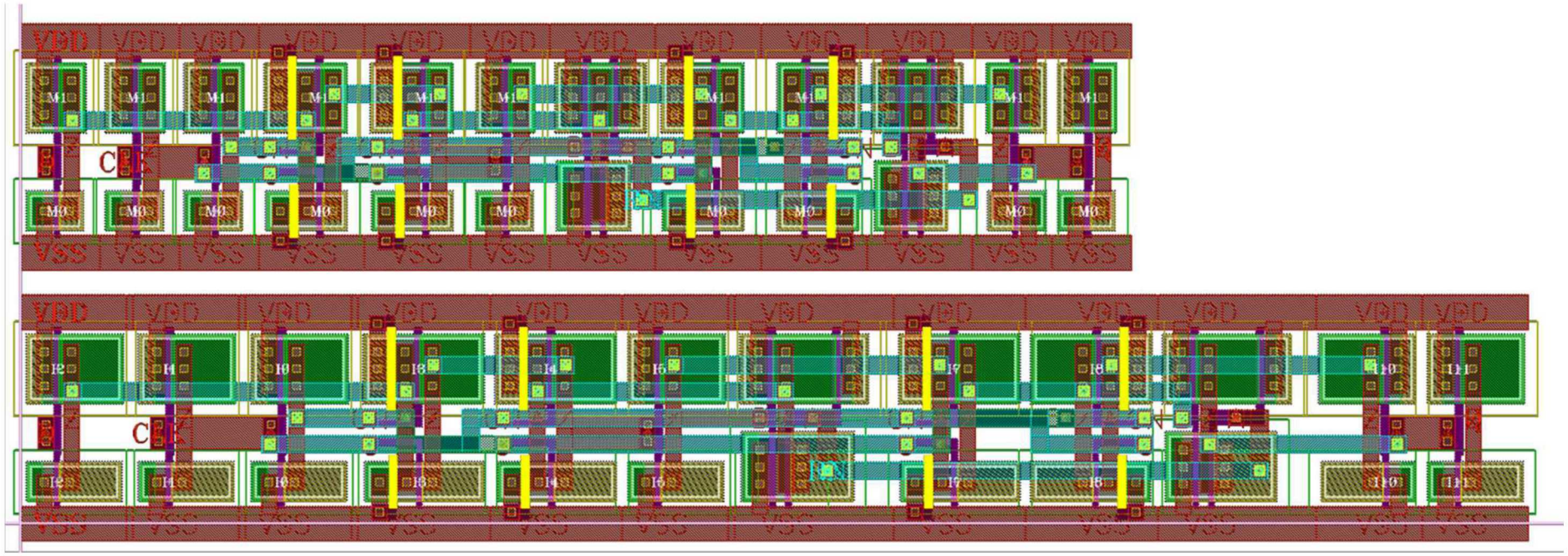


DFF Layout Variations

2 Layout Topologies
- Standard
- Extended Drain

2 NMOSFET Variations
- Standard (all NMOSFET drains deep)
- Shallow (all NMOSFET implants shallow)

Experiment	Layout Topology	NMOSFET Variation
Baseline	Standard	Standard
Shallow	Standard	Shallow
Extended Drain	Extended Drain	Standard
Extended Shallow	Extended Drain	Shallow



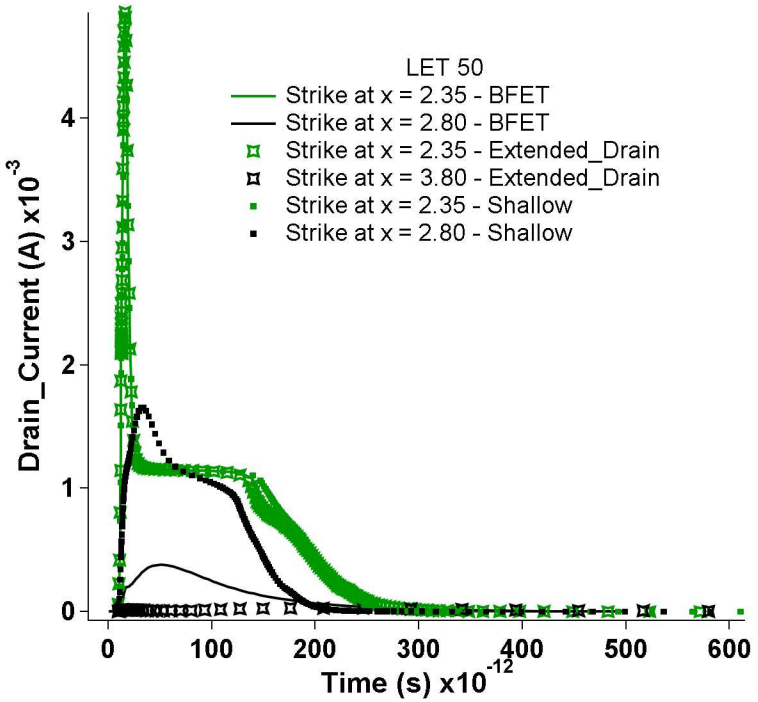
TCAD Modeling - Inverter

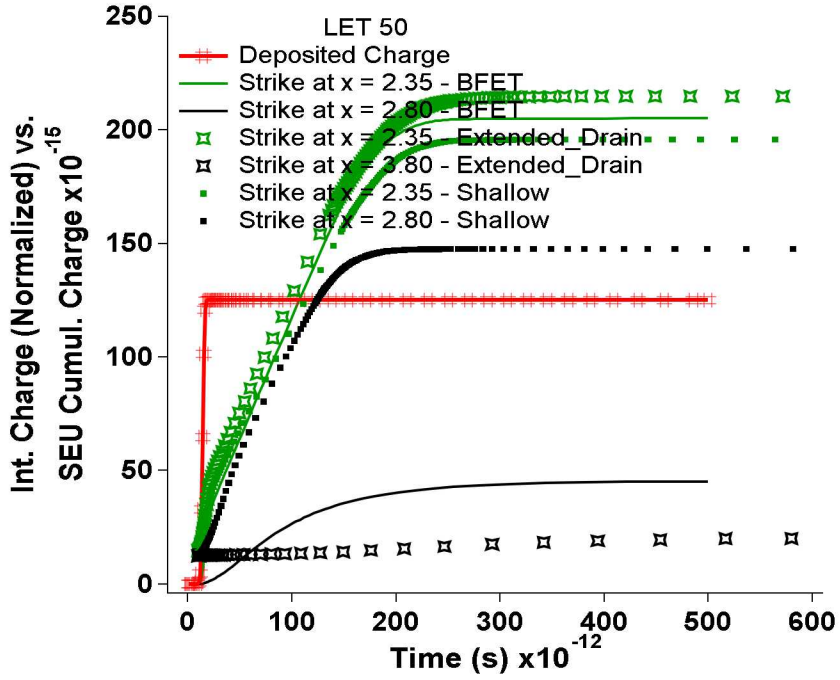
Silvaco Altas 3D mixed-mode

Inverter configuration, 3D device OFF

Results Summary

- BFET with deep drain has highest charge collection under gate near drain – deep drain doesn't collect charge efficiently
- Shallow BUSFET collects charge efficiently under gate and in drain, but bipolar gain is much less inside the drain
- Extending the drain doesn't affect deep drains, increases cross-section for shallow drains



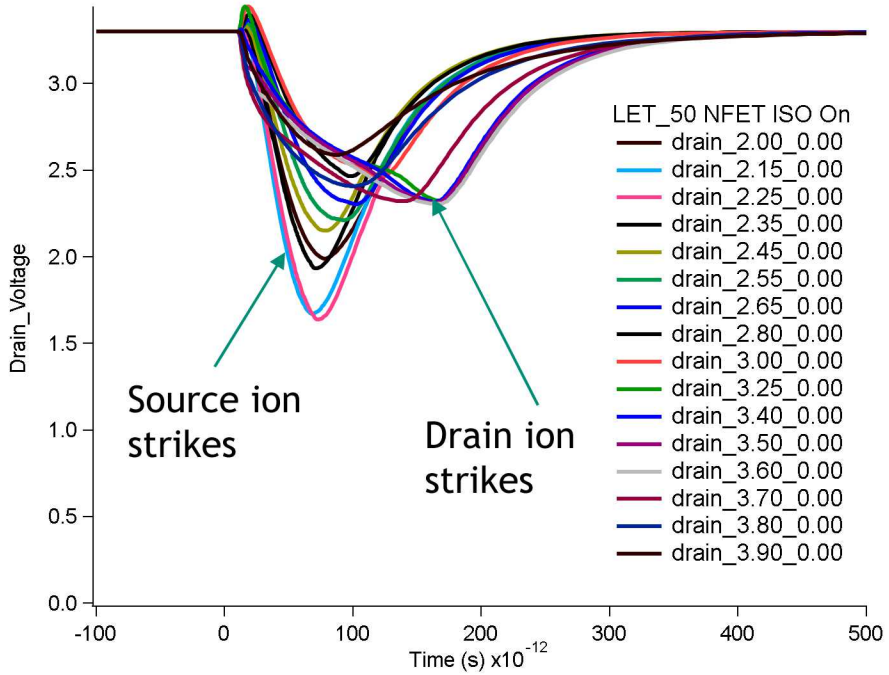


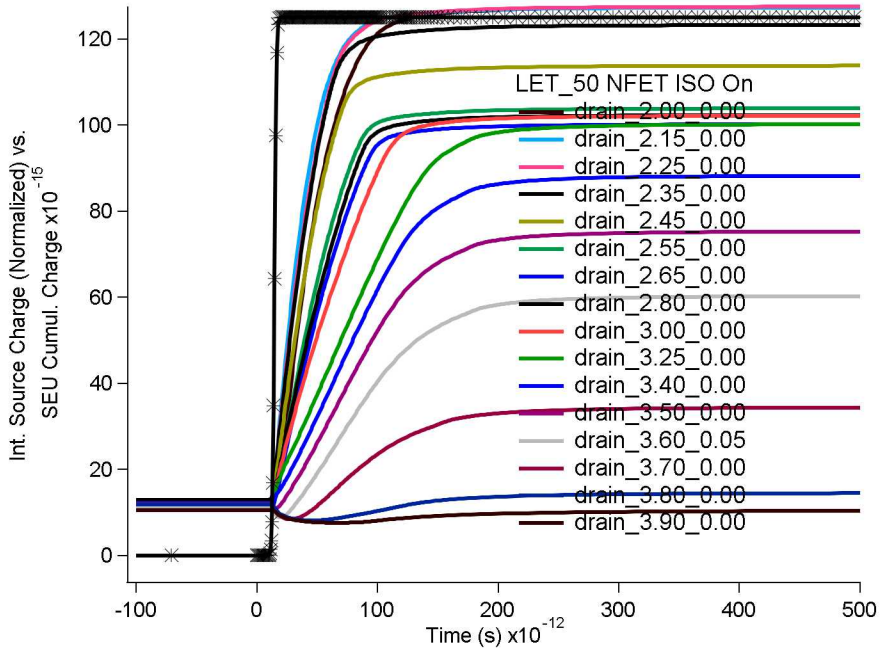
TCAD Modeling - Transmission Gate ON

Ion strikes to the drain will not displace the voltage enough to propagate a voltage transient

Ion strikes to the source just are starting to displace the voltage enough at LET = 50

- This is a small region
- Charge collection is relatively high, but voltage displacement is not reflective of the charge collection
  - Used FWHM characteristic to set charge collection volumes

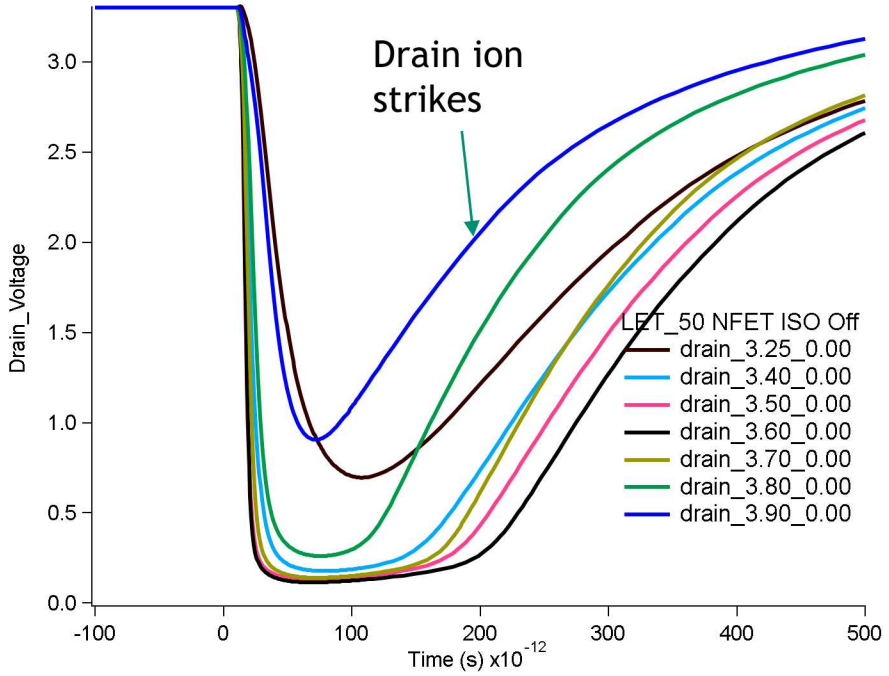


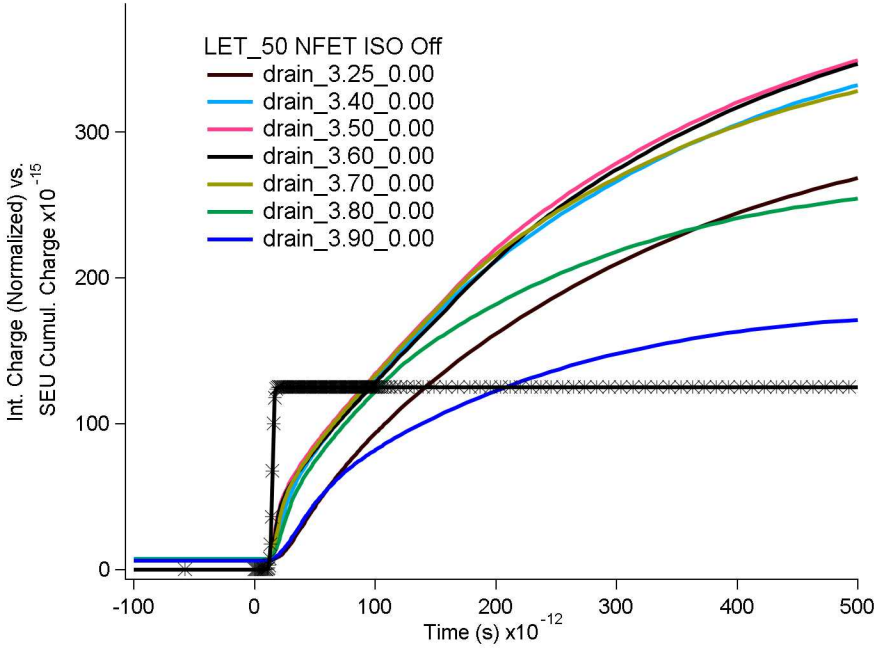


TCAD Modeling - Transmission Gate OFF

This looks a lot like the NBUSFET in the inverter configuration

More charge collection but a lot after the transient is over, takes longer to restore the transistor





Single Event Upset Test Results

Texas A&M Cyclotron, 15MeV/AMU

Test Conditions

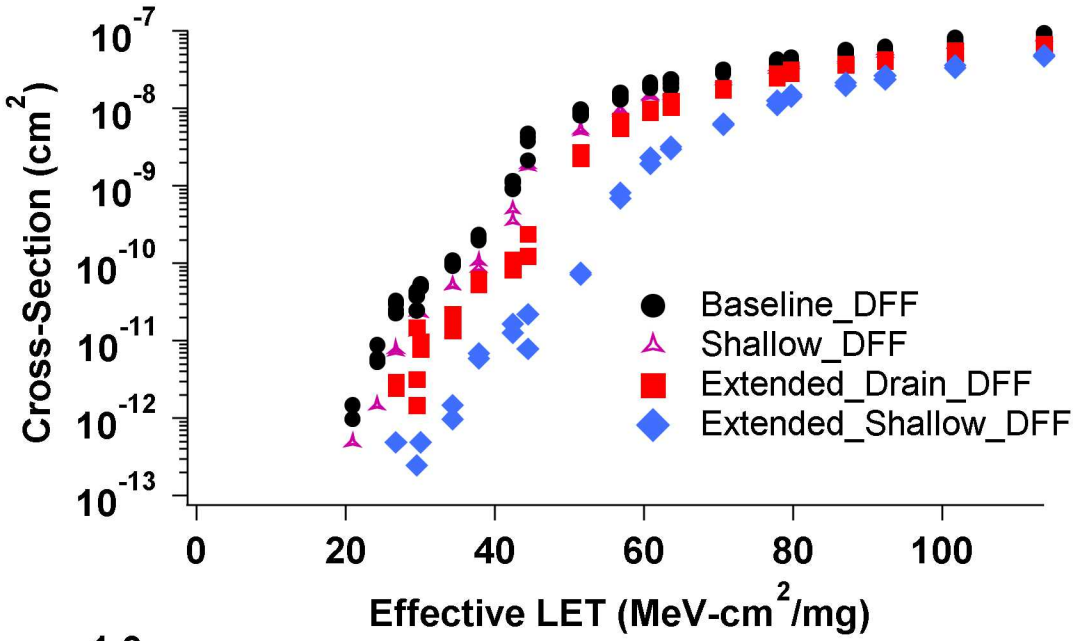
- 2048 bit DFF shift registers
- 3.0 V, 1 MHz, alternating data pattern
- Ions

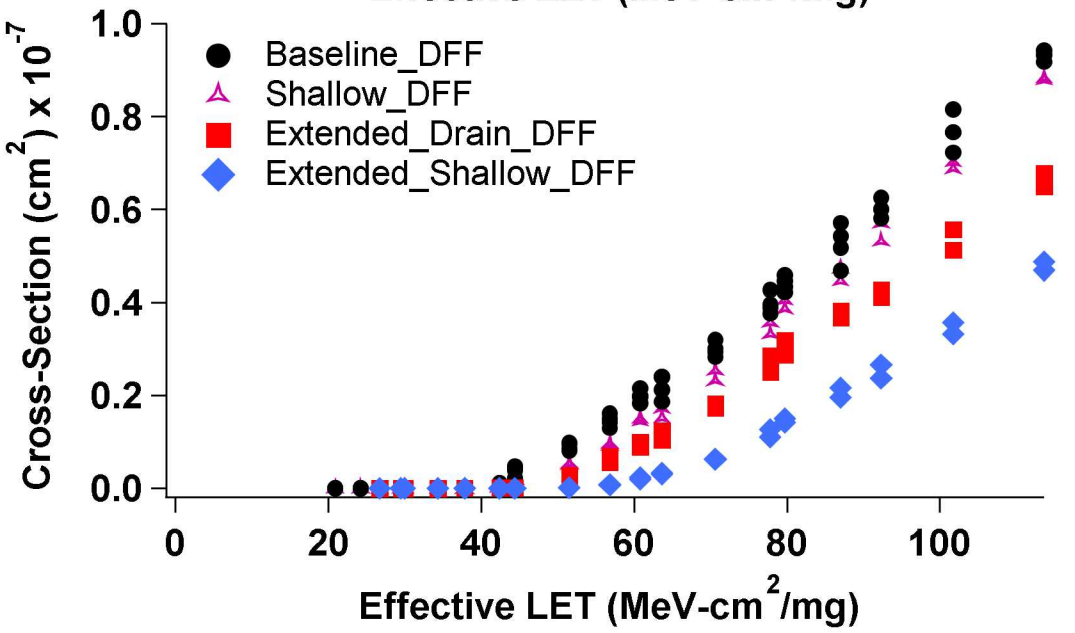
Ion	LET at Si, MeV-cm²/mg	Energy at Si, MeV
Cu	20.9	689
Kr	29.5	896
Ag	44.4	1083
Pr	60.8	1351
Ta	79.7	1702

- Incident angles – 0, 30, 38, and 45 degrees

SEU hardness from least to most

- Baseline
- Shallow
- Extended Drain
- Extended Shallow





MRED Modeling

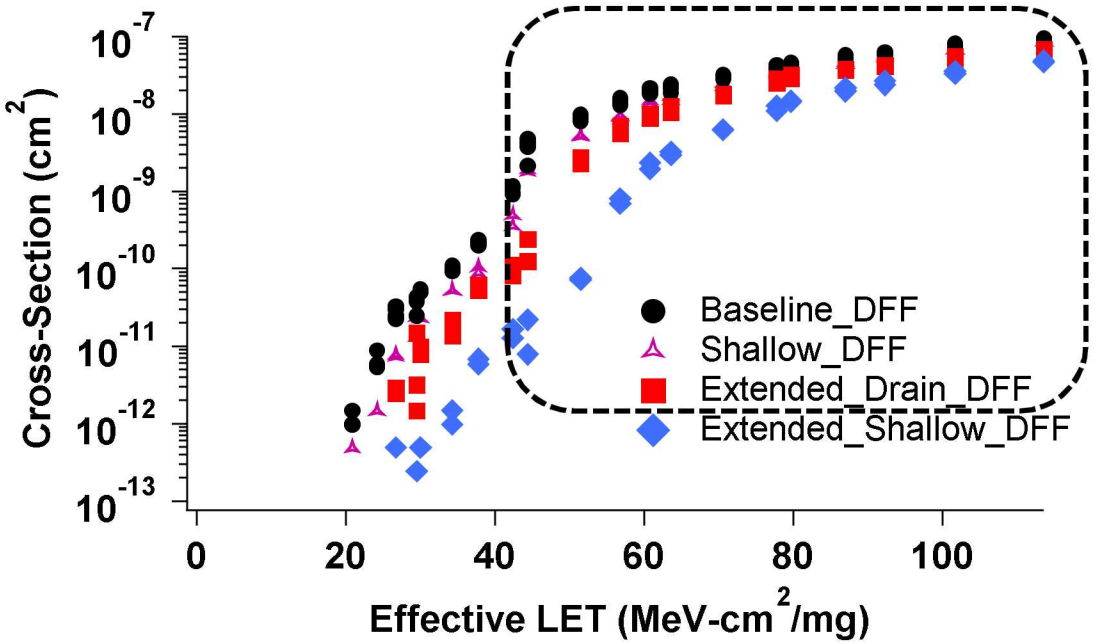
Goal is to understand why shallow DFFs do not eventually have a higher cross-section since target area is much bigger

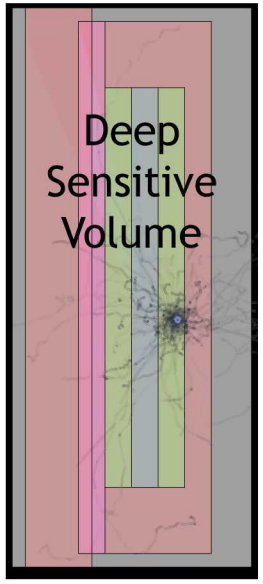
Modeling focused on direct ionization region of the test data

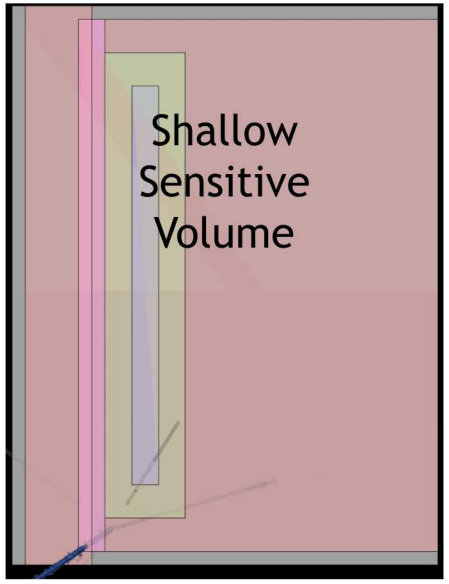
- Upsets at effective LETs below that region are the result of direct ionization plus a rare event
- Target material only includes Si – 40 μm x 40 μm x 25 μm
- Require BEOL materials near the sensitive volumes to calibrate lower effective LET region

Sensitive volume construction

- 3 sets of volumes
  - Deep NMOSFET
  - Shallow NMOSFET
  - Deep PMOSFET







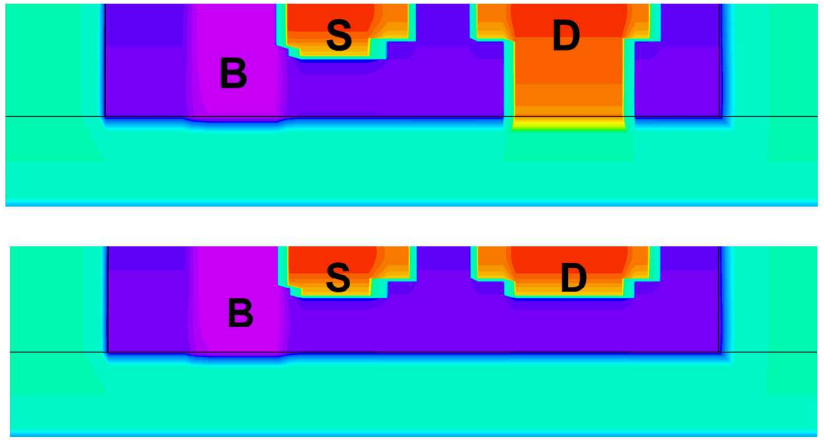
MRED Modeling

Key challenge is getting the critical charge (nodal capacitance) accurate

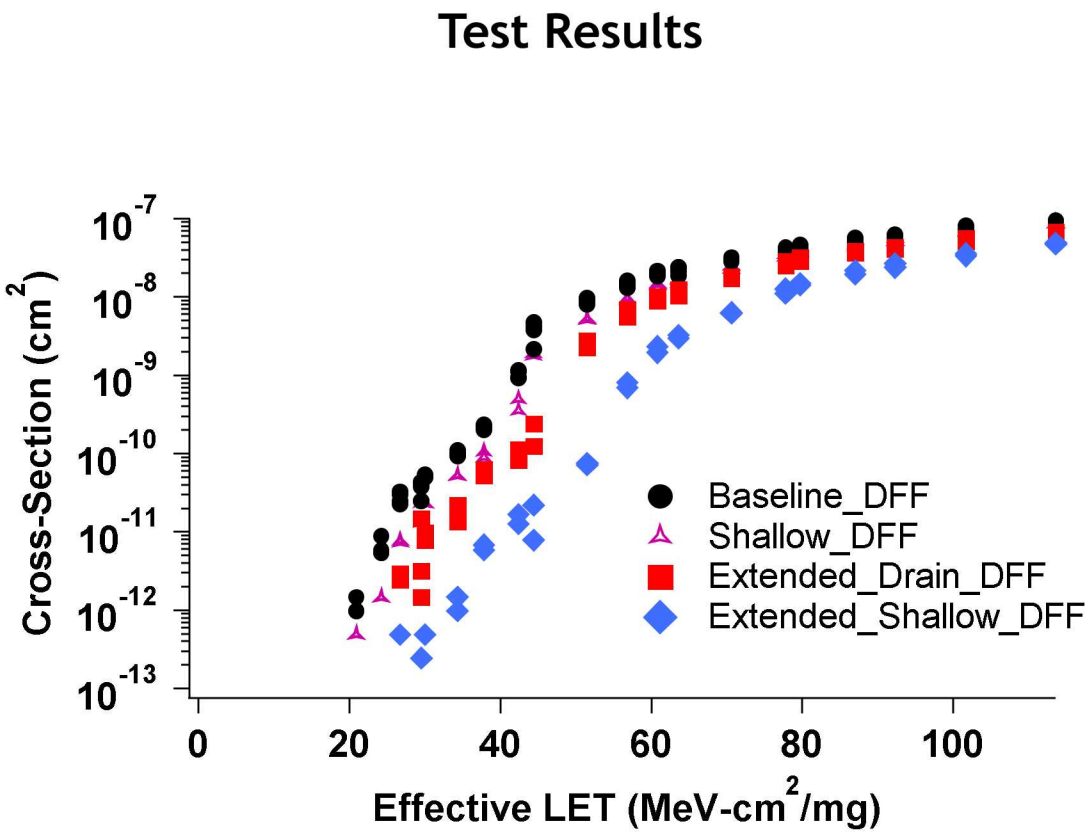
- Figures show TCAD cut planes of deep and shallow NMOSFETs
- Drain-body junction capacitance is the main difference between these transistors
  - Deep NMOSFET has perimeter based calculation
  - Shallow NMOSFET has perimeter and area based calculation

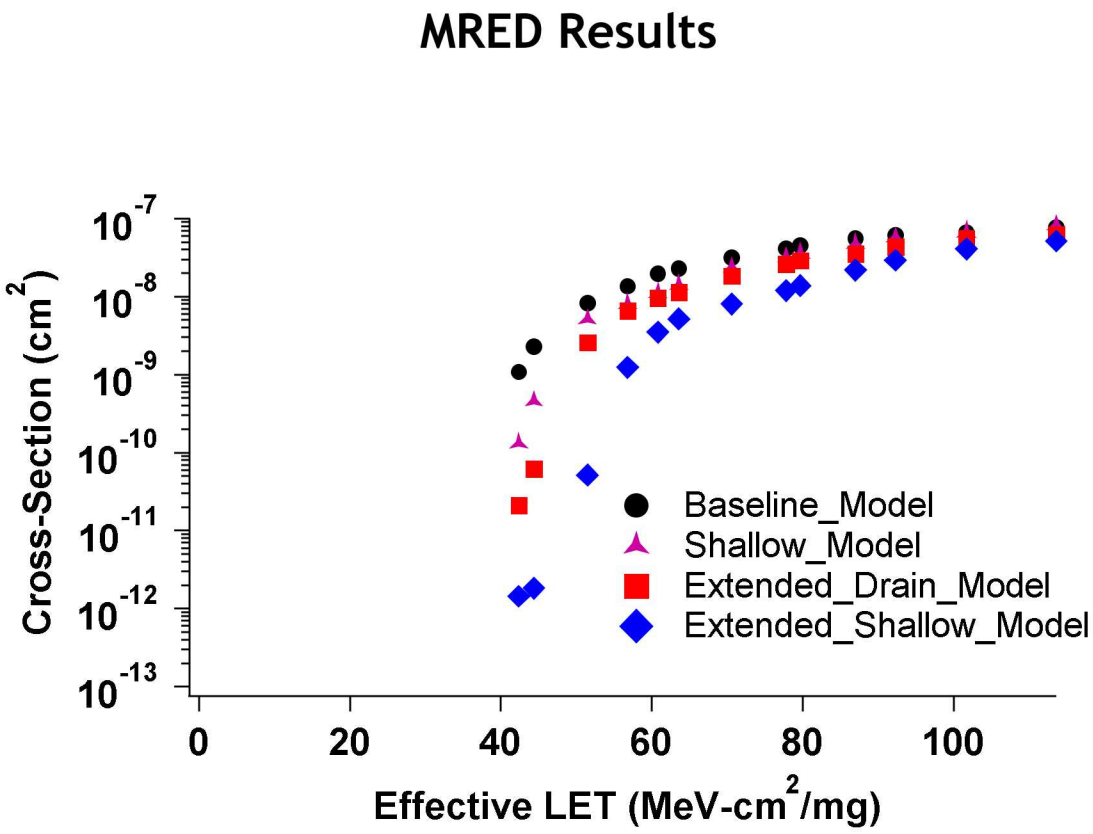
MRED Conditions

- 10M samples
- Rare event bias – 200x
- Critical charge determined by SPICE simulation



MRED Simulation Results

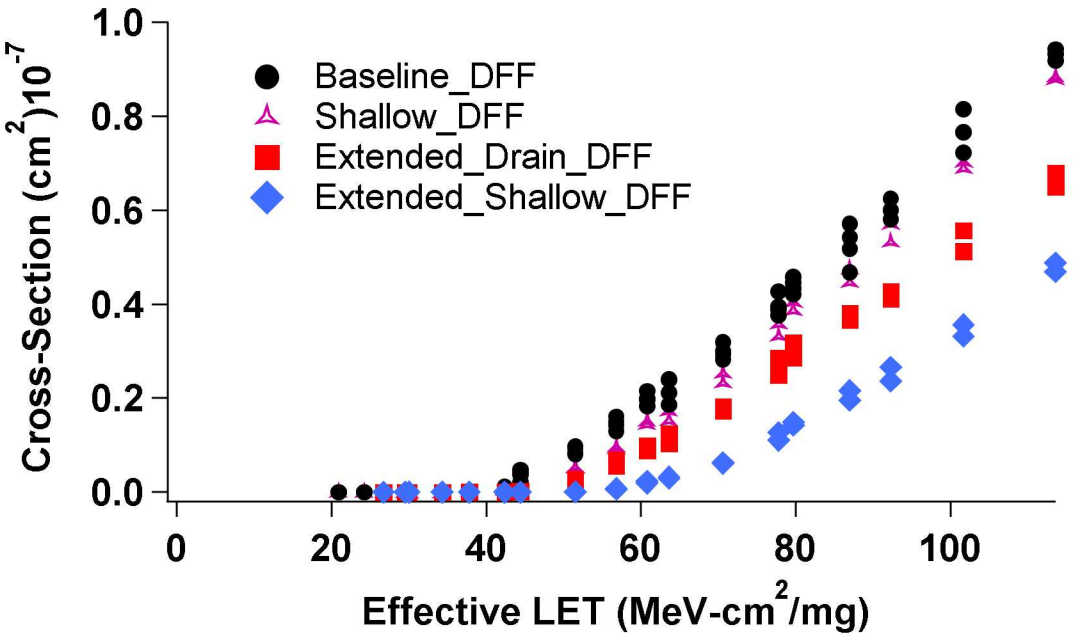


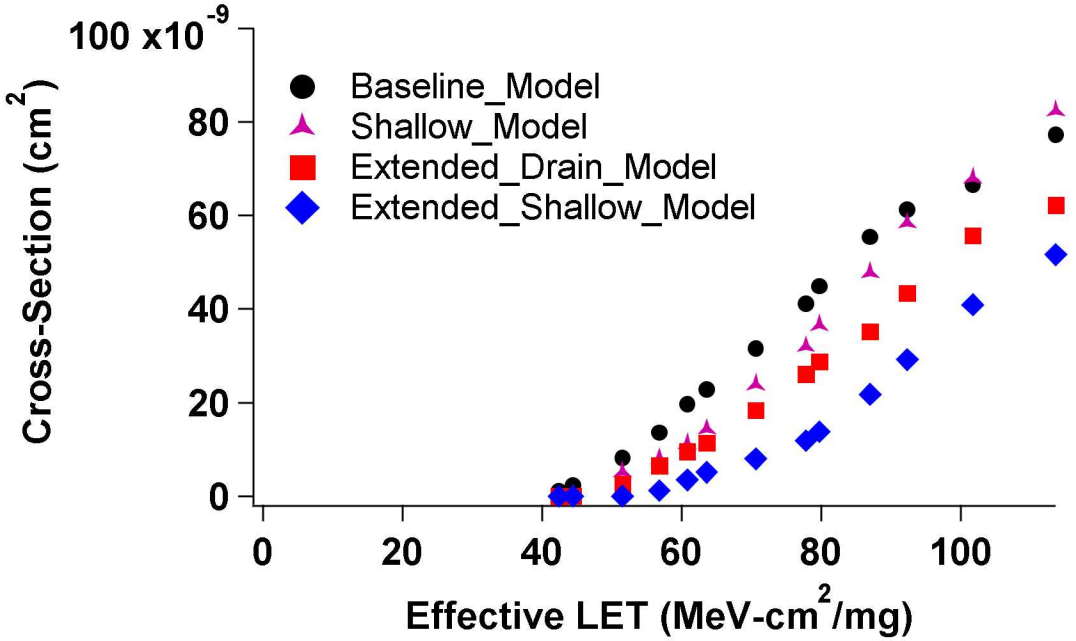


MRED Simulation Results

MRED simulations match pretty well until upper LETs

- Baseline simulation has one of the transistors saturated at about LET 80, no increase in cross-section – probably need to model more of the transistor with charge collection volumes and less efficiency
- This also hold for the highest point of the extended drain





Hardness By Design Implications

Increase in shallow sensitive volume cross-section is offset by increases in node capacitance (critical charge) and reduced bipolar gain

Drain size increases may not negatively affect SEU performance

IFET hits are primary contribution to hardness – lowest critical charge and highest bipolar gain

HBD Penalties

- Size
  - Shallow versus deep implant – no penalty
  - Extended versus standard – 36% increase, but could be lowered with optimal application
- Speed – Clock to Q (typical transistor models)
  - Baseline – 398ps
  - Shallow – 407ps
  - Extended Drain – 408ps
  - Extended Shallow – 435ps

Case Study #2 – Multiple Node Charge Collection Mitigation in Global Foundries 32nm SOI Process

Review of Single Node Charge Collection Hardened Design Options

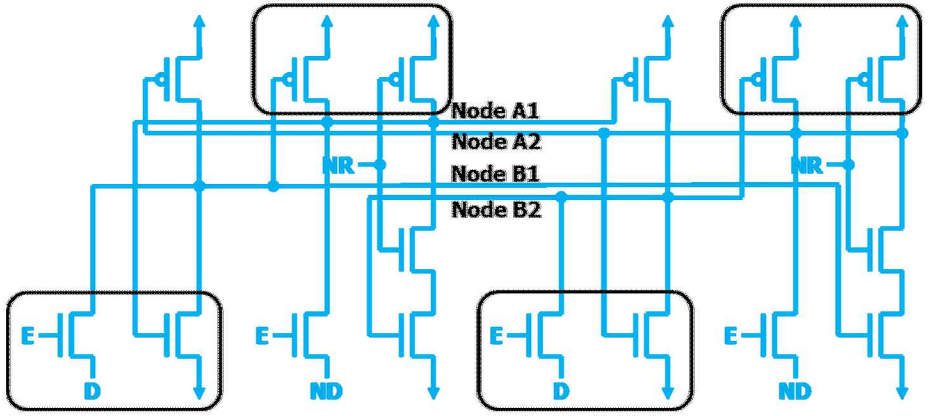
Multiple Node Charge Collection Mitigation Designs/Layouts

Ground-Based Testing Challenges

Modeling Results

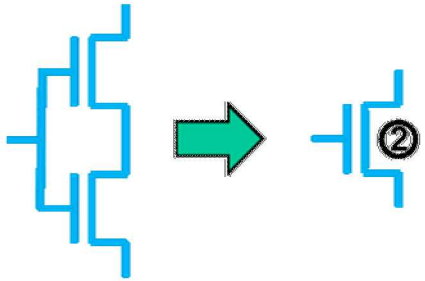
Single Node Charge Collection Mitigated Designs

Dual Interlocked Cell (DICE)



Transient Immune Composite Logic (TICT) or Stacked

- Only works when transistors are fully isolated, e.g. SOI



Triple Modular Redundancy (TMR)

- Triplicate circuits and vote out errors

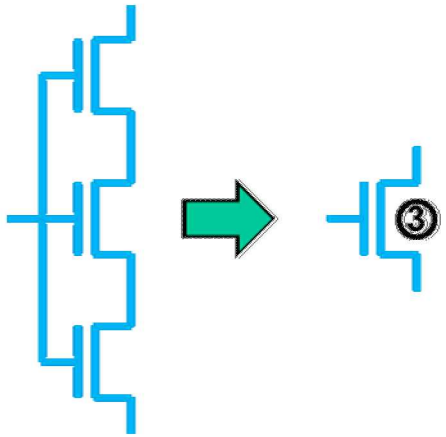
All are susceptible to co-incident charge collection events in two specific circuit nodes. Keeping those maximally separated in the layout is an important part of the design.

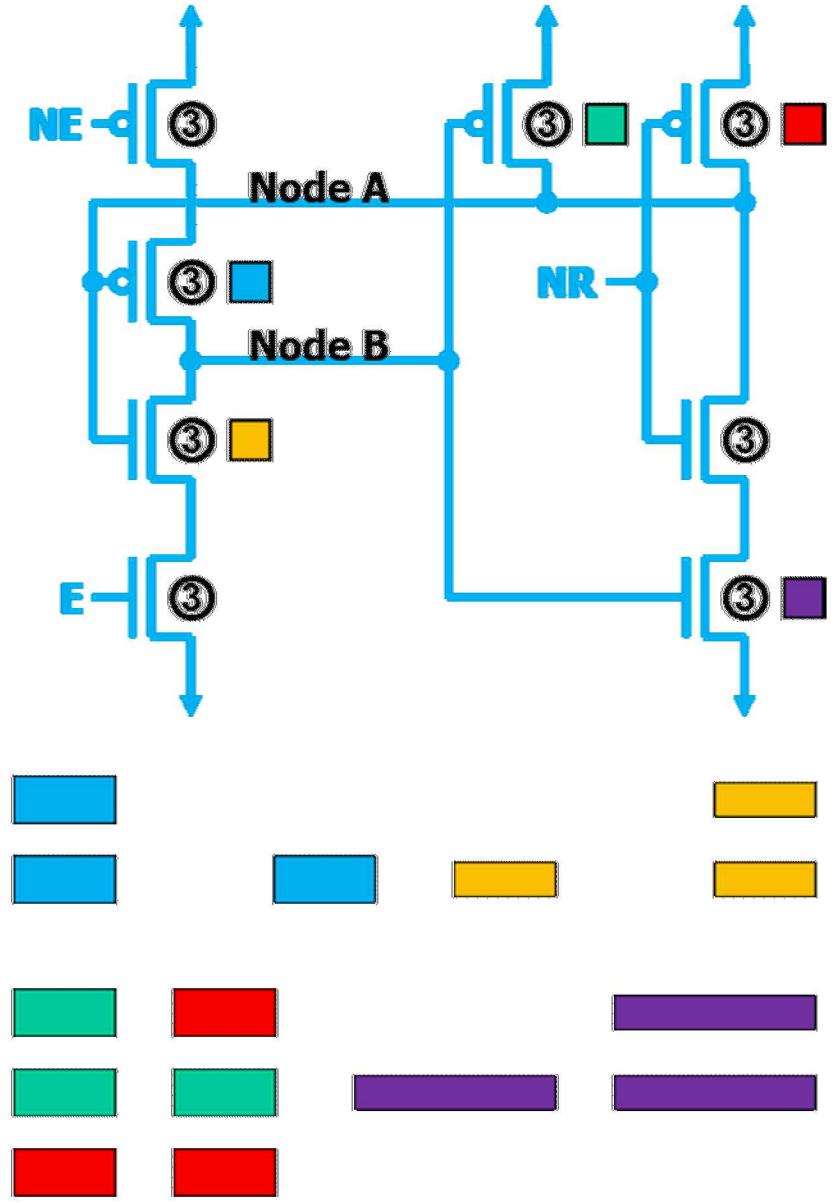
Triple Stacked Transistor Latch

Triple stacked transistor islands should not be colinear in layout.

- Right triangle layout shown

Requires sufficient charge collection in all 3 transistors in a stack to potentially cause upset.



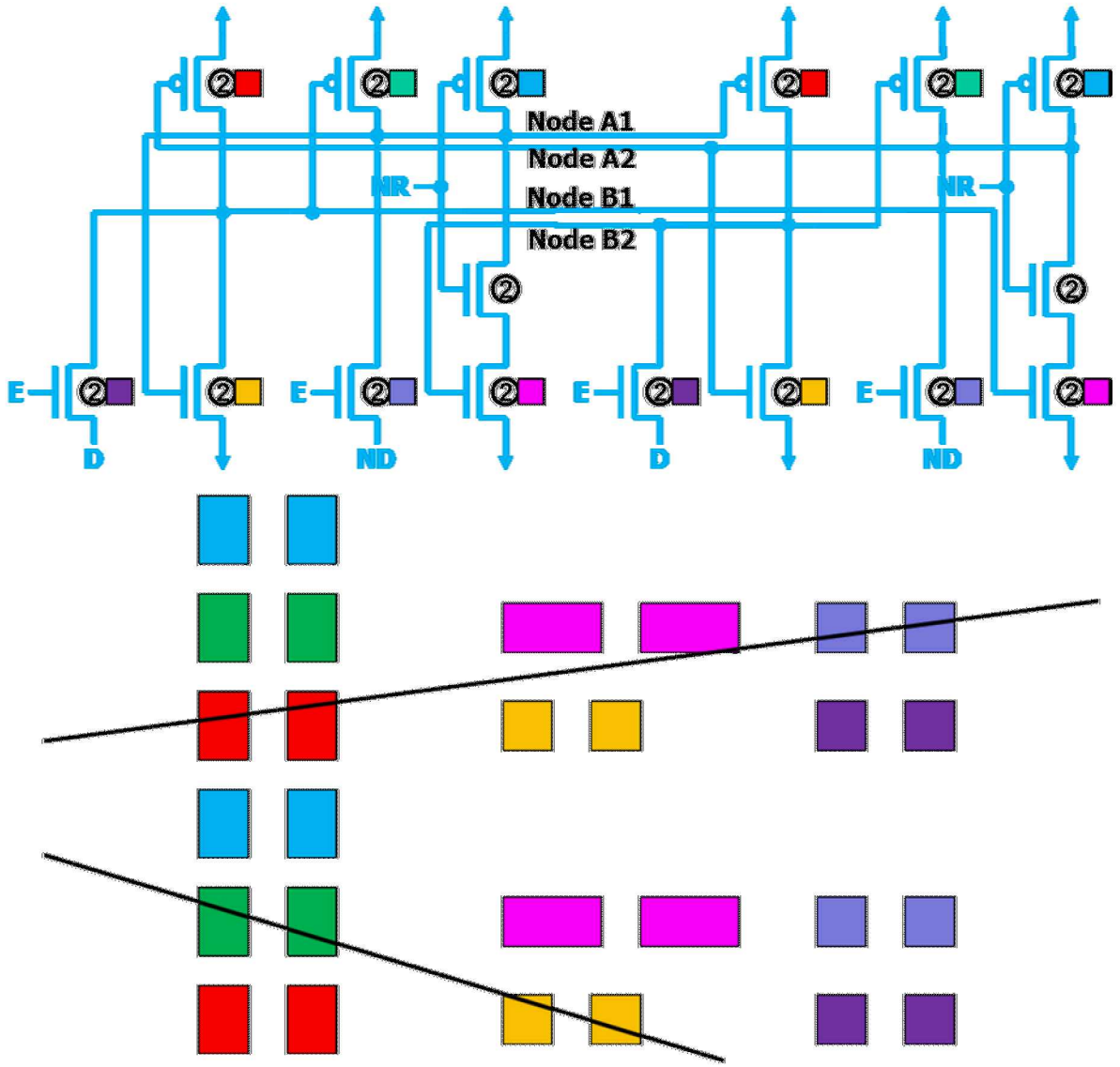


Stacked DICE Latch

Vertical DICE Redundancy

Horizontal Stacking Redundancy

Requires sufficient charge collection in 4 specific transistors to potentially cause upset



Ground-Based Testing Challenges

Ions/Particles lose energy as they pass through semiconductor materials, especially metals

The higher the grazing angle of incidence to the surface of the IC, the longer the path through the metal layers

- Ground-based accelerators don't produce ions with sufficient energy to go near lateral in an IC
- But, these ions and energies exist in the space environment

Testing works pretty well for standard, soft designs where charge collection at a single node is the primary failure mechanism – Data can be used to reasonable predict upset rates in an environment

Advanced designs/layouts can't be adequately evaluated through testing

- Modeling and simulation is the only way to predict error rate
- Test results aid in calibrating models

Modeling Results

MRED Simulation Parameters

- 100 Million Monte Carlo samples per data point
- Multiple Node Event Count is 2 for DICE, 3 for Triple Stacked, and 4 for Stacked DICE and in specific node combinations
- Isotopically incident ions

Latch Type	45 MeV He		178 MeV Ni		531 MeV Ar		785 MeV Cu		1032 MeV Kr	
	Single Node Event Count	Multiple Node Event Count	Single Node Event Count	Multiple Node Event Count	Single Node Event Count	Multiple Node Event Count	Single Node Event Count	Multiple Node Event Count	Single Node Event Count	Multiple Node Event Count
Standard	283	N/A	111,815	N/A	151.282	N/A	157,445	N/A	158,036	N/A
DICE	747	7	284,410	814	389,401	868	403,165	946	405,494	874
Triple Stacked	1,698	0	798,883	0	990,497	0	1,013,661	4	1,019,973	0
Stacked DICE	1,378	2	553,376	114	752,736	154	778,702	166	783,126	160

Summary

Modeling and simulations has become an integral part of single event effects understanding

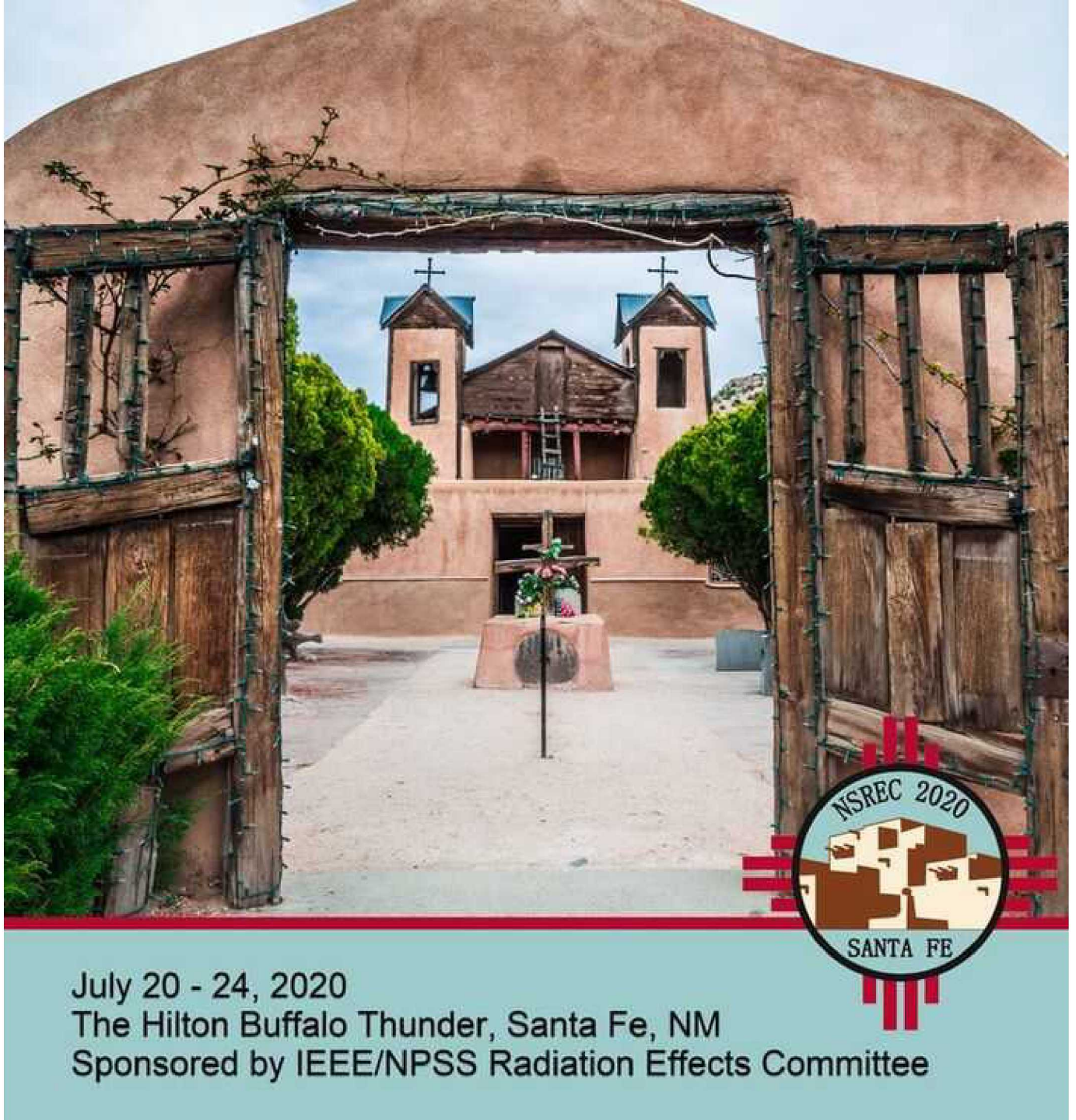
Single event effects are for the most part a 3D transient simulation problem

- Very time consuming simulations
- Shortcuts, using 2D simulation or reducing physics being modelled, usually leads to errant results

There is not one modeling and simulation tool that does everything

- 3D TCAD handles carrier drift and diffusion well, but only emulates single event charge deposition
- 3D MRED handles particle physics and produces energy deposition, but cannot inform about the importance of the generated carriers
- Circuit simulation can emulate single event charge collection, but has no spatial information

IEEE TNS Nuclear and Space Radiation Effects Conference (NSREC) is coming to Buffalo Thunder this July


NSREC 2020
SANTA FE
July 20 - 24, 2020
The Hilton Buffalo Thunder, Santa Fe, NM
Sponsored by IEEE/NPSS Radiation Effects Committee