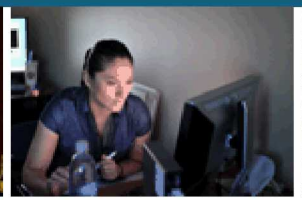
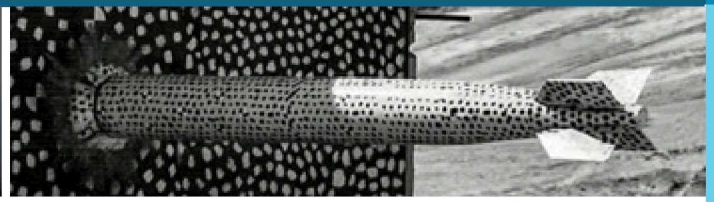
SAND2020-1820PE

hCMOS Pixel Design Imrovements





PRESENTED BY

Quinn Looker

hCMOS Workshop

Sandia NM 2/13/20

Sandia National Laboratories is a multimission laboratory managed and operated by National Technology & Engineering Solutions of Sandia, LLC, a wholly owned subsidiary of Honeywell International Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA0003525.

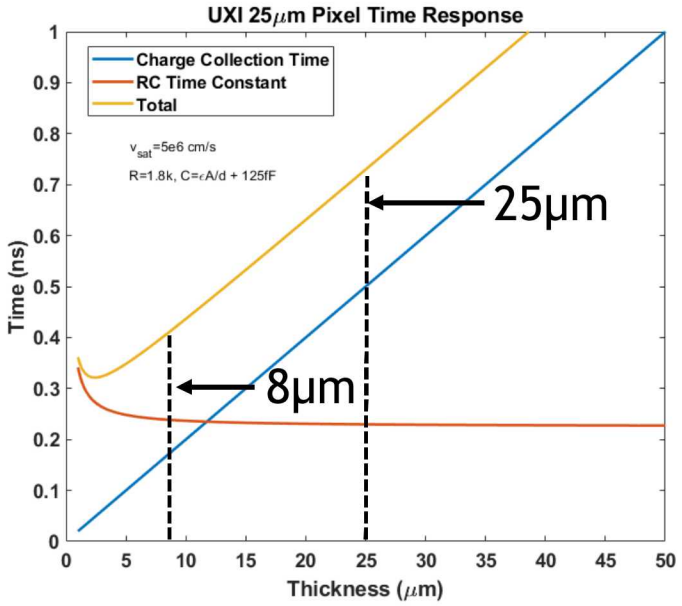
SAND

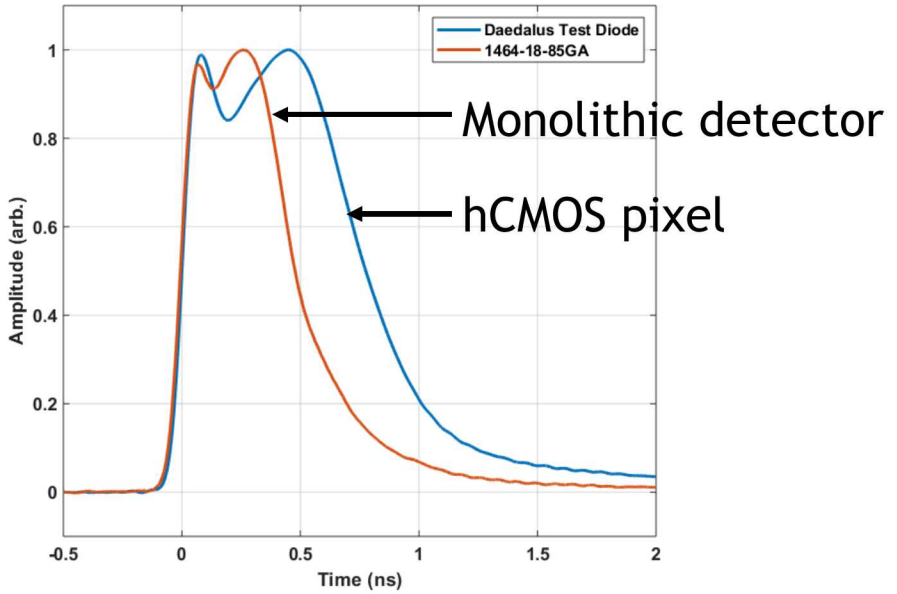
Temporal Impulse Response

The hCMOS pixel design has a slower than expected impulse response

- A first-principles calculation indicates <1 ns detector response
- Measurements on monolithic detector design confirm expectations
- Measurements on 25 μm pixels show significantly slower impulse response

- Icarus gate profile likely limited by detector response
- Future ROIC designs anticipate ~0.5 ns gate times
- **How can we reach 0.2-0.5 ns impulse response in the pixel?**





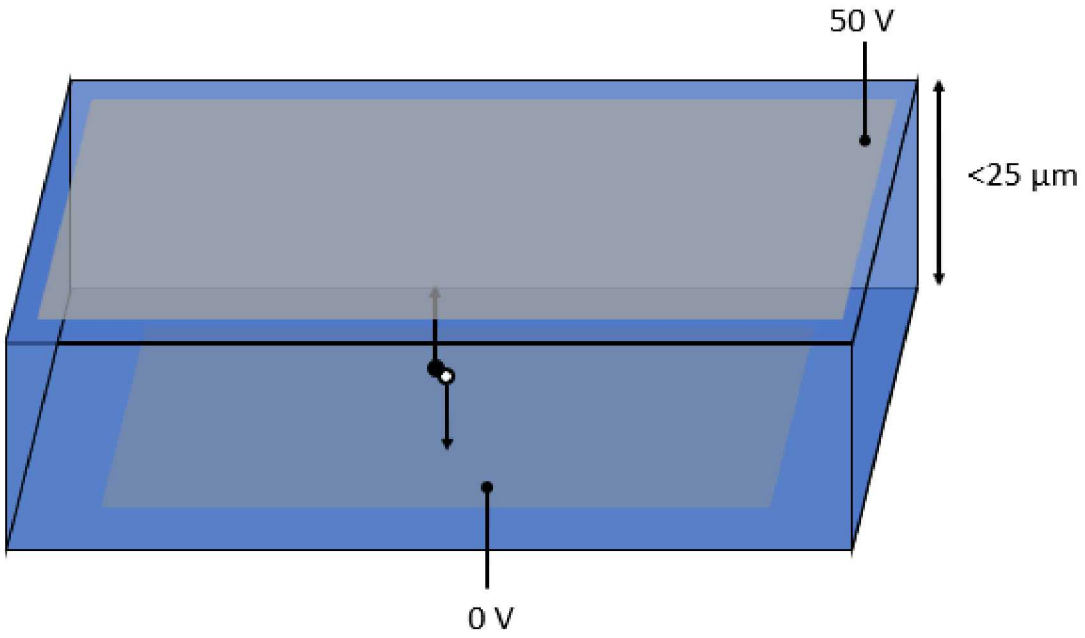
Potential Speed Improvements Summary

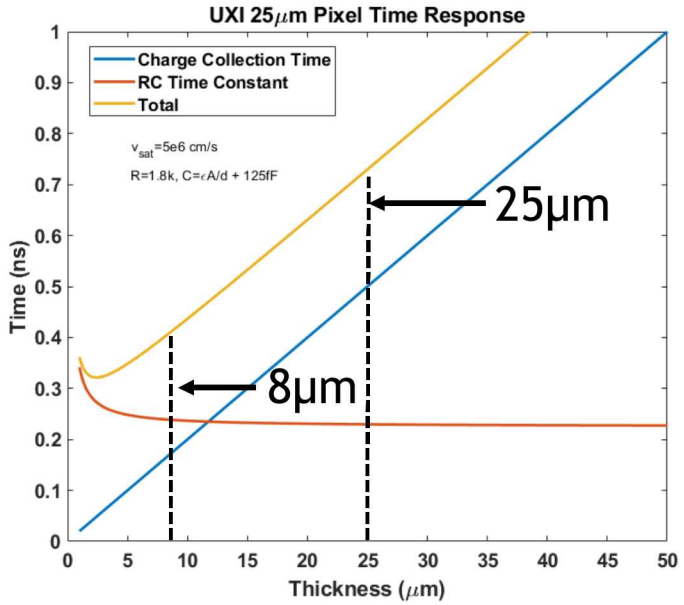
Availability

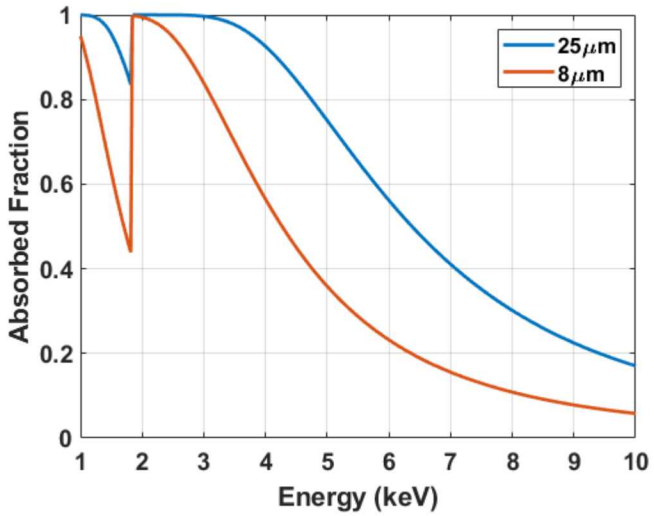
Method	Potential Reduction	Feasibility	
Thinner Absorber Layer	50%	Done	Undesirable QE reduction
Higher Electric Field	10-20%	New Diode Lot – in progress	Universal – stacks with other methods
Cooling	10%	New package needed	
Point Contact Electrode	40%?	Easy to fab, need to understand behavior	Some uncertainty as to how these will behave
Coplanar Grid Electrode	40%?	Can fabricate, need ASIC changes	
Trench 3D Diode	50%?	Some process development work done; more needed	Requires process development ($$$)
Cylindrical 3D Diode	60%?	Major process development work needed	

Thinner Absorber Layer

8μm thick diodes ~2x faster than standard 25μm





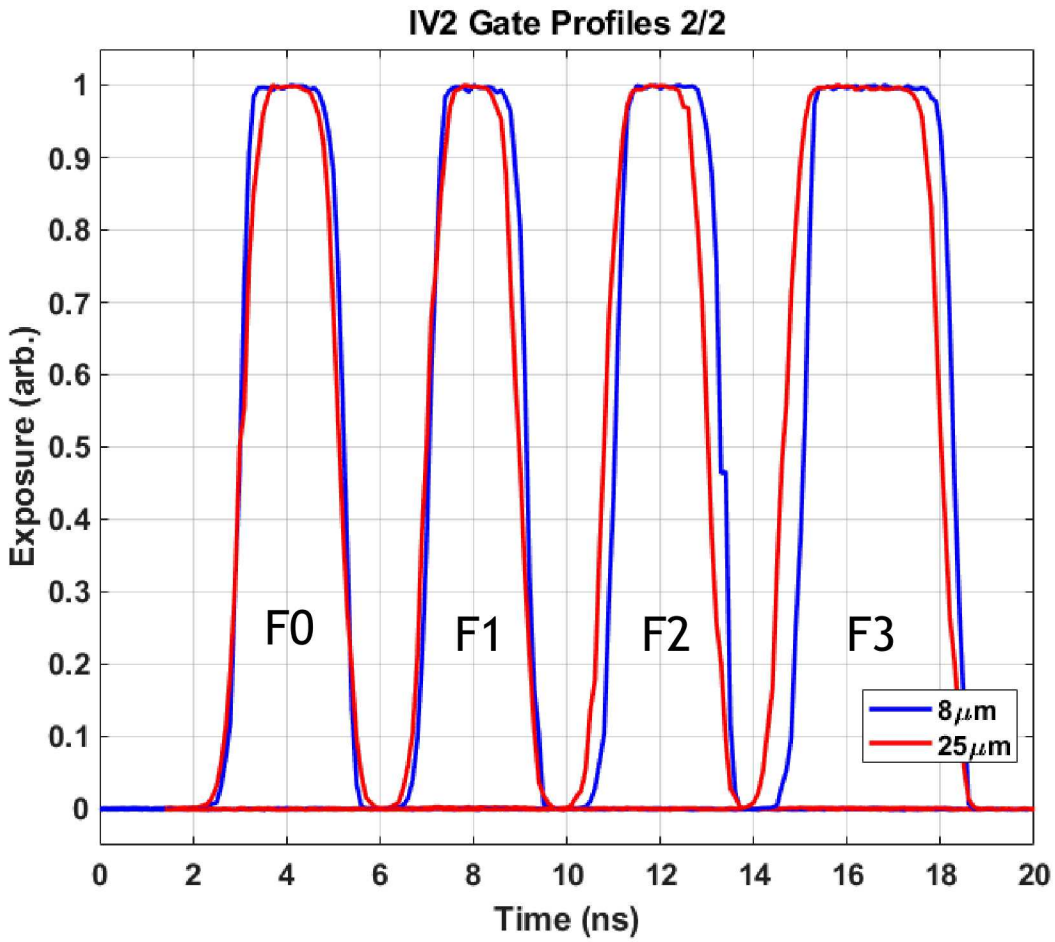


Key Features
-Proportional decrease in charge collection time with decreasing detector thickness
-Lower QE for all radiation types; may need thickness 10 μm or less
-Limit ~2 μm, where capacitance begins to take over

Feasibility: already done

Thinner Absorber Layer

- This is the difference in 2/2 timing for Sandia-configured systems – not particularly dramatic
- Livermore results vary?
- Also of note: this effect is at least partially due to increased electric field (50V/8µm compared to 50V/25µm)



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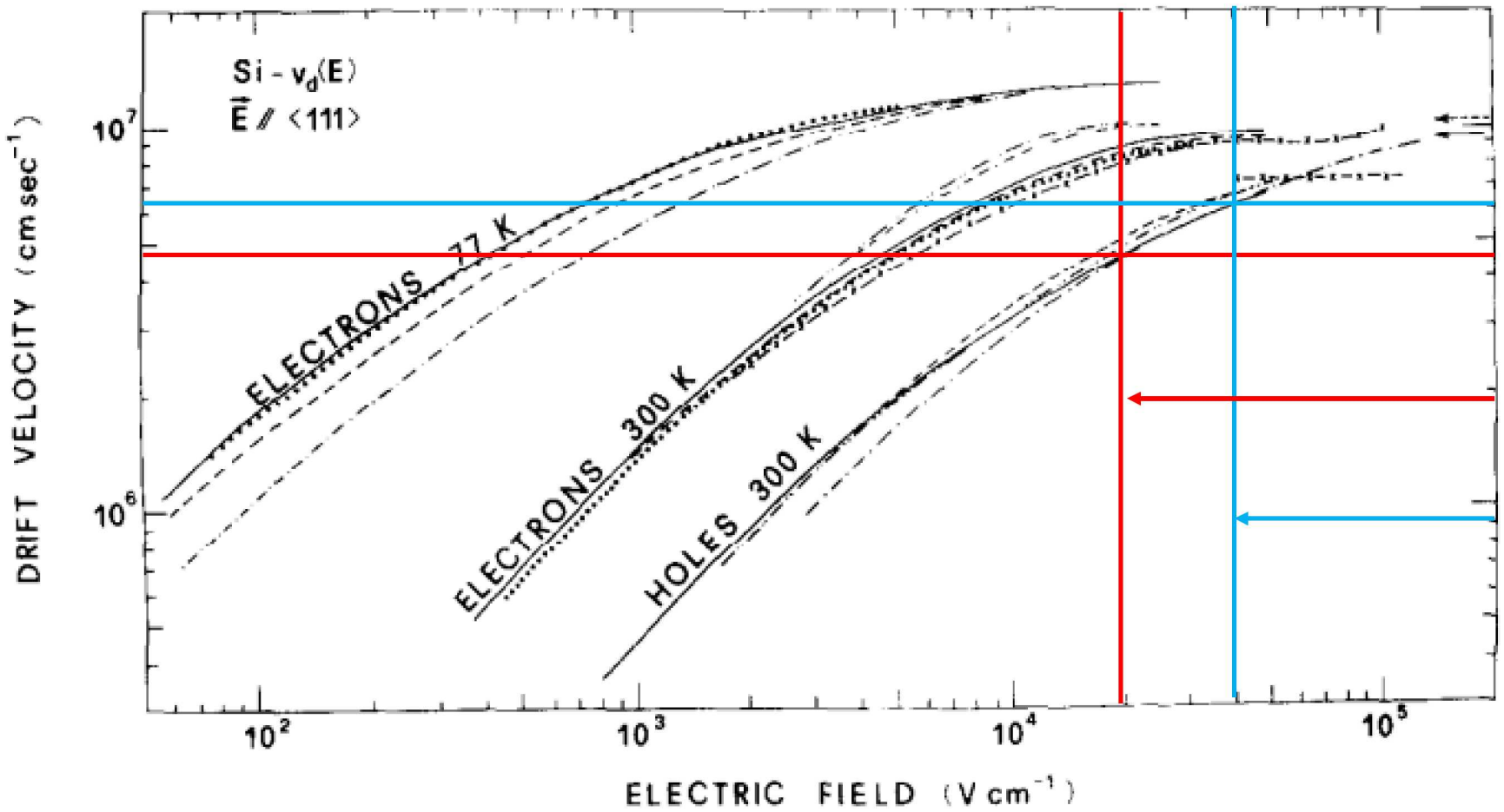
Increasing Electric Field

Jacoboni et al., Solid-State Electronics Vol. 20, pp. 77-89 (1977)



We are probably here
~5e6 cm/s

Maybe double E field?
~6e6 cm/s

Key Features
-Likely minor design changes will allow the option of higher bias
-May reduce yield
-Unmitigated speed increase for successful devices
-May require changes in bypass caps, power supplies

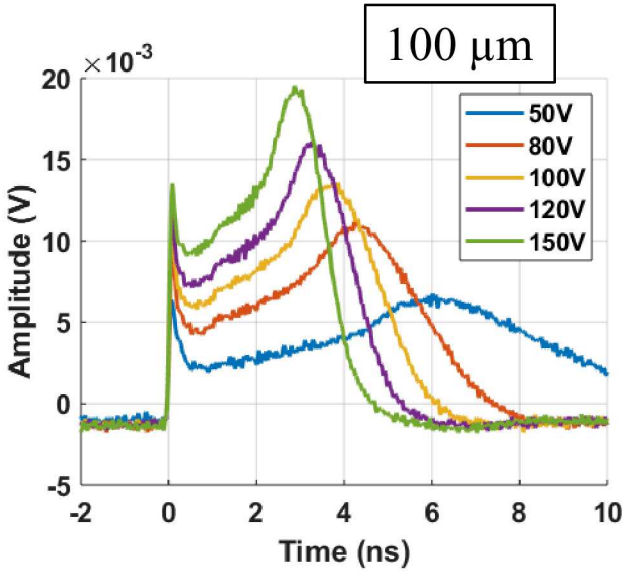
10-20% reduction

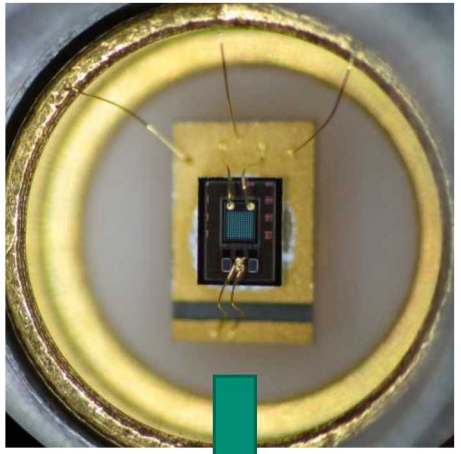
Feasibility: new diode lot

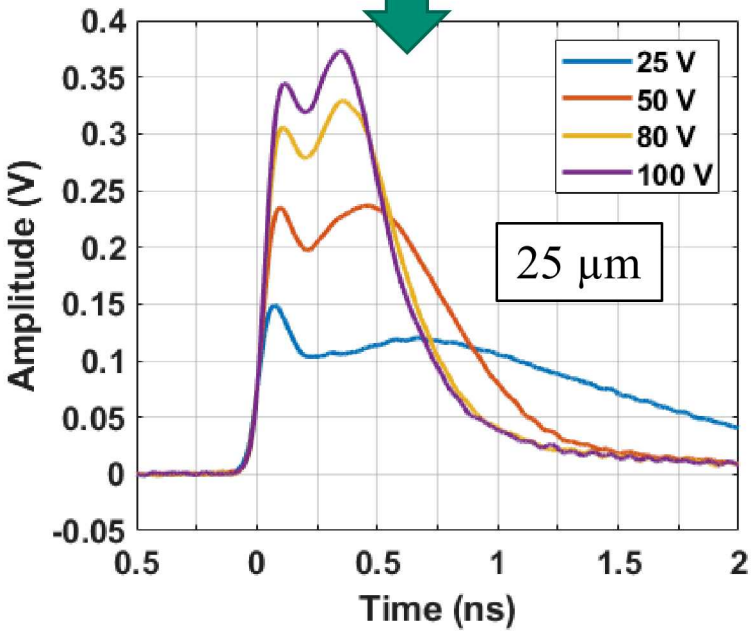
Increasing Electric Field

- Faster impulse response demonstrated in 25 µm thick hybrid Si photodiode by increasing bias
- Most effect seen in 2x voltage increase, diminishing return with further increases
- Added benefit of greater resistance to field collapse
- Semi-stochastic device breakdown – may reduce final yield

Critical for thicker detectors!







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Key Features
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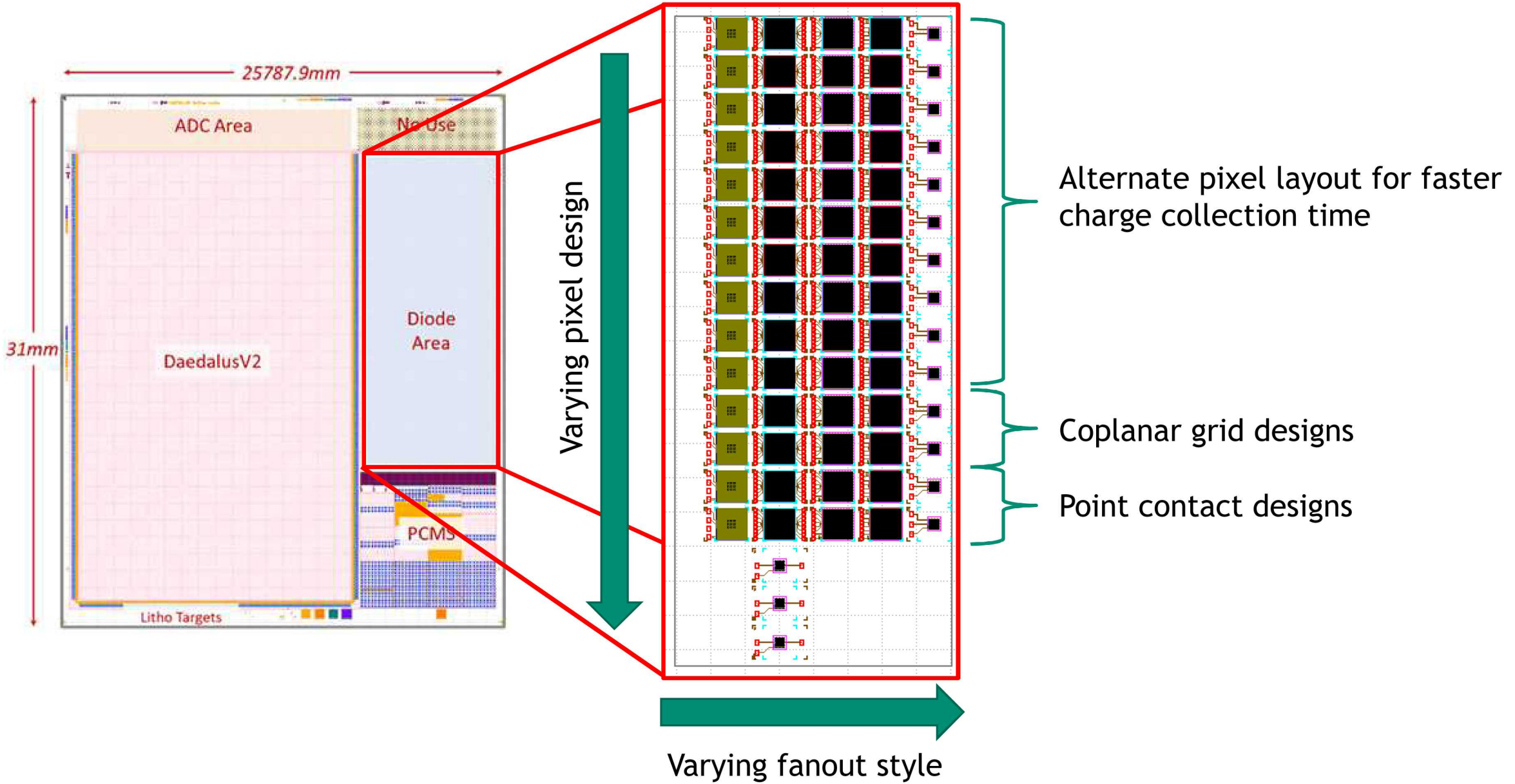
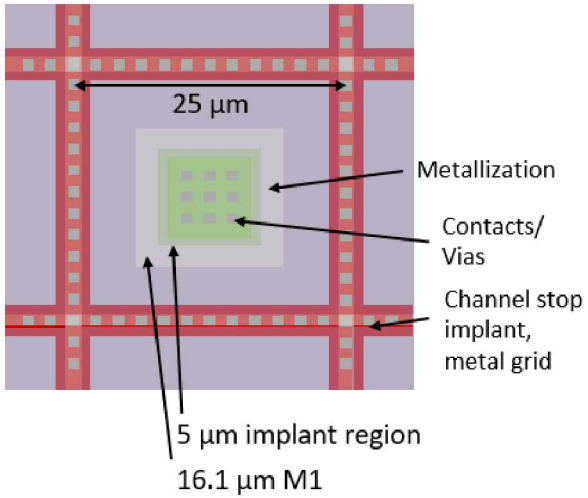
Feasibility: new diode lot

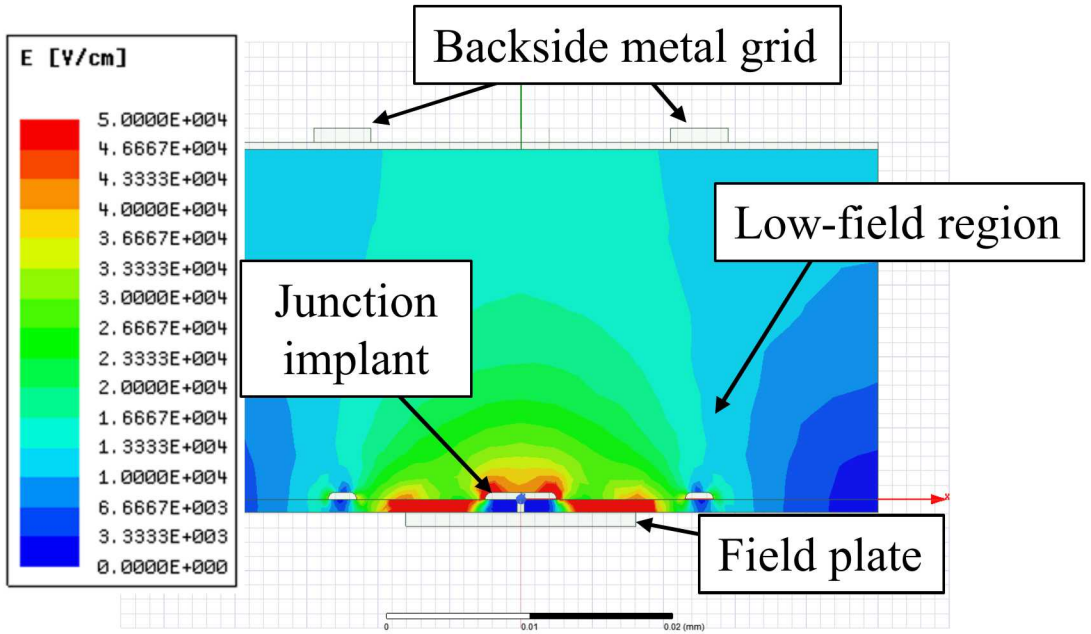
New Pixel Designs Will Be Tested

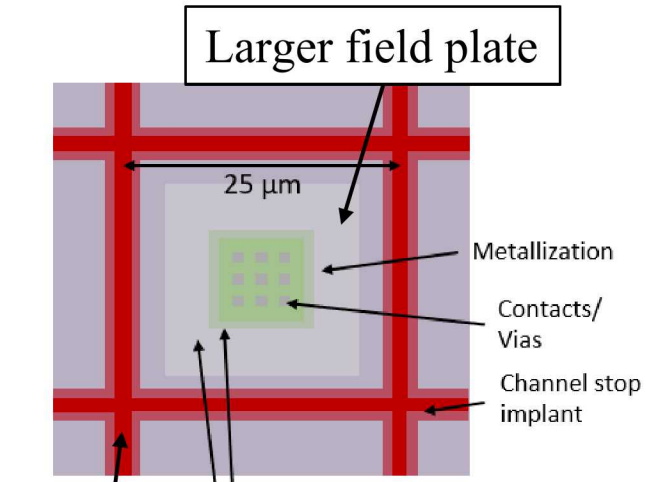


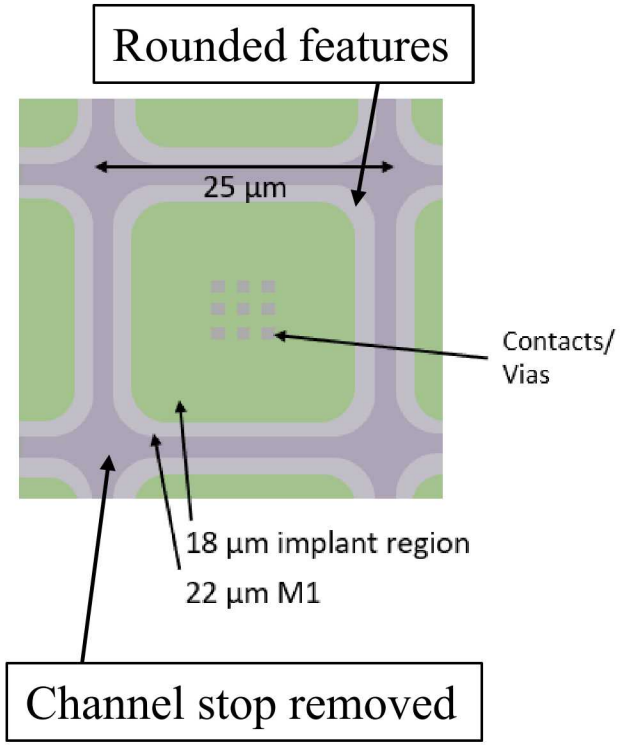
Example Structures

Present-day pixel design



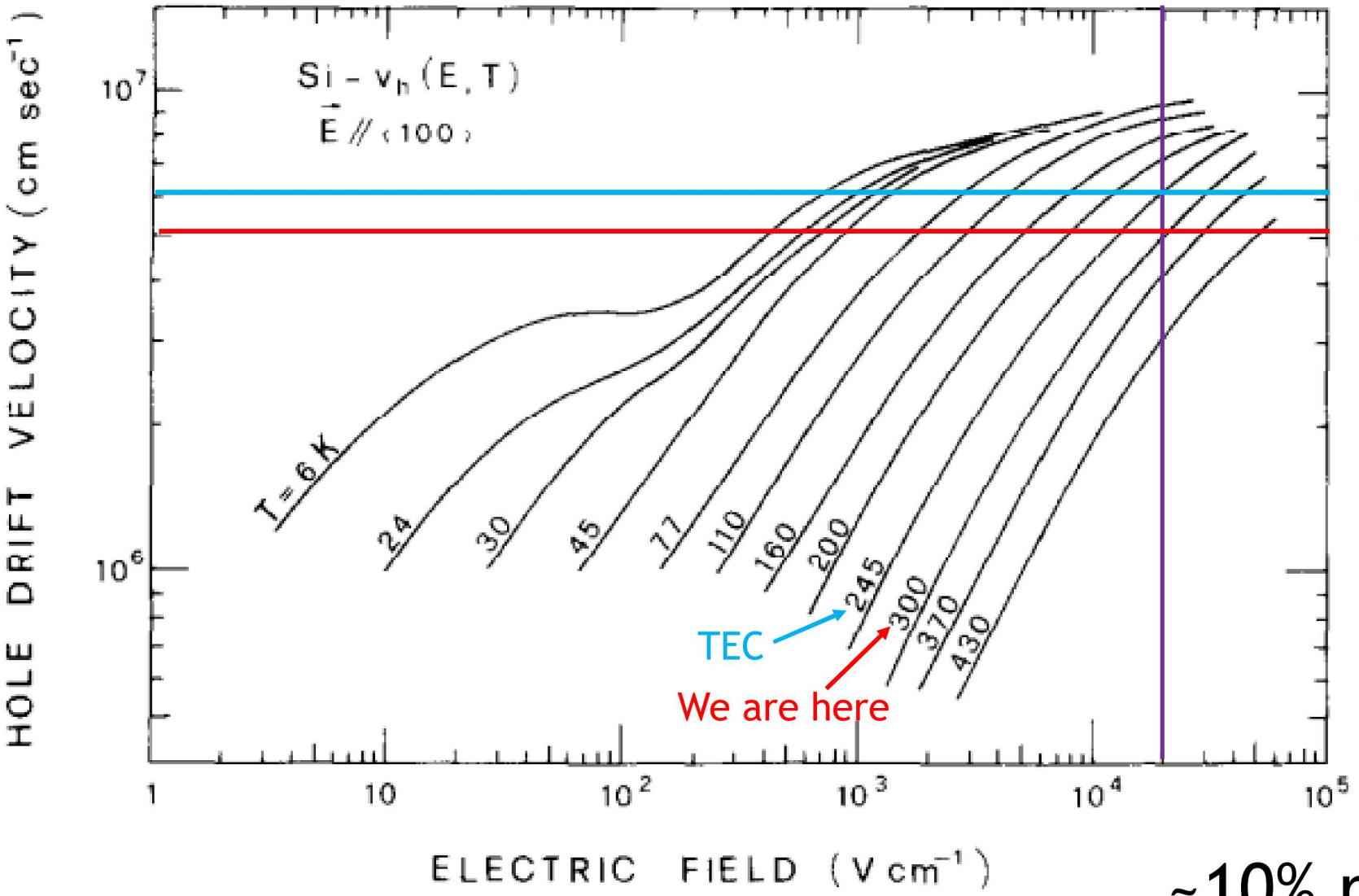






Cooling

Jacoboni et al., Solid-State Electronics Vol. 20, pp. 77-89 (1977)



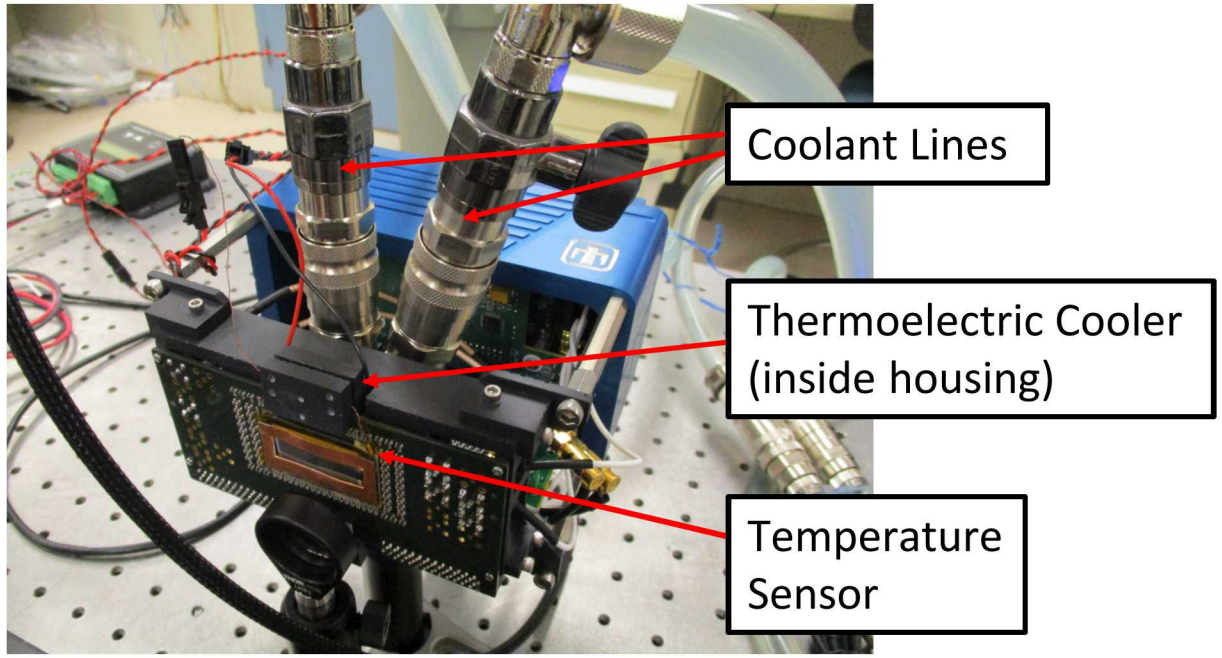
Key Features
-Complementary to other efforts
-Use is optional; no risk to baseline use case
-More complex camera operation

~10% reduction

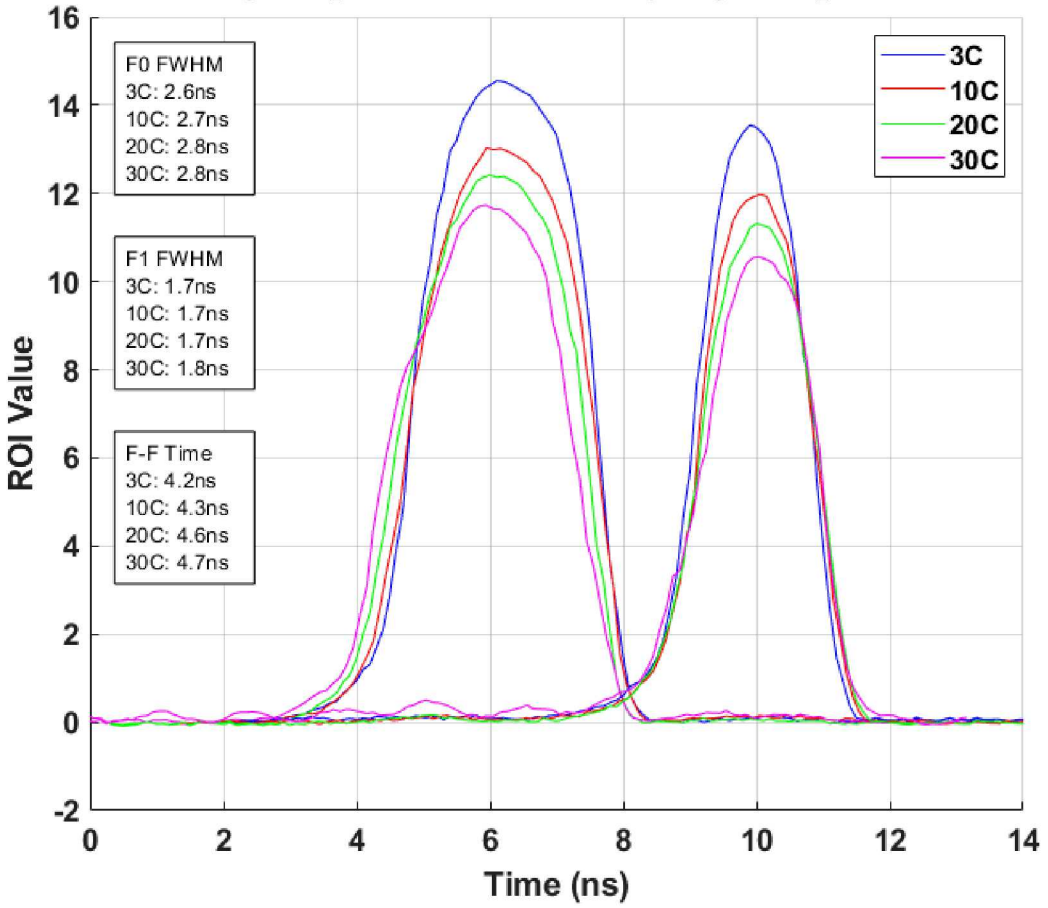
Feasibility: done
Need compatible package

Cooling

Hippogriff camera with thermoelectric cooler



Laser gate profiles with varying temperature



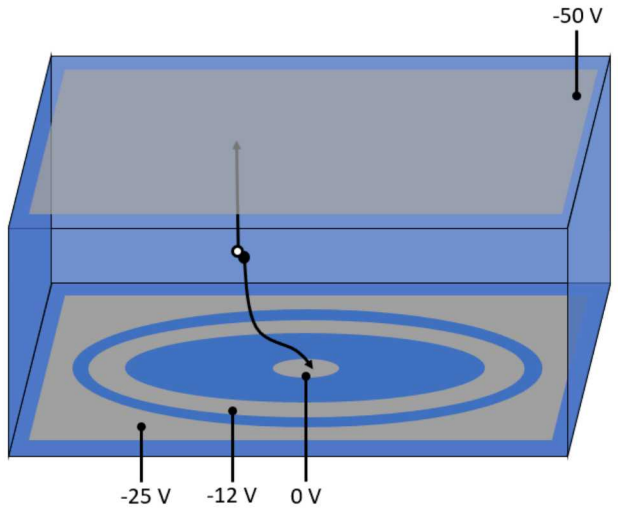
Key Features
-Complementary to other efforts
-Use is optional; no risk to baseline use case
-More complex camera operation

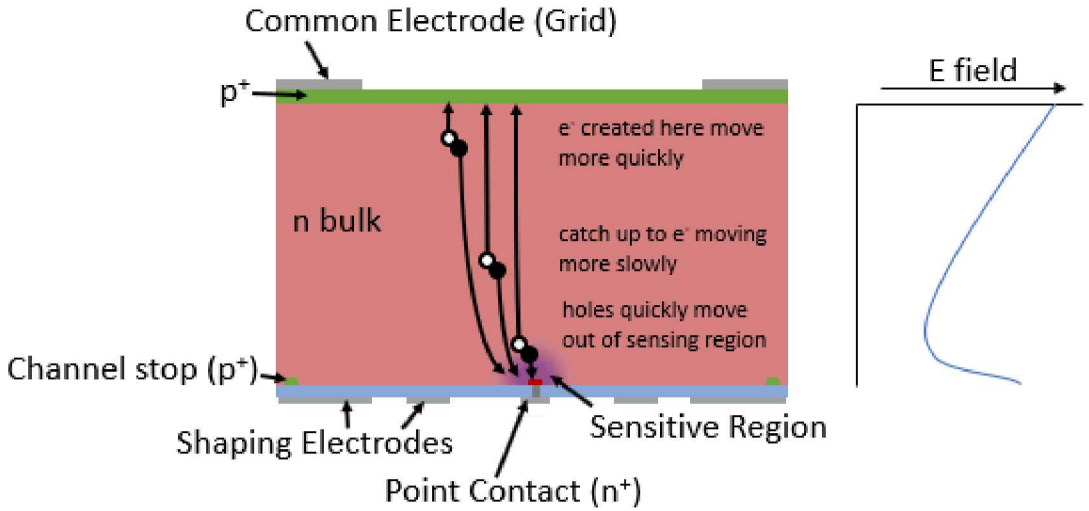
~10% reduction

Feasibility: done
Need compatible package

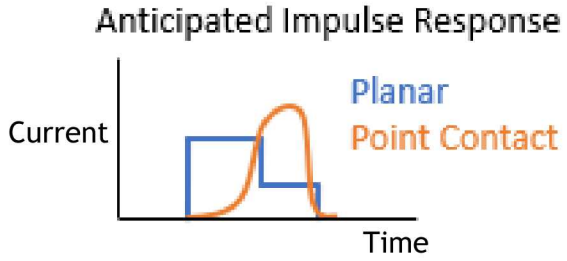
Other Electrode Configurations: Point Contact

This on its own may not offer much improvement. To fully take advantage of this electrode structure, we would need to move the junction to the illuminated side and collect electrons.





Key Features
-Small collecting electrode senses moving charge only in small volume nearby
-Field shaping electrodes needed to funnel charge to collecting electrode
-Secondary benefit of lower capacitance

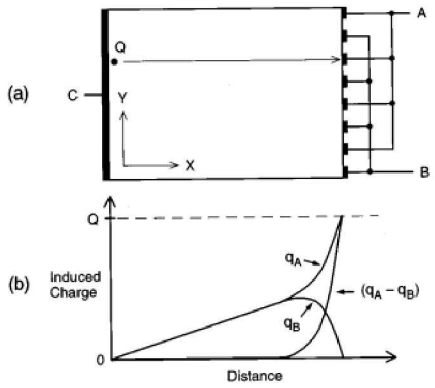


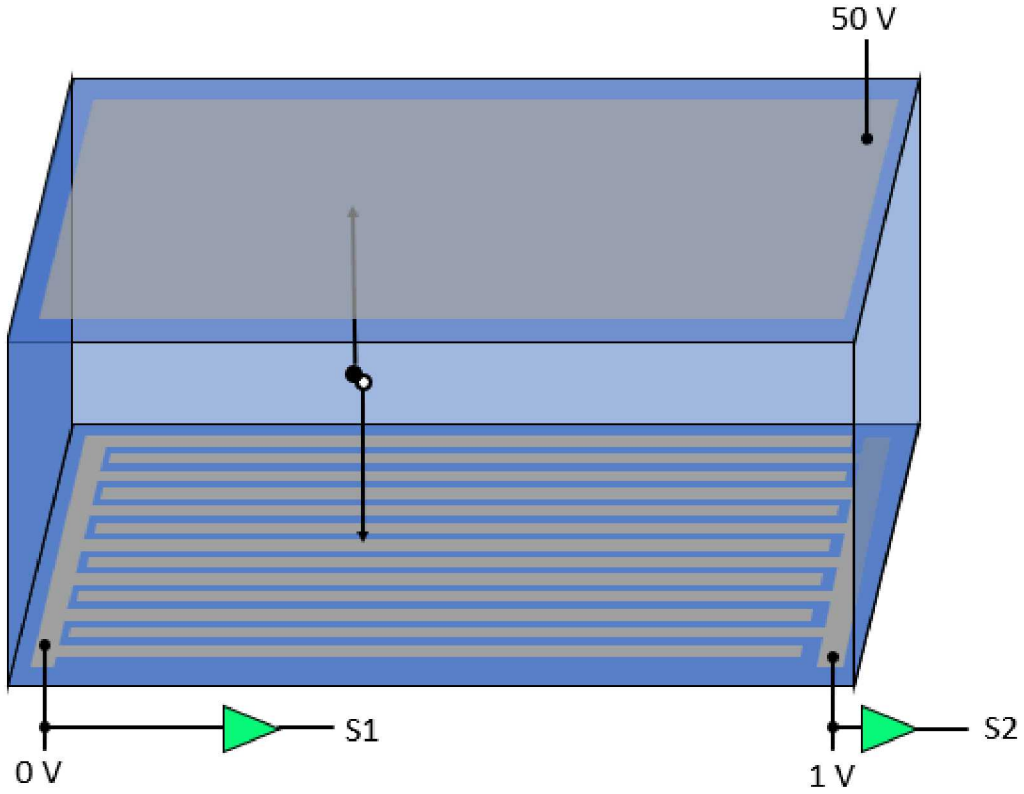
~40% reduction?

Feasibility: significant design risk, better suited to p-type

Other Electrode Configurations: Coplanar Grid

P. Luke, APL 65, p.2884 (1994)





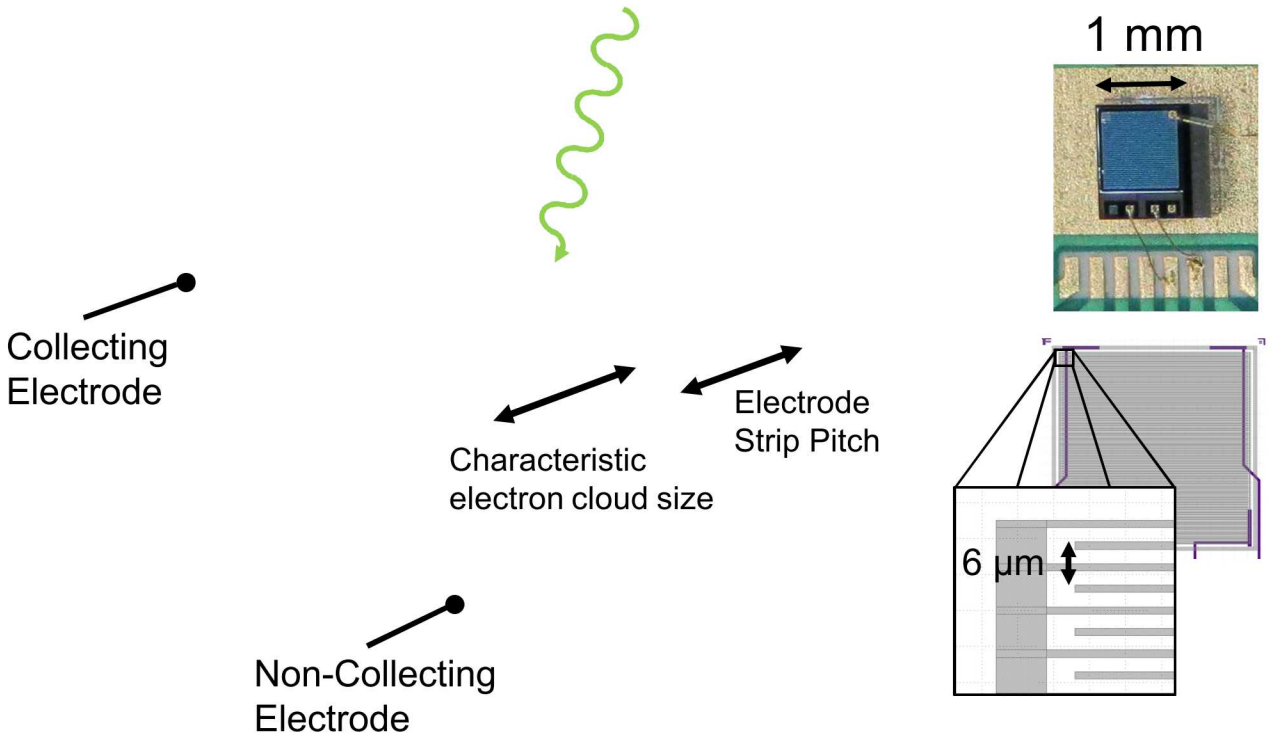
Key Features
-Requires more in-pixel structure
-Can operate as typical pixel when PV=S1+S2
-Can increase dynamic range when PV=S1 . S2 shunted to VRST.
-Can reduce sensitive volume when PV=S1-S2 , similar to point contact
-Unlike point contact, capacitance is higher

~40% reduction?

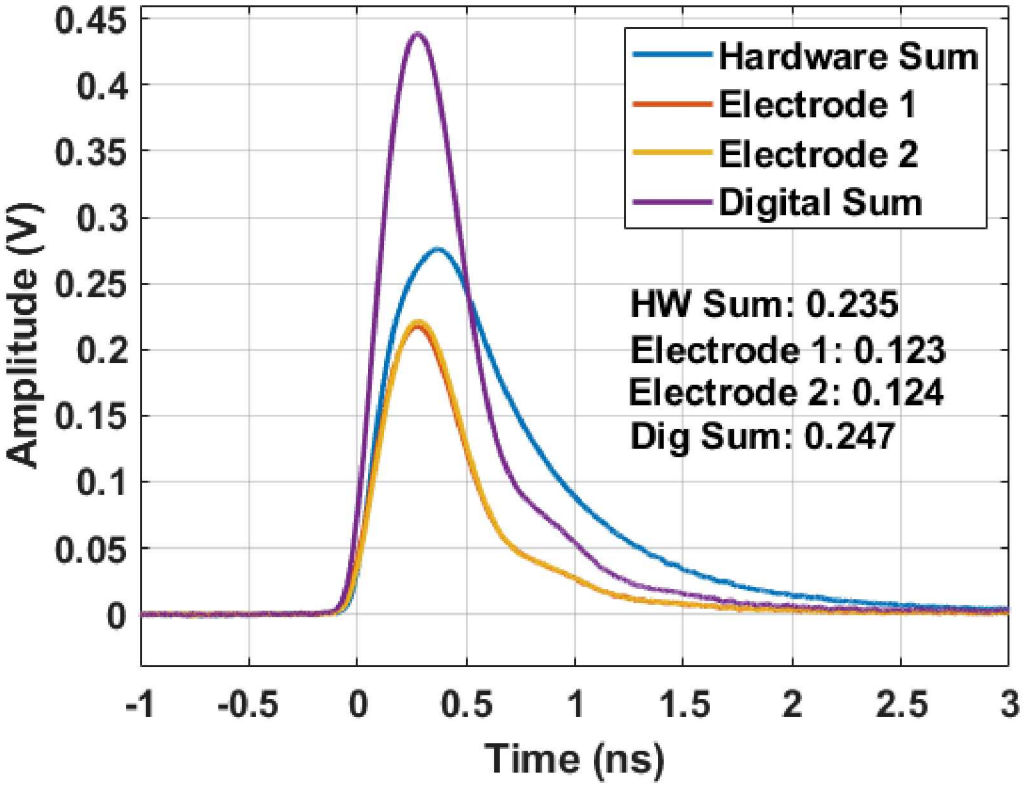
Feasibility: significant design risk, better suited to p-type

Other Electrode Configurations: Coplanar Grid

- Reduce collection area *without increasing shot noise*
- Keep feature size less than characteristic charge carrier cloud size
- Can be recombined to operate as standard pixel

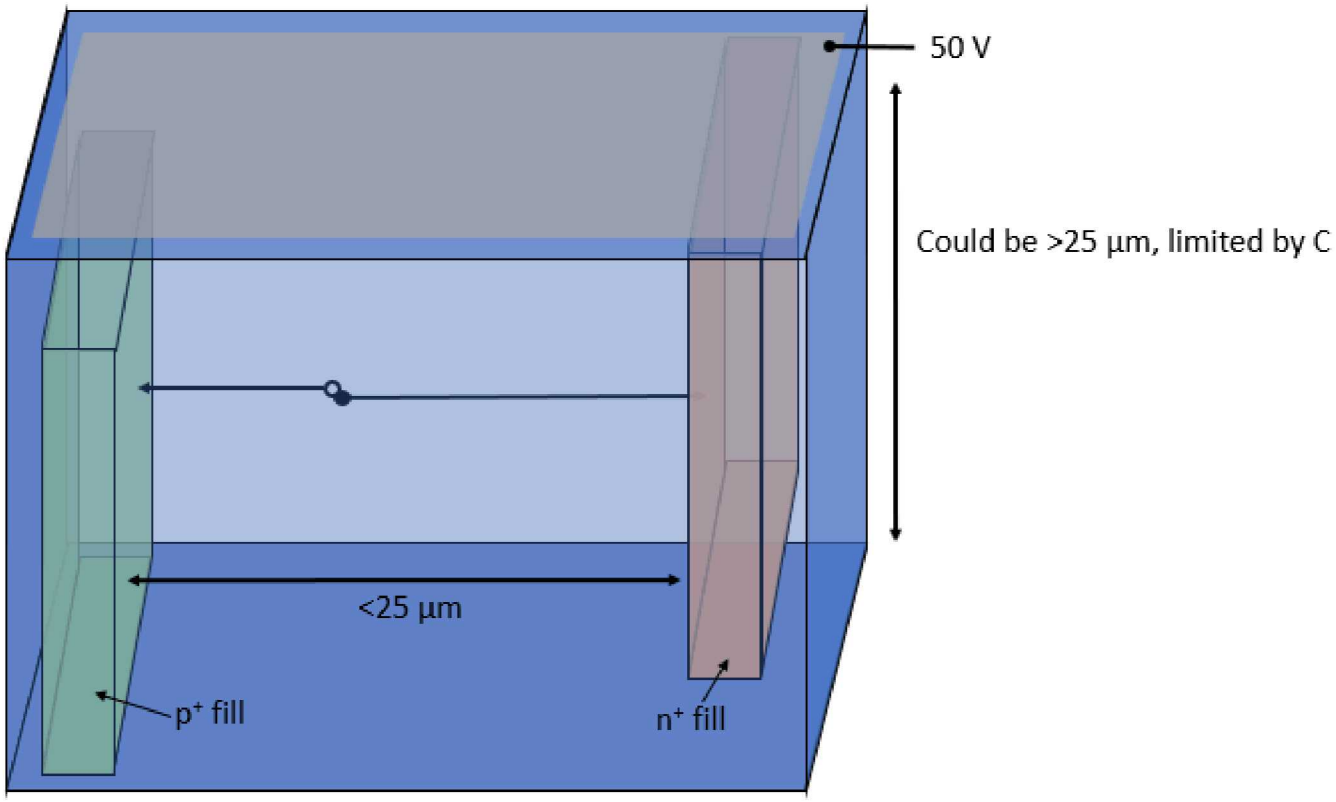


Pulsed laser demonstration of 1 mm CPG detector, current divided by 2



Other Electrode Configurations: 3D Diode (Trench)

Doped polyfill column structures described in Parker 1997, Kenney 1999, Kok 2006, etc.



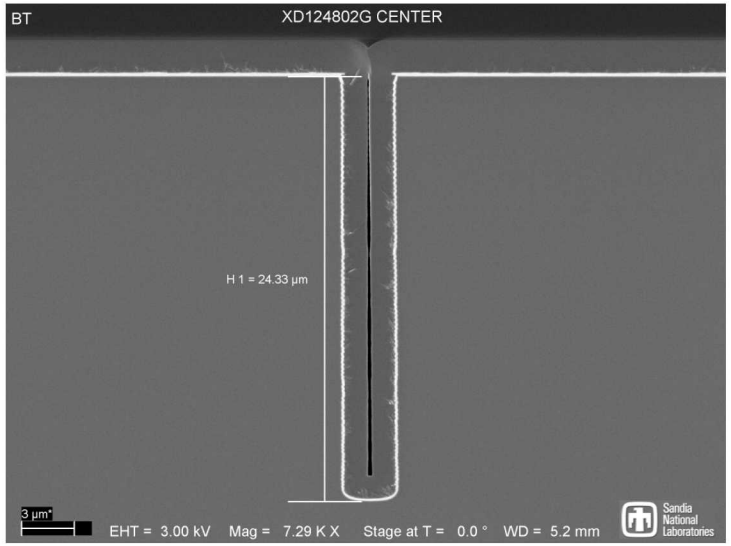
Key Features
-Can select width based on desired timing; may be connected to pixel size
-Thickness can be increased to keep high QE
-Need to develop dry etch and conductive fill process for thick device layers
-2nd electrode would need to be created after hybridization (need low T process)

~50% reduction?

Feasibility: significant process development

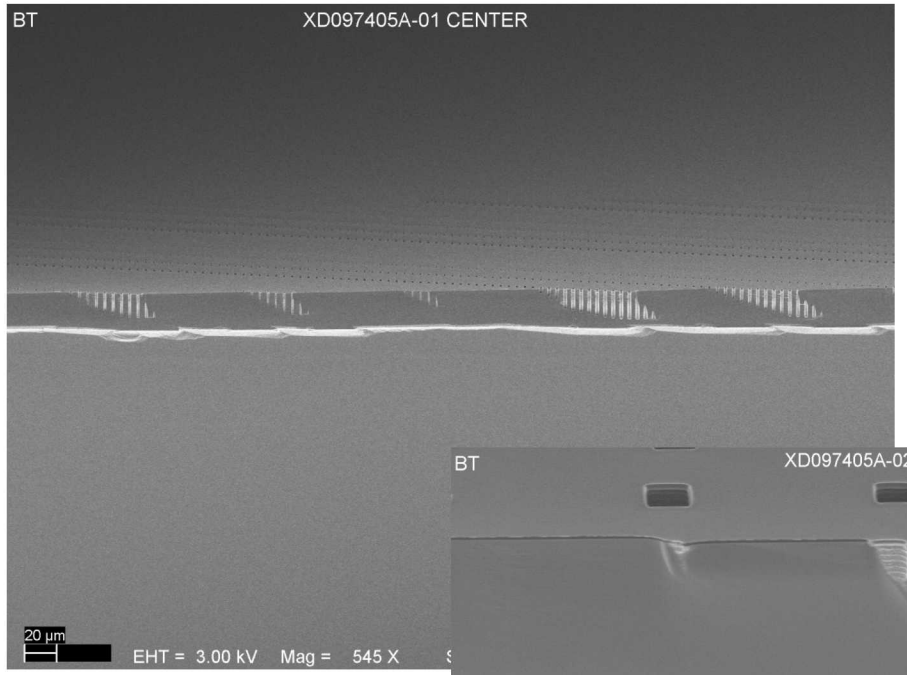
3D Diode (Trench)

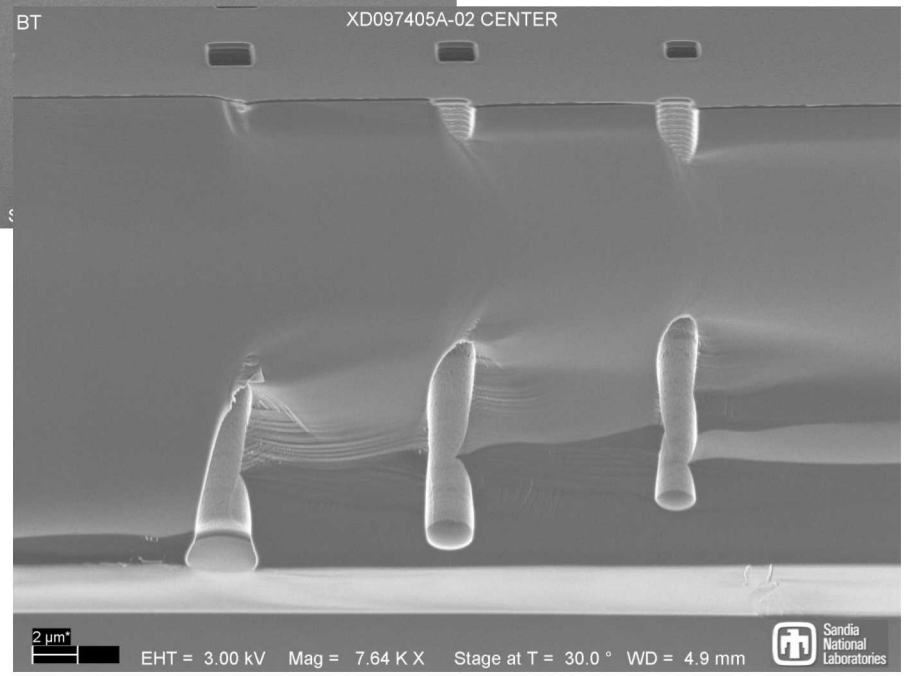
Polysilicon-filled trenches



Poly-filled trench 25 µm deep

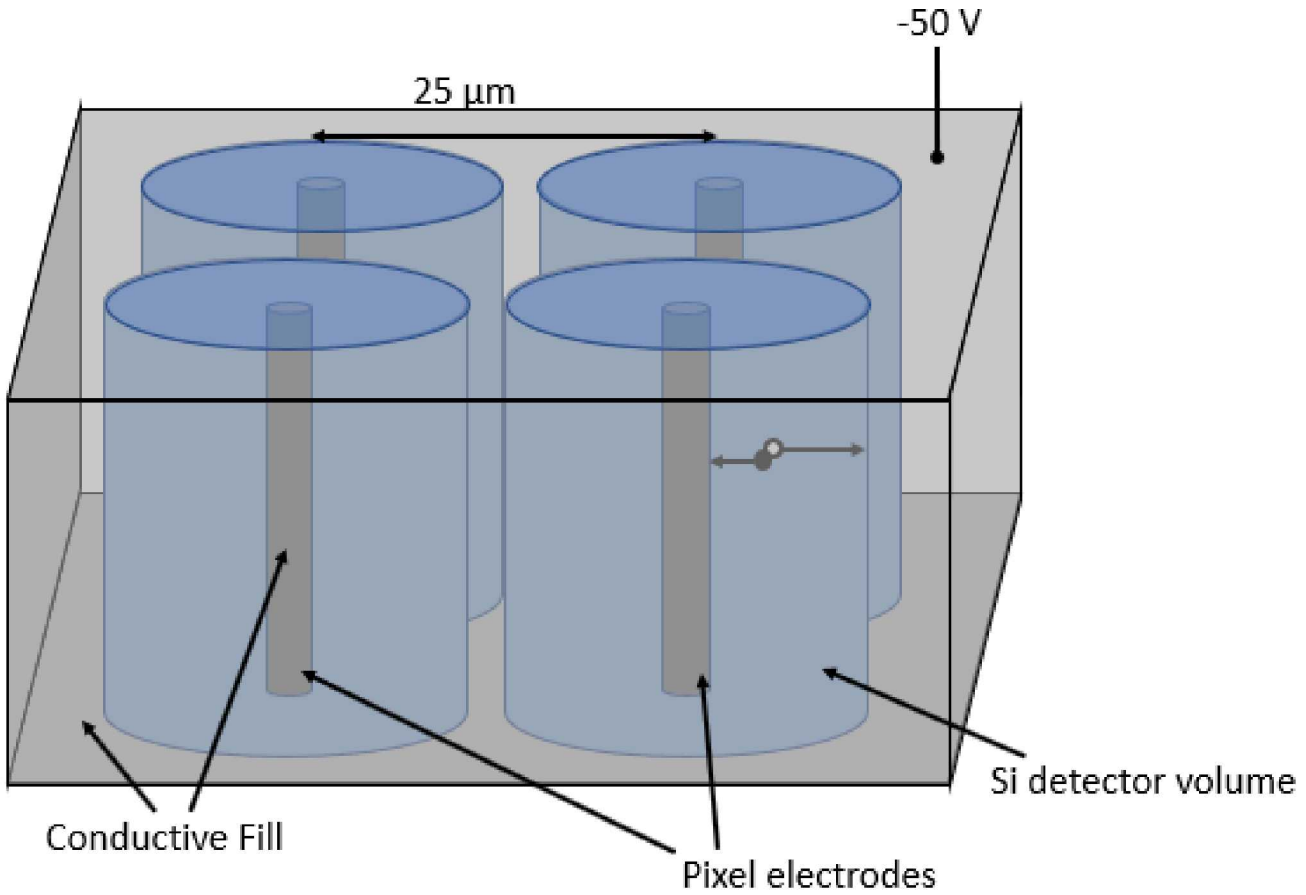
2 µm holes/trenches for W fill





- Key challenge is in assuring good conductance to bottom of trench
- p-n junction ideal, but p+ doping a challenge

Other Electrode Configurations: 3D Diode (Cylinder)



Key Features
-Need mature dry etch and conductive fill process
-Better takes advantage of geometry to reduce hole contribution to signal

~60% reduction?

Feasibility: significant process development

Development Needs

- Funding for wafer purchases
  - 200 mm SOI wafers, n-type and p-type, multiple device layer thicknesses
- Funding for lot starts
  - Need to test concepts in real devices
  - Some concepts require flexibility of a dedicated lot
- Package development
  - Assess maximum applied voltage, path forward to 100V+ PDBIAS
  - Option for thermally sunk package
- Process development for 3D structures

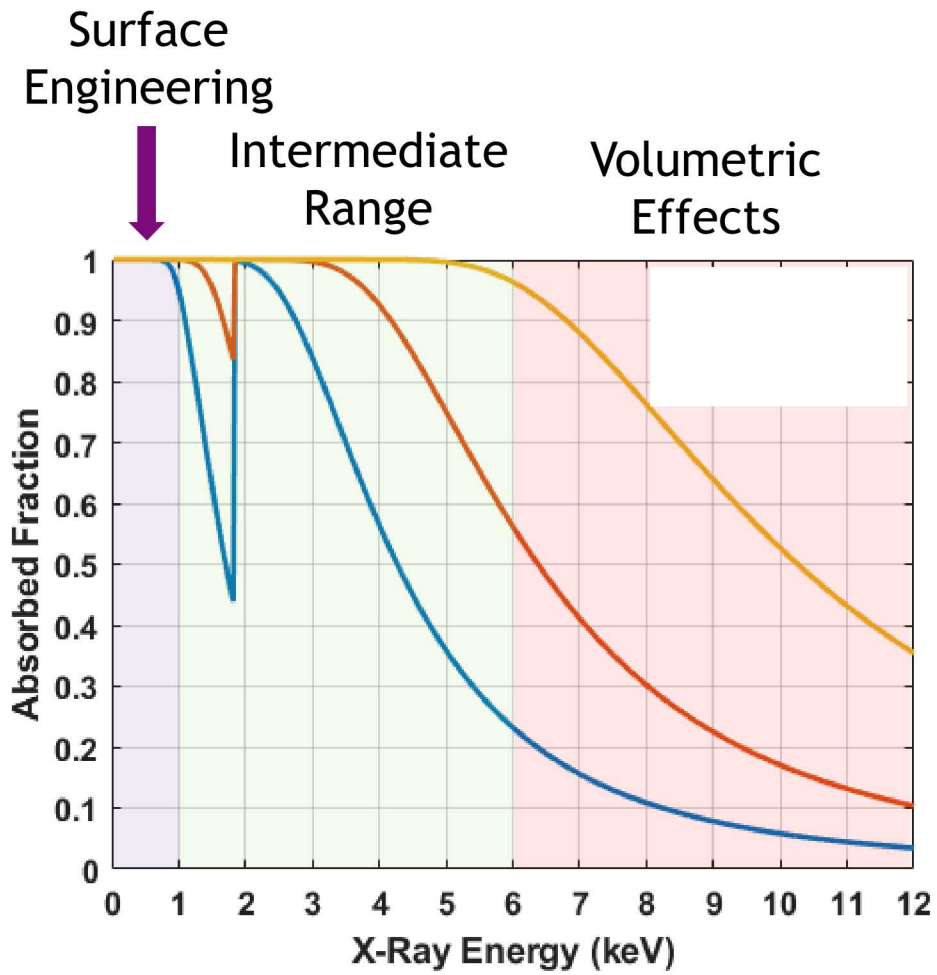
- JPL Superlattice enhancement on Icarus sensors

Detection Efficiency

Our Si Detectors are now capable of sensing a wide range of radiation species and energies

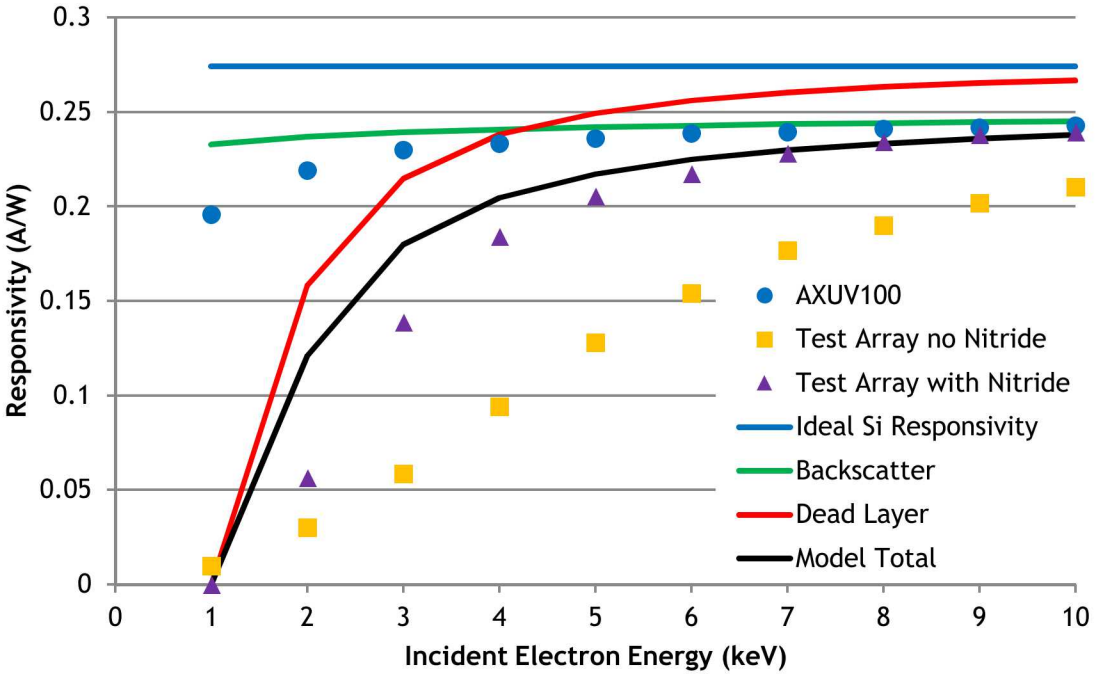
- Original design was optimized for 1-6 keV x-rays
- Detection efficiency for x-rays <1 keV, electrons <10 keV, and light <450 nm dictated by surface conditions
- Detection efficiency for x-rays >6 keV, electrons >20 keV, light >800 nm dictated by volume

- High radiation energy detectors best captured in Michael Wood's discussion

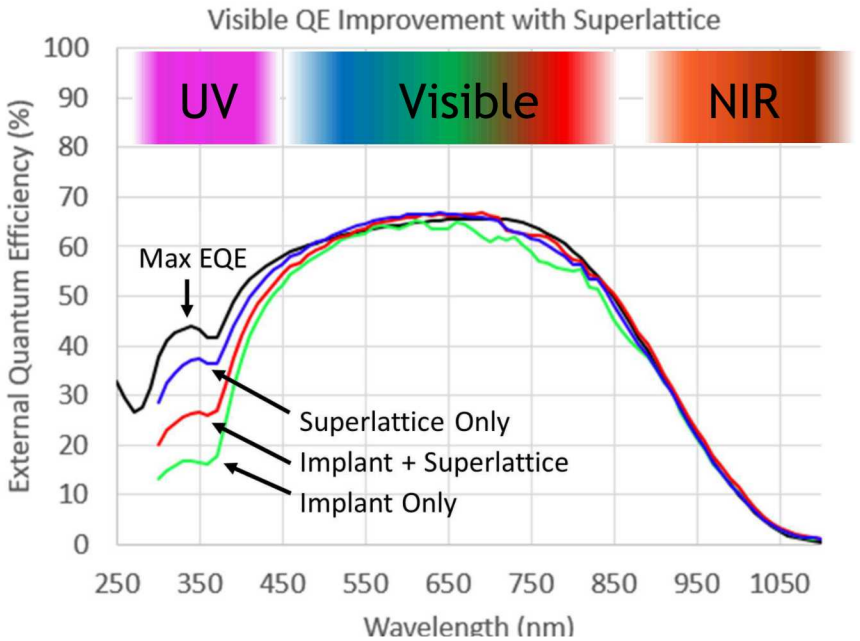


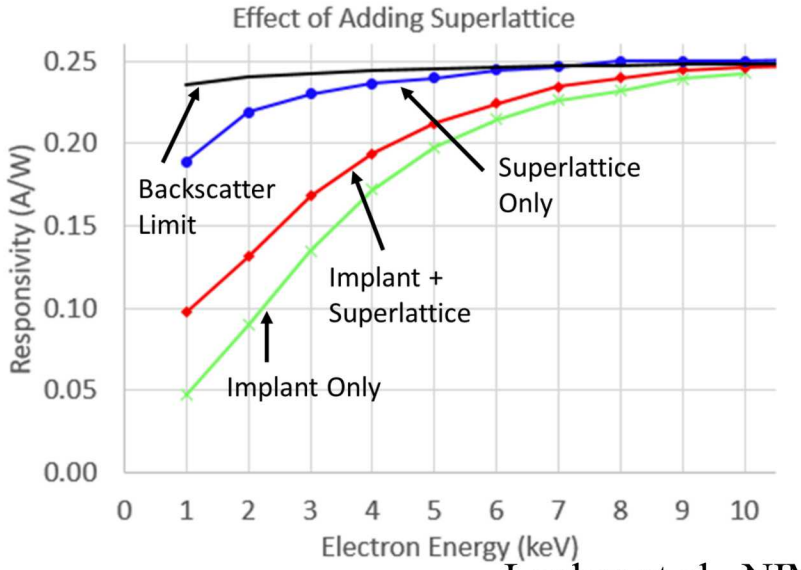
Our Si Detectors are now capable of sensing a wide range of radiation species and energies

- Surface engineering demonstrated increased QE for UV, low-energy electrons
- No inherent disadvantage in higher energy particle detection



Described in Jewell et al., JVSTA (2020)



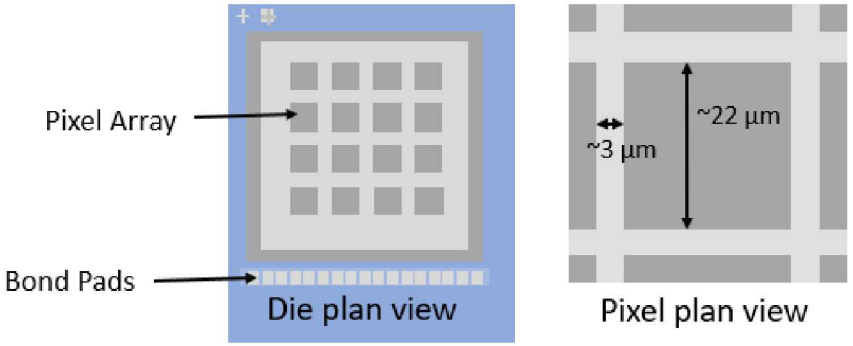


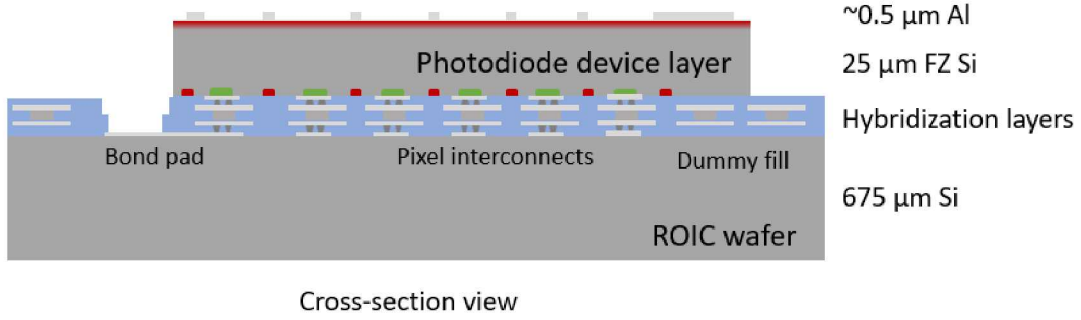
Looker et al., NIM A vol. 916 (2019)

Extra Slides

Today's Pixel Design

Hybrid Device, Die-level

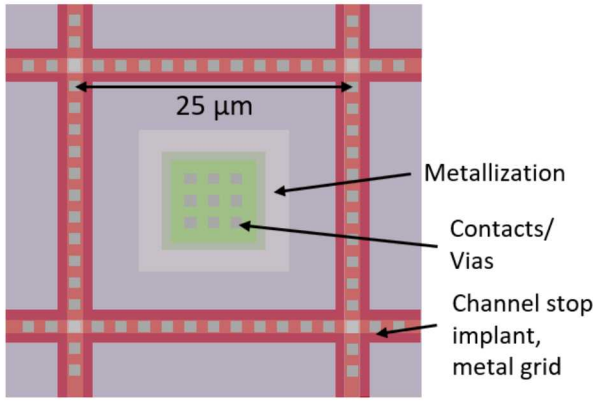




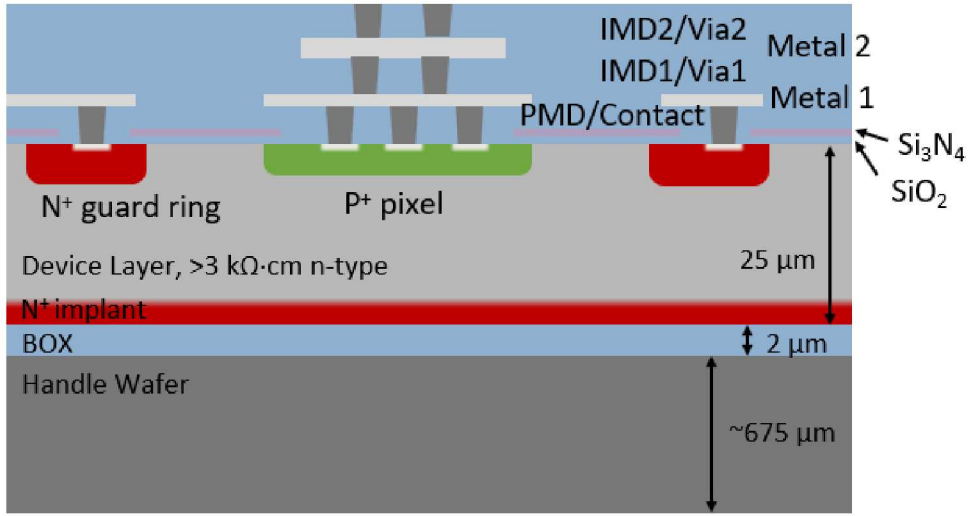
Cross-section view

Detector Wafer, Single-pixel

Pixel Plan View



Cross Section View



Shockley-Ramo Theorem

Key Principle: charge induction efficiency of electrodes can be calculated as a function of volume, independent of real electrostatic conditions

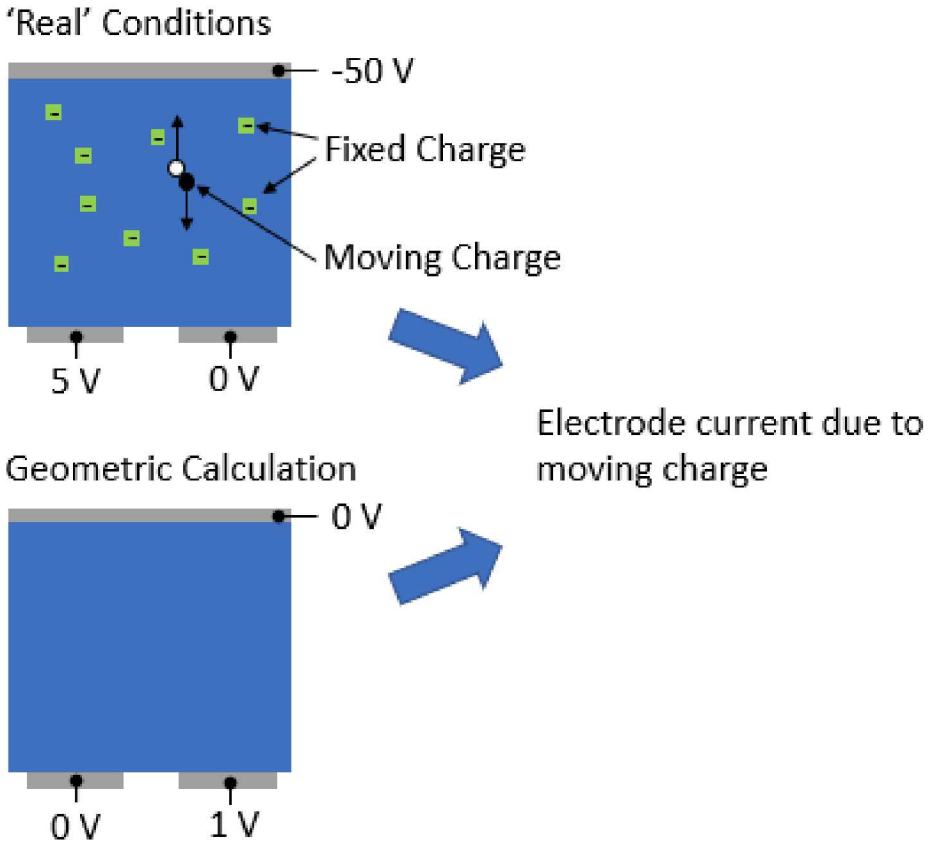
1. Remove all fixed charge
2. Set all electrodes to 0 V
3. Set electrode of interest to 1 V
4. Calculate potential => 'weighting potential' φ_0
5. Calculate E field => 'weighting field' $\overrightarrow{E_0}$
6. The following are true for given geometry:

Charge induced on an electrode $Q = -q\varphi_0$

Current induced on an electrode $i = q\vec{v} \cdot \overrightarrow{E_0}$

From real electric field, we have $\vec{v} = v(|\vec{E}|)\vec{E}$

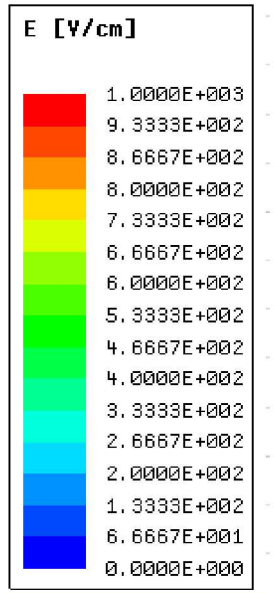
Combination gives $i = qv(|\vec{E}|)\vec{E} \cdot \overrightarrow{E_0}$

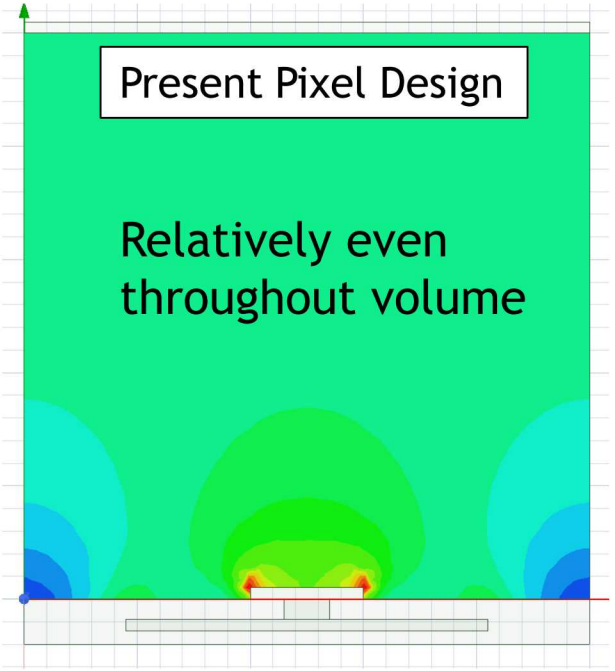


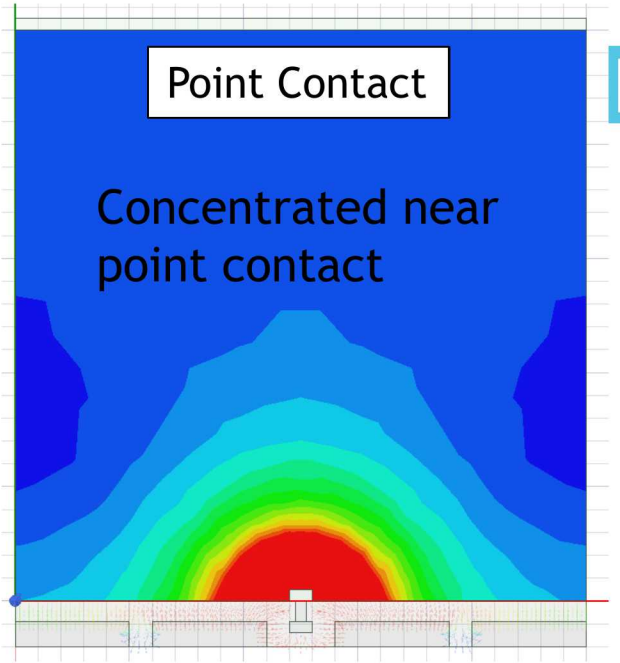
For more information, see Helmuth Spieler's "Semiconductor Detector Systems" Ch. 2 or Zhong He NIMA 463 p. 250 (2001)

Point Contact

Weighting Field $|E_0|$
A measure of sensitivity to moving charge



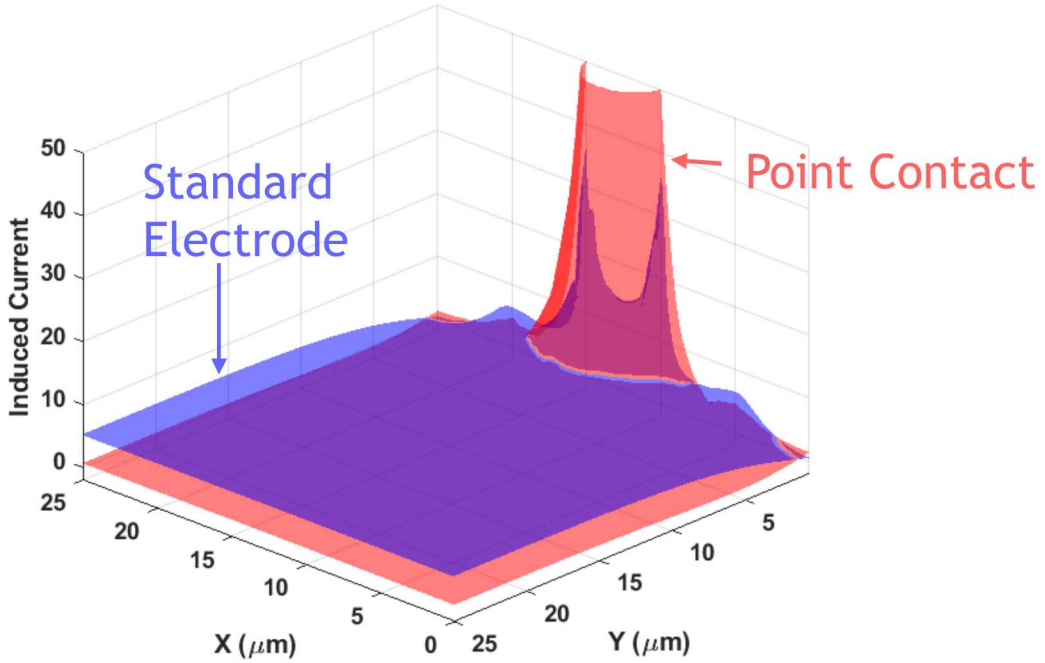




$$i = q\vec{v} \cdot \overrightarrow{E_0}$$

Velocity due to real field

Weighting field



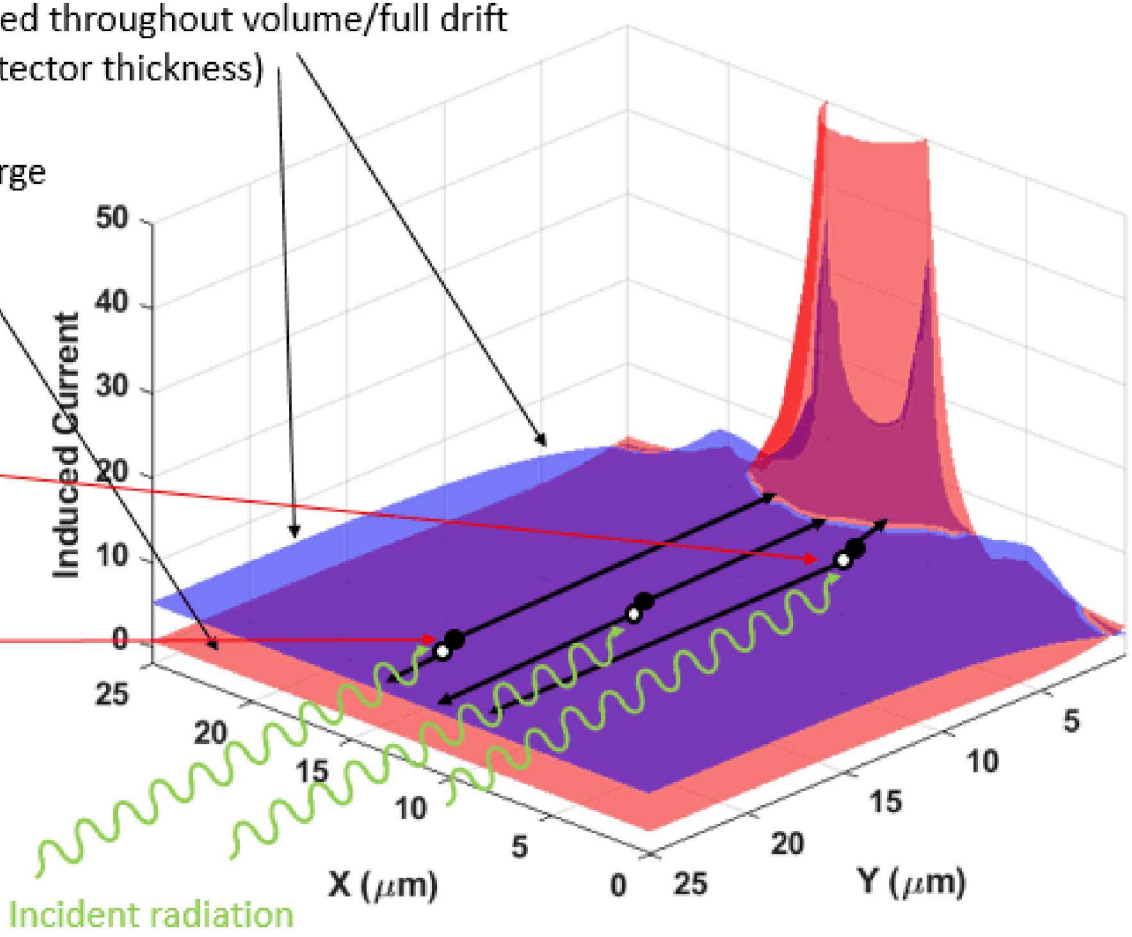
Point Contact

With standard electode, both electrons and holes sensed throughout volume/full drift length (detector thickness)

Point contact does not sense moving charge here; majority of hole drift ignored

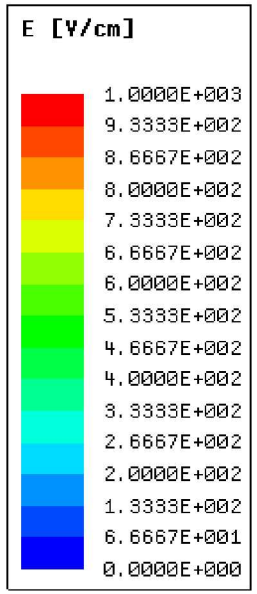
If we sense all moving charge, this case where holes drift much further than electrons is the limiting factor

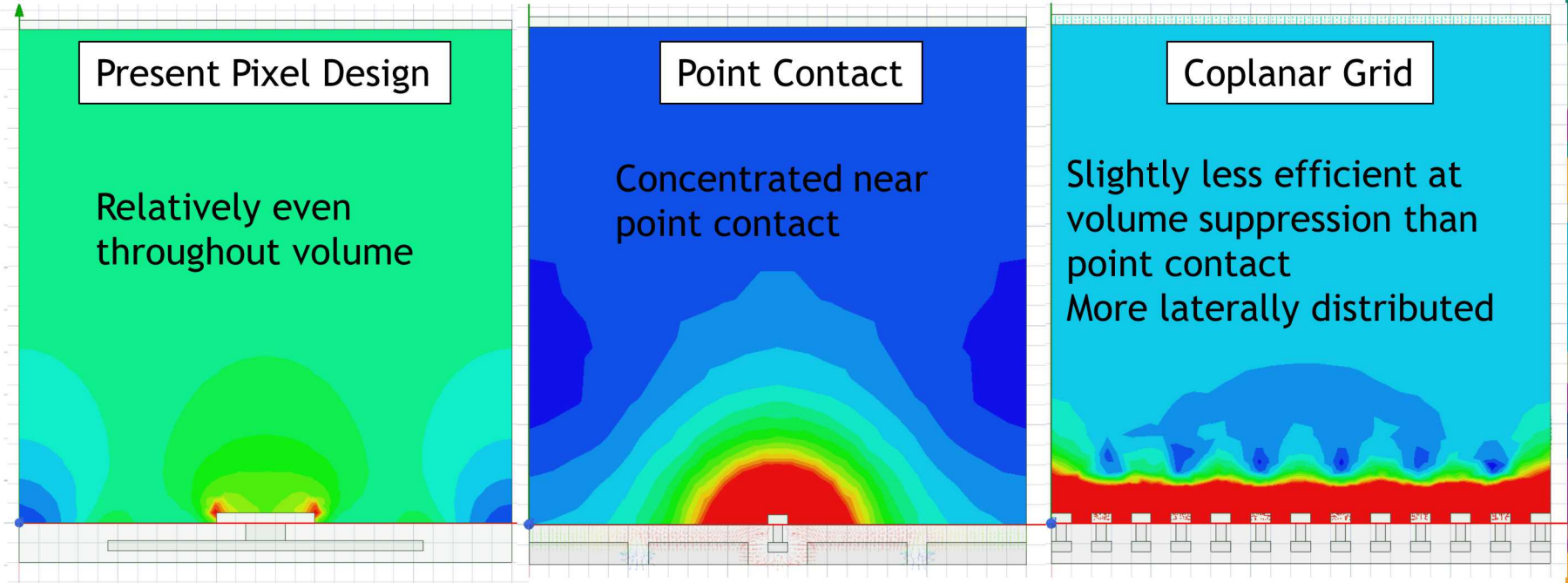
If we ignore hole drift, this case where electrons drift much further than holes is the limiting factor (~2x faster)



Coplanar Grid

Weighting Field $|E_0|$
A measure of sensitivity to moving charge

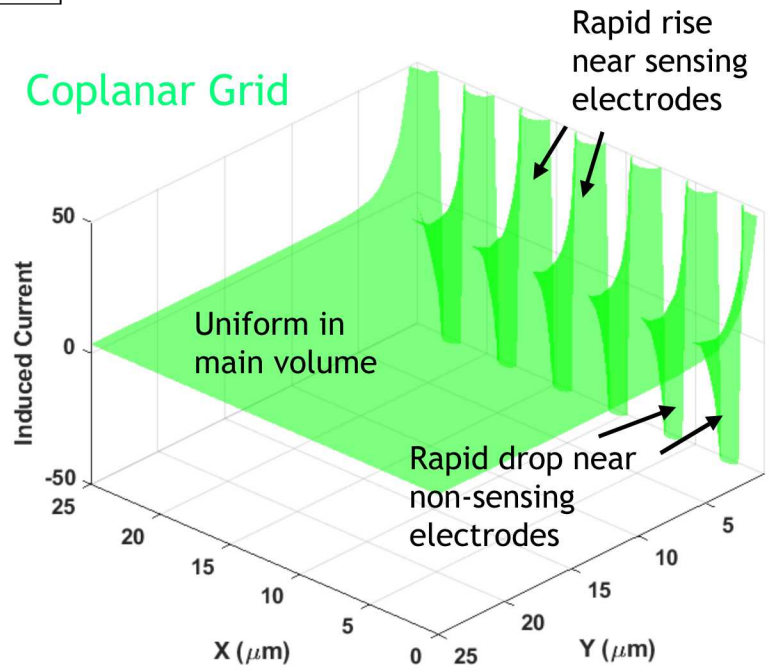


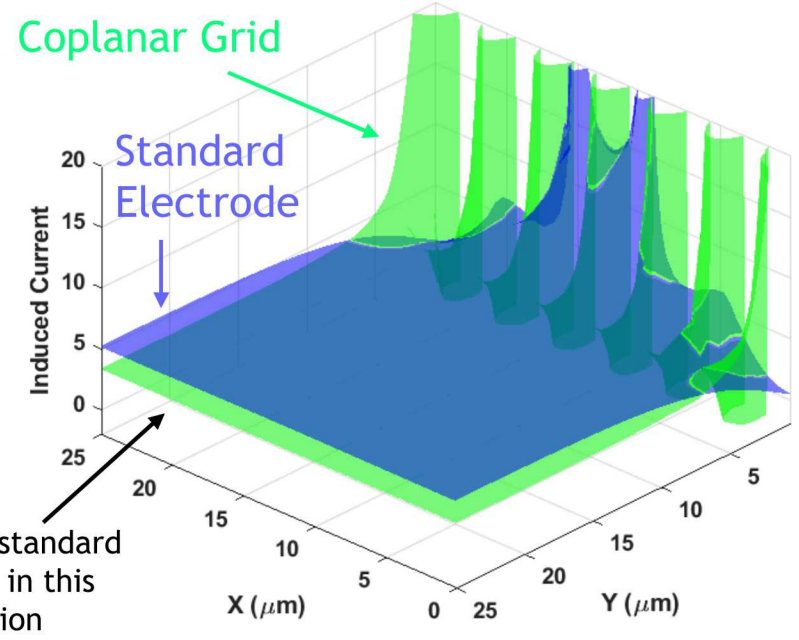


$$i = q\vec{v} \cdot \overrightarrow{E_0}$$

Velocity due to real field

Weighting field

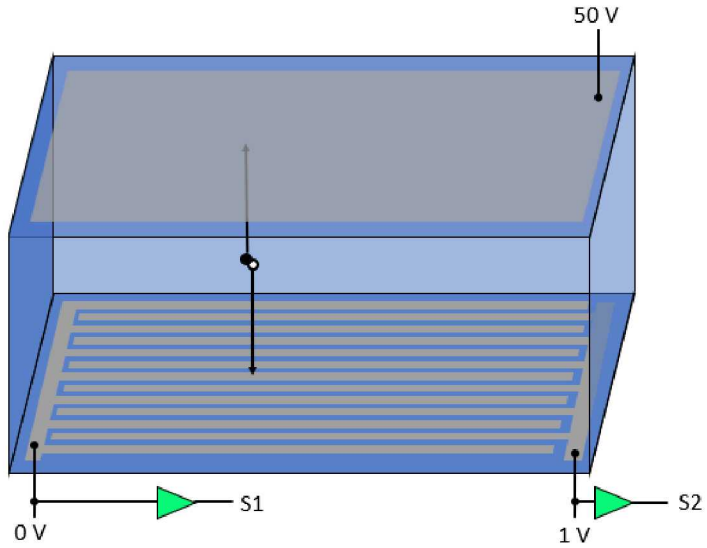


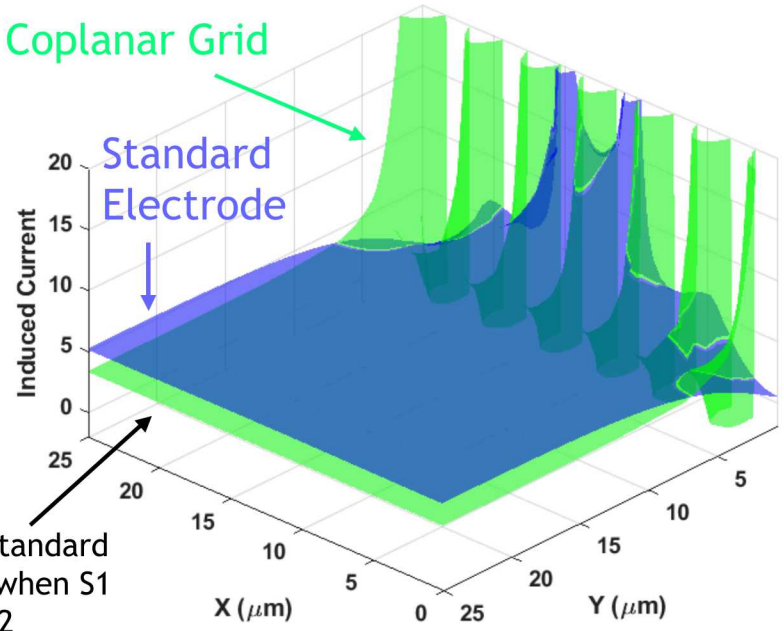


CPG ~1/2 standard sensitivity in this configuration

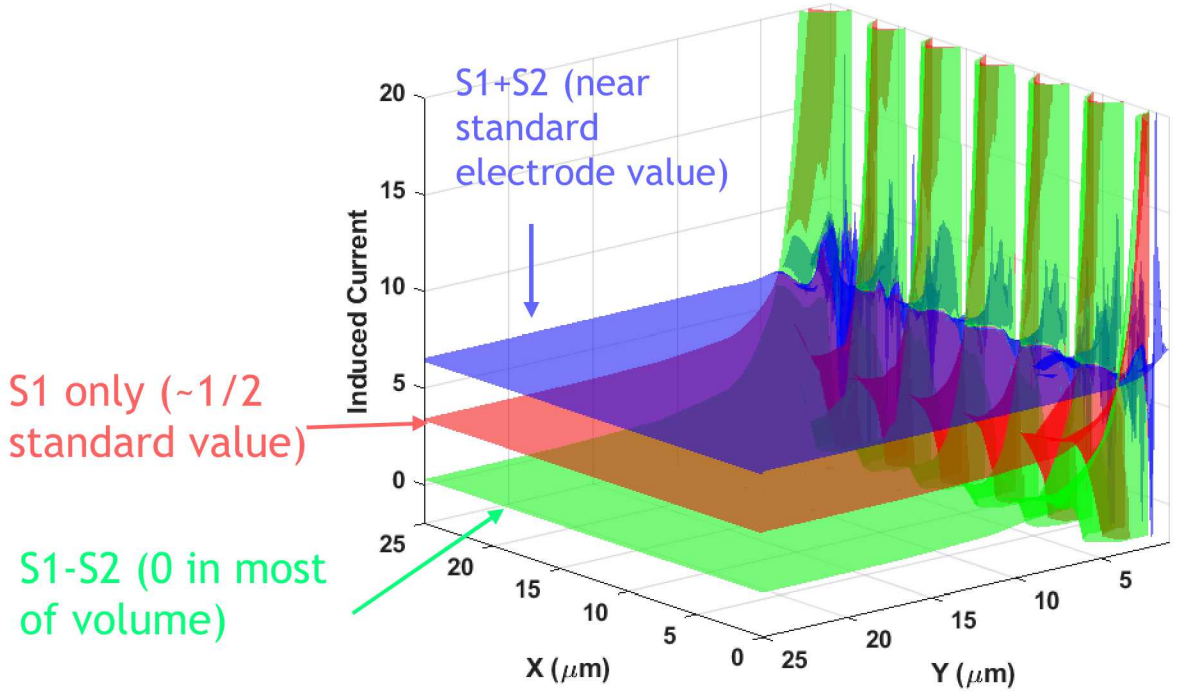
Coplanar Grid

Readout Options

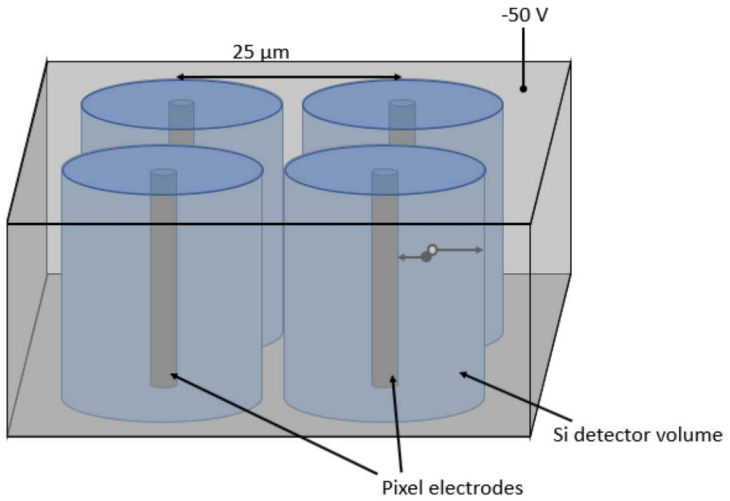




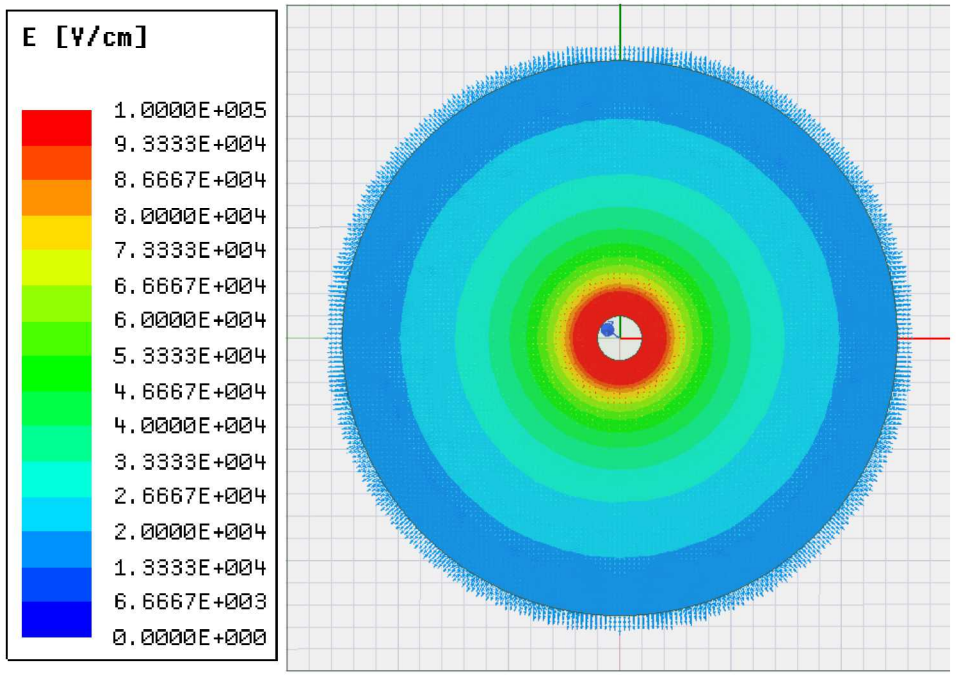
CPG ~1/2 standard sensitivity when S1 read out, S2 shunted to VRST



3D Diode (Cylinder)



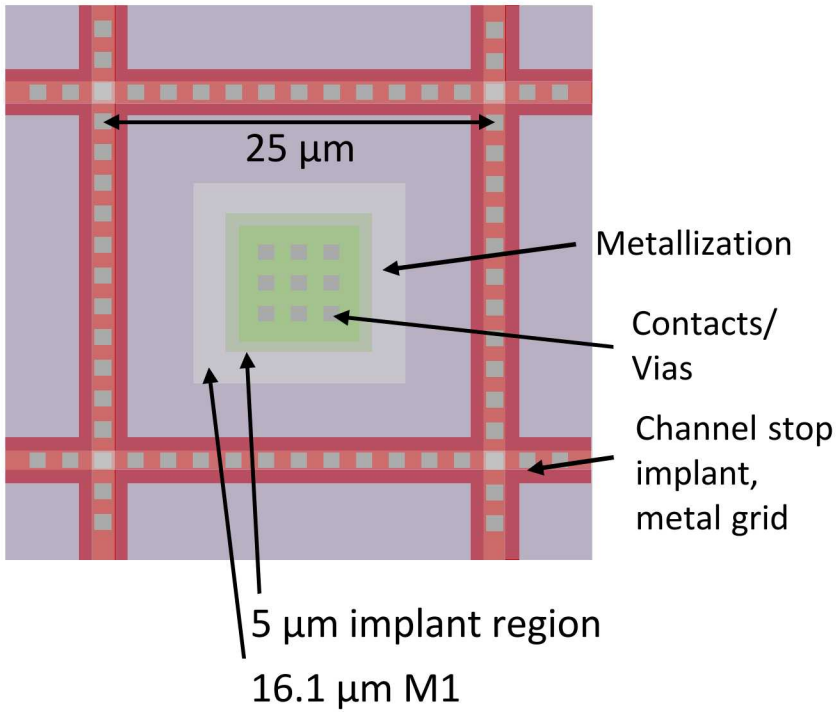
Very high field throughout



Pixel variants

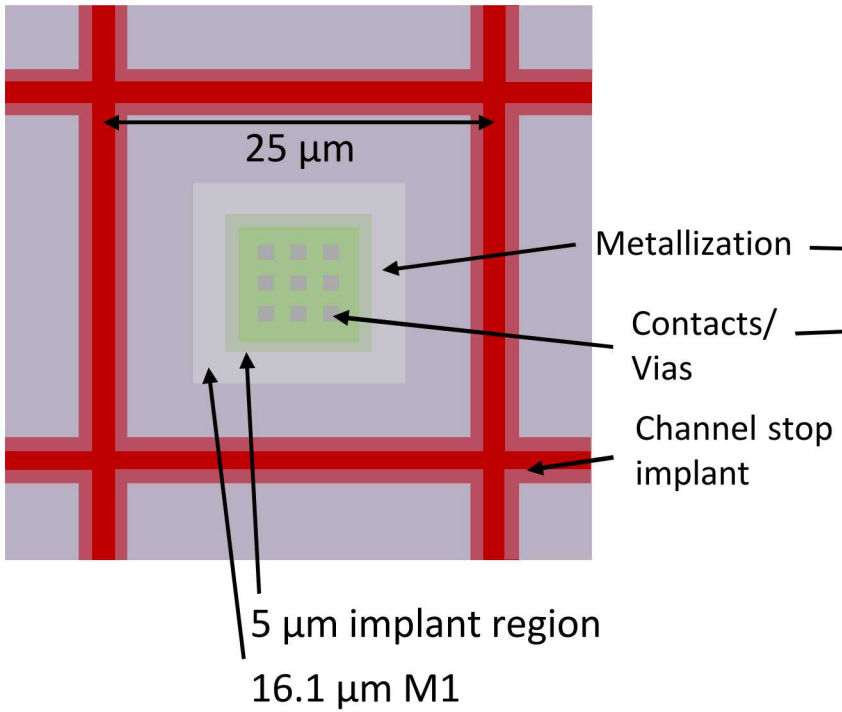
1. Baseline pixel

Exact used by Icarus/Daedalus



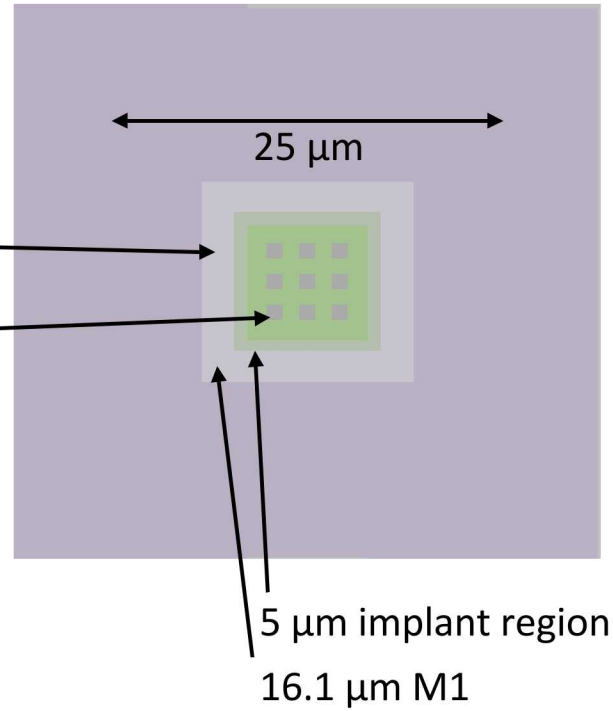
2. No channel stop metal (baseline 2)

Baseline pixel no channel stop metallization



3. No channel stop

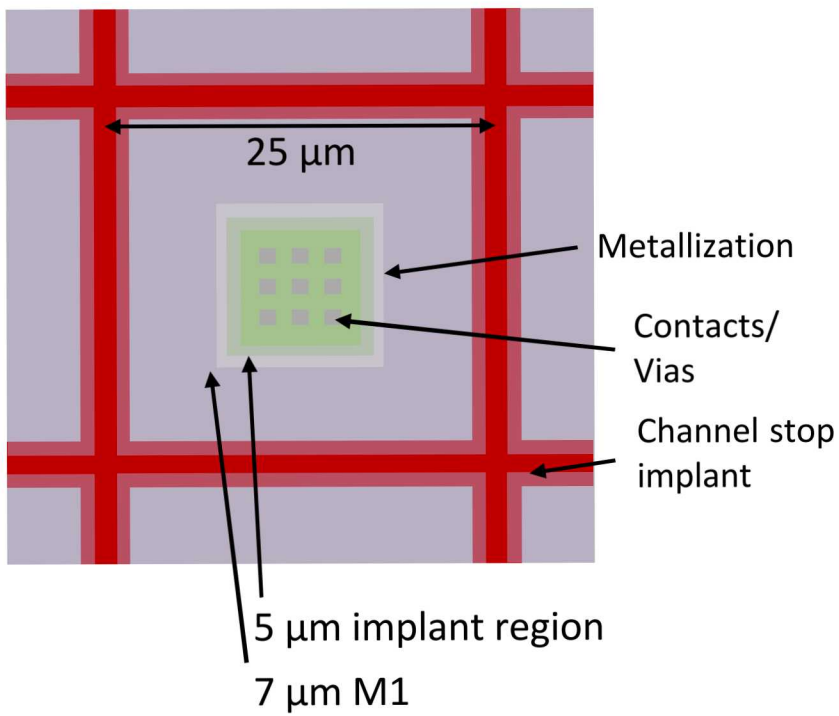
Baseline pixel no channel stop



Pixel variants

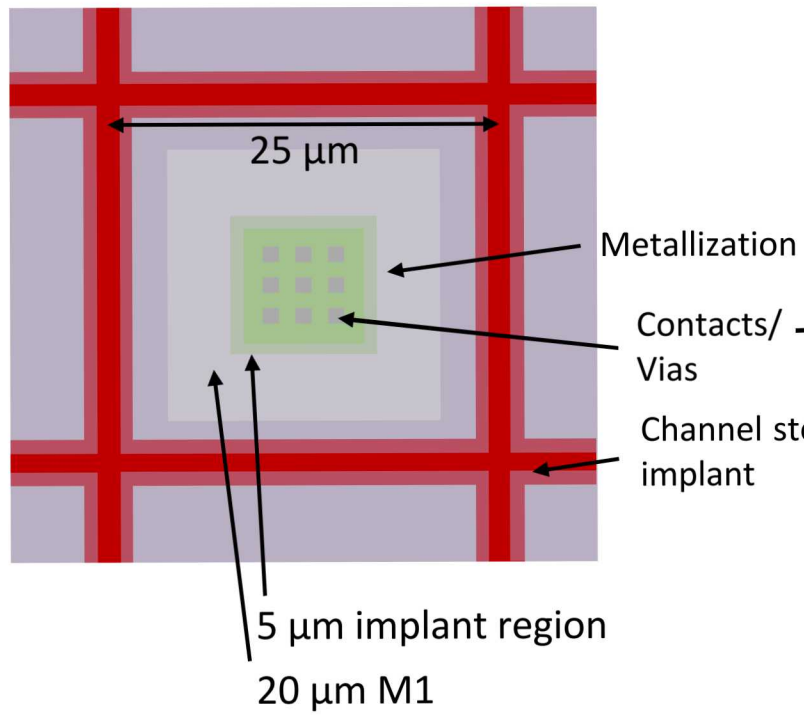
4. Baseline 2 smaller FP

Baseline pixel 2 with smaller field plate



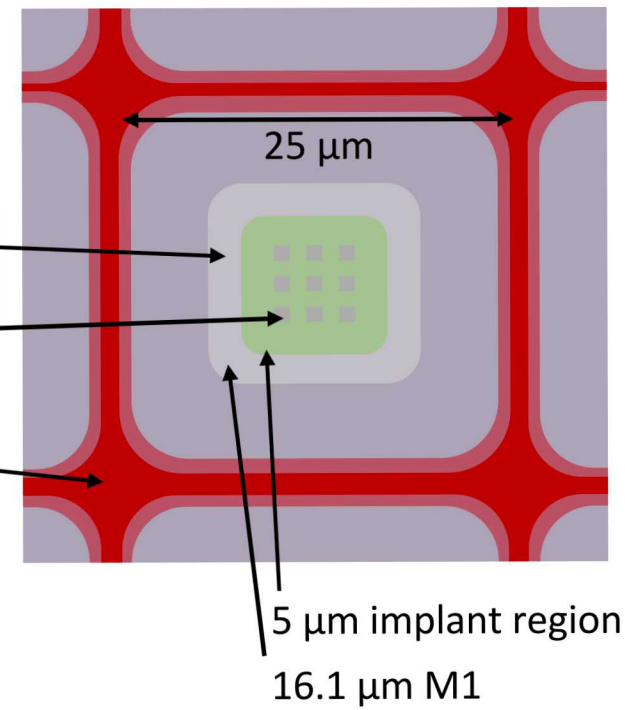
5. Baseline 2 larger FP

Baseline pixel 2 with larger field plate



6. Baseline 2 rounded features

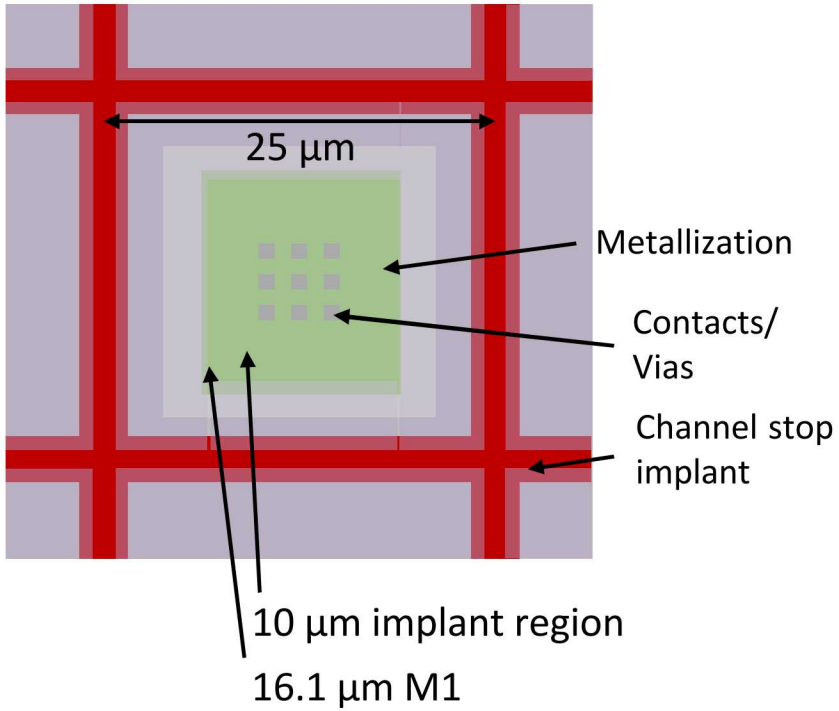
Baseline pixel 2 with rounded features



Pixel variants

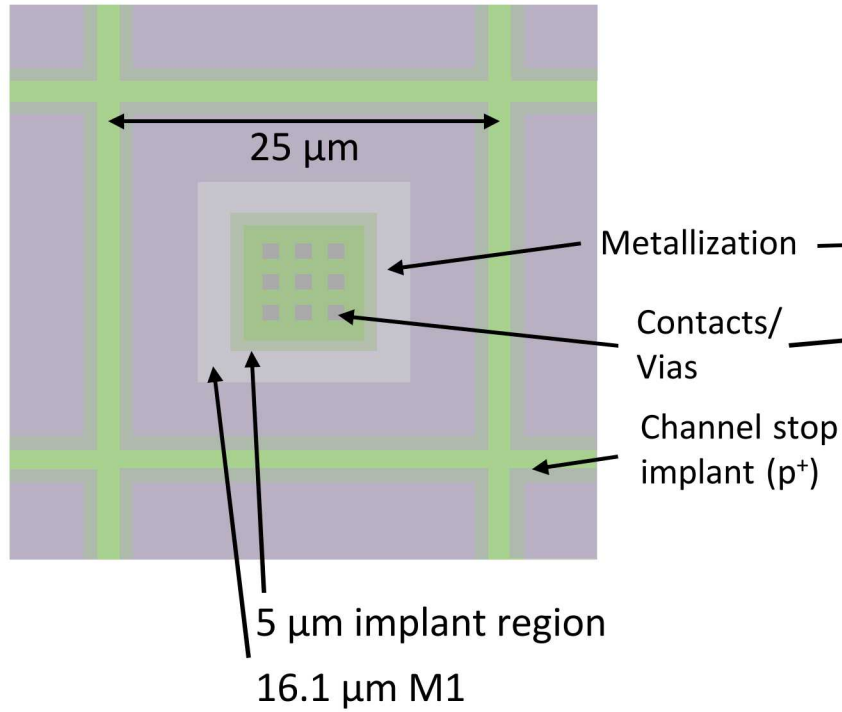
7. Baseline 2 larger implant

Baseline pixel 2 with larger implant region, standard M1 shape



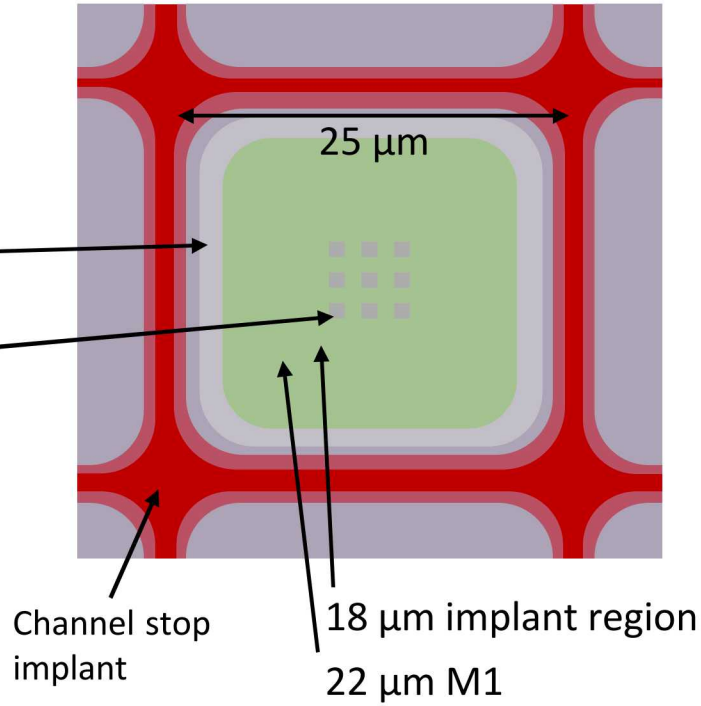
8. Baseline 2 reverse polarity chstop

Baseline pixel 2 with junction channel stop



9. Baseline 2 larger implant

Baseline pixel 2 with larger implant region, larger M1 feature, rounded



Pixel variants

10. Baseline 2 larger implant no chstop

Baseline pixel 2 with larger implant region, larger M1 feature, rounded, no channel stop