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Investigating Heavy Ion Effects on 14nm-Process FinFETs: Displacement Damage Versus Total Ionizing Dose

Madeline G. Esposito[1], *Member, IEEE,* Jack E. Manuel[1], Edward Bielejec[1], Gyorgy Vizkelethy[1], *Member, IEEE*, Jeramy Dickerson[1], *Member, IEEE*, Pranita Kerber[1], Michael P. King[1], *Senior Member, IEEE,* A. Alec Talin[1], David Ashby[1], Michael McLain[1], *Senior Member, IEEE,* Matthew J. Marinella[1], *Senior Member, IEEE*
Aymeric Privat[2], *Student Member, IEEE*, Hugh Barnaby[2], *Fellow, IEEE,* and John Brunhaver[2], *Senior Member, IEEE*

[1]Sandia National Laboratories, Albuquerque, NM
[2]Arizona State University, Tempe, AZ

Abstract – Heavy ion irradiation was examined on a commercial 14-nm n-type FinFET technology to investigate displacement damage and total ionizing dose effects. Low temperature measurements were conducted to reveal underlying physics.

Corresponding (and Presenting) Author:

Madeline G. Esposito, Sandia National Laboratories, 1515 Eubank Blvd SE, MS-1084, Albuquerque, NM 87123, USA, phone: 505-844-0998, email: msciull@sandia.gov

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I. Introduction

Displacement damage (DD) is a nonionizing effect that creates defects in a semiconductor lattice and can result in changes in intended carrier concentration, leakage current, channel resistance, mobility, gain, and more. DD is well studied in minority carrier devices, such as bipolar junction transistors, as it increases recombination current, increasing base current to result in a reduced gain [1]. Majority carrier devices, particularly advanced deep sub-micron MOSFETs, have traditionally been immune to DD, except for heavily irradiated devices [2], [3]. DD studied in silicon diodes has resulted in increased leakage current [4] and results of DD in power MOSFETs include increased on-resistance of the drift region [5]. While FinFETs have been studied for total ionizing dose (TID) effects, DD experiments on FinFETs have yet to be discussed. TID in FinFET devices has been reported to cause subthreshold slope variation, increased leakage current, and threshold voltage shift [6]–[13].

Simulation work by Ni *et al.* [14] studied extended defects in 3-D FinFETs in comparison with 2-D planar MOSFETs and concluded these dislocations in a FinFET are negligible. However, dislocation-induced scattering and other such mechanisms were not included in their model and can be important in simulating FinFET structures. Further simulation work of FinFETs has predicted on-current, or drive current degradation, with an elongated subthreshold slope, as a key trait of displacement damage [15], [16].

Drive current degradation can have serious effects for high-density memory arrays and are a potential concern for terrestrial and cosmic radiation environments. This argument is proposed by Kim *et al.* [15]. If large memory arrays of small FinFET devices experience single neutron strikes over long periods of time, the memory locations will degrade over time, leading to read/write instability, and potentially system failure.

This paper presents data on n-type 14-nm FinFET transistors irradiated with heavy ions. The transistors had varying gate lengths and number of fins. As a result of irradiation, the threshold voltage shifts, subthreshold slope degrades, leakage current increases, and drive current decreases. As the gate length decreases, the drive current degradation effect becomes more severe, indicating the size of the transistor fin is a critical dimension for the observed response in these n-type FinFET devices. Low temperature measurements of these irradiated devices reveal a decrease in transconductance, which is proportional to mobility, for irradiated devices. This decrease in mobility could be a consequence of increased scattering from a disrupted lattice from DD or a trapped charge effect where a local electric field degrades channel mobility from TID. However, a decrease in mobility combined with the observed subthreshold slope elongation suggests that displacement damage is impacting the operation of the device [3], [5], [12]. Increased leakage current and threshold voltage shift are likely results from TID. A TID study will be presented in the final paper to elucidate this assertion.

II. Experimental Set Up

An ion source in conjunction with the 6 MV Tandem accelerator at the Ion Beam Laboratory was used to produce a 42 MeV Si^{7+} beam. The 35 nA (±2 nA) beam was pulsed on target using a pair of precisely timed low- and high-energy beam blankers that pulse the beam via parallel plate electrodes bearing 2.4 kv and 6 kV, respectively. Pulses were limited to ~1 ms with a duty cycle no greater than 20% to mitigate adverse heating effects within the test chip. High fluence irradiations (10^{14} ions/cm^2) required on the order of 10^5 pulses. A constant ion flux of ~$3x10^{11}$ ions/cm^2-s was used.

Simulations using the Monte Carlo program Stopping Range of Ions in Matter (SRIM) [17] indicate on average, 42 MeV Si ions are expected to penetrate between 13.6 and 14.3 μm of the metal and dielectric materials, where the devices reside approximately 10.6 μm beneath slight variations of these materials. From SRIM simulations, the approximate vacancies produced per ion at the device in the stack was found and used to approximate displacements per atom, or DPA. An example of the DPA approximated for a fluence of 10^{12} ions/cm^2 was found to be $6x10^{-5}$. Although 42 MeV Si ions penetrate unnecessarily deep into the test chips, damage produced near the active device depth was expected to be more uniform due to the reduced sensitivity of process variation, individual fin overlayer, and overlayer variation between the two chips tested. During irradiation, the devices were unbiased and kept at room temperature. Electrical measurements were done ex-situ on a probe station using a Keysight B1500 parameter analyzer.

A broad beam of 3 x 3 mm^2 was aimed at the devices. The area of a fin for the smallest effective gate length 14/16 nm is approximately 240 nm^2. At a fluence of 5×10^{11} ion/cm^2, we can estimate 1.2 ion hits per fin, if equally distributed. Table 1 assumes a Poisson distribution to find approximated number of ions per fin for three fluences. For fluences of 5×10^{12} and 1×10^{13}, the Poisson distribution is too broad to list so we only included the expectation value of the number of ions hitting the device.

Two sets of low temperature experiments were conducted; one with liquid nitrogen for a temperature of 77 Kelvin (K) and another with liquid helium for a temperature of 35 K. 82 n-type FinFET devices were tested in this work and come from a standard 14/16-nm process and have a nominal supply voltage

TABLE I
PROBABILITY OF AN ION STRIKING A FIN FOR A GIVEN FLUENCE

Fluence (ions/cm^2)	Probability of an ion striking a fin
5×10^{11}	36% : 0 ions 36%: 1 ion 18%: 2 ions 10%: > 2 ions
1×10^{12}	14% : 0 ions 27%: 1 ion 27%: 2 ions 18%: > 2 ions
5×10^{12}	12 ions per fin
1×10^{13}	24 ions per fin

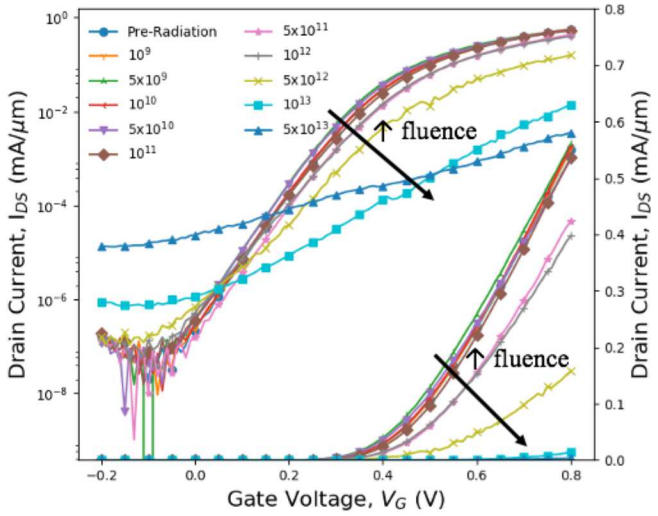

Fig. 1. Example of drain current versus gate voltage curve (I_d vs V_g) for a single fin device with a gate length of 14/16 nm with fluences from 10^9 to 5×10^{13} ions/cm^2.

V_{DD} of 800 mV. It is denoted here as Test Chip, and has four different gate lengths (14 nm, 16 nm, 80 nm, and 200 nm) and different number of fins in each transistor (1, 2, 10, and 40 fins). A Keysight B1500 was used for device measurements. Through repeated experimental error tests, the Keysight B1500 device measurement error was found to be insignificant and correlates to a standard deviation of $\pm 5.2 \times 10^{-4}$ mA/μm. Probing devices is a significant portion of this work. The probing error was found to give a standard deviation of $\pm 1.1 \times 10^{-2}$ mA/μm.

III. EXPERIMENTAL RESULTS

Figure 1 presents an example drain current versus gate voltage (I_{ds} vs V_{gs}) curve of a single fin device with an effective 14 nm gate length for both log and linear scales. Figure 1 demonstrates the result of the wide range of fluence levels tested. At lower fluence levels ranging from ~10^9 to 10^{11} ions/cm^2, the statistical probability of 1 ion hit per fin is small. However, small shifts in the threshold voltage and current degradation is still observed. These device effects become more pronounced with higher fluences. Drive current degradation, threshold voltage shift, increased leakage current, and decreased subthreshold slope are all observed as a result. These four observations were predicted through simulation work as a result of displacement damage in FinFETs by Kim *et al.* [15]. These changes in the device operation were observed on all 82 transistors tested.

To better understand the drain current degradation, the drive current is examined in Figure 2. Here the drive current is defined as the maximum drain current where the gate voltage is equal to the drain voltage. For these devices, this drive current occurs in saturation at $V_{DS} = V_{GS} = 800$ mV. Figure 2 (a) illustrates the drive current as a function of fluence with varied gate length. Figure 2 (b) shows the change in drive current from the devices shown in Fig. 2 (a) to display how the change in fluence results in a change in the drive current. In Fig. 2 (b), a factor in drive current degradation is the gate length rather than

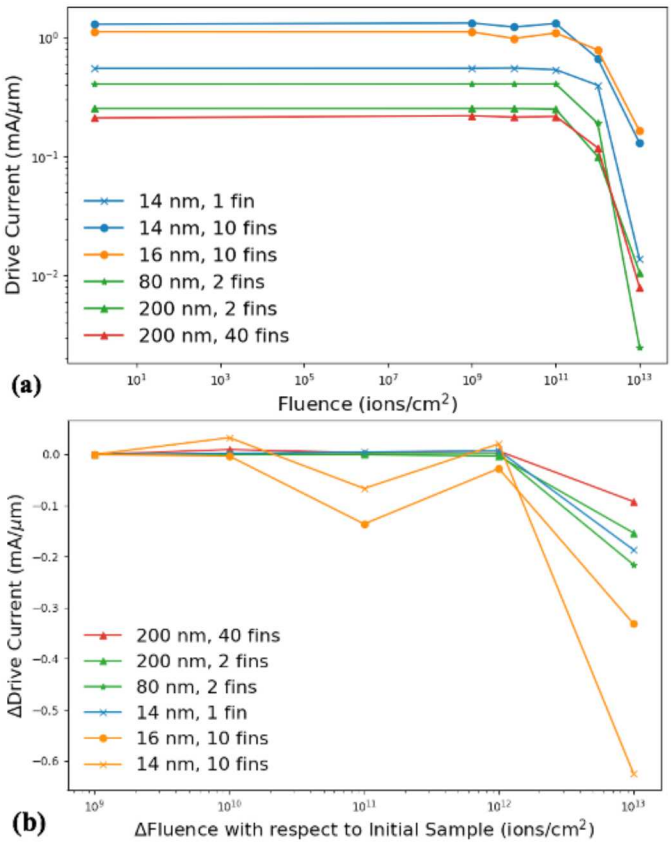

Fig. 2. (a) Drive current versus fluence for each device tested organized by gate length. (b) The change in drive current with respect to change in fluence.

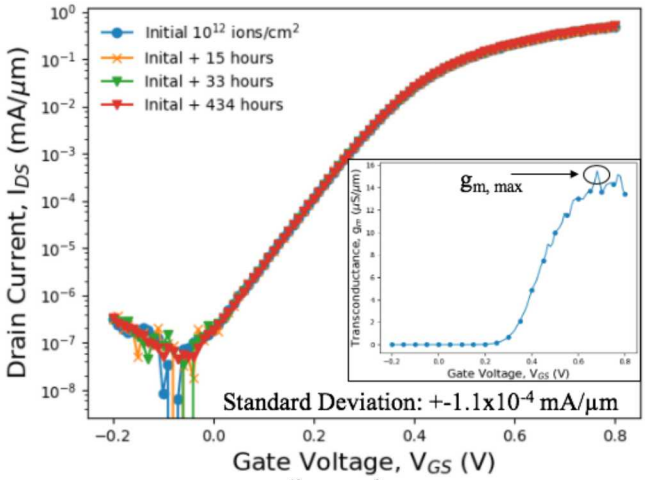

Fig. 3. An irradiated device of 10^{12} ions/cm^2 measured hours after exposure. These devices were kept unbiased and at room temperature in between measurements.

the number of fins. For shorter gate lengths, drive current degradation is greater than for longer channel devices.

These devices were also checked for annealing. Between measurements, the devices were kept unbiased and at room temperature. An irradiated sample at 10^{12} ions/cm^2 was measured three times; 15 hours post-irradiation, 33 hours post-irradiation, and 20 days, or 434 hours after irradiation. This data

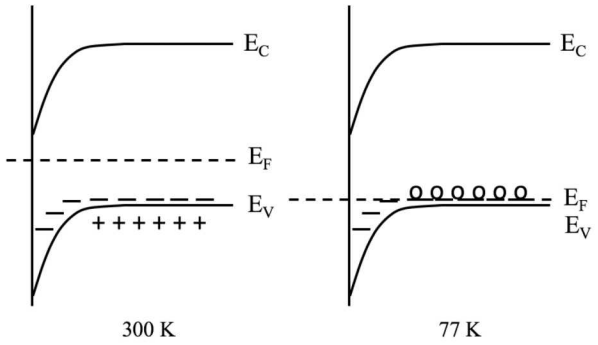

Fig. 4. Energy band diagram of a MOSFET at room temperature, 300 K, and at 77 K, redrawn from Ref [18].

is shown in Figure 3 where the standard deviation is within measurement error, demonstrating no room temperature annealing occurs on the time scales considered in this work.

IV. DISCUSSION AND ANALYSIS

At room temperature, shallow defects are thermally ionized. However, lower temperatures will freeze-out holes in the bulk. Yet in the surface depletion region these shallow defects remain ionized due to band bending from the built-in and applied potentials. This is depicted in Figure 4 and is redrawn and summarized from Ref [18]. At 77 K and temperatures below this, the mean free path increases as phonon scattering decreases, leaving ionized impurity scattering as the dominant mechanism that limits carrier mobility [18], [19]. At lower temperatures, MOSFET devices have noticeably higher mobility, lower leakage current, increased threshold voltage, and improved subthreshold slope [18]–[20].

Low temperature measurements were conducted with four different samples of Test Chip; an unirradiated sample and samples with fluences of 10^{12}, 3×10^{12}, and 5×10^{13} ions/cm^2. The drive current at 35 K was divided by the drive current at room temperature to observe quantitative differences in drive current relative to nominal device operation. This drive current ratio and a ratio of 77 K divided by 300 K are presented in Figure 5. It is noticeable that drive current increases as temperature decreased for the unirradiated sample. However, the ratio decreases as the fluence increases.

This work also examines the transconductance to extract the mobility of irradiated devices. If displacement damage is present, the mobility should decrease due to an increased scattering from a disrupted lattice. Transconductance, g_m, can be solved at a low drain bias and at a high drain bias to extract mobility. Both will be examined here to ensure accuracy in this claim. Transconductance for low drain voltage is presented in Equation 1 where transconductance for large drain voltage is presented in Equation 2 [19].

$$g_m = \left.\frac{\partial I_{DS}}{\partial V_G}\right|_{V_{DS}=\text{constant}} = \mu \frac{\epsilon_{ox}\epsilon_o}{t_{ox}} \frac{W}{L} V_{DS} \quad (1)$$

$$g_m = \left.\frac{\partial I_{DS}}{\partial V_G}\right|_{V_{DS}=\text{constant}} = \mu_{eff} \frac{\epsilon_{ox}\epsilon_o}{t_{ox}} \frac{W}{L} (V_G - V_T) \quad (2)$$

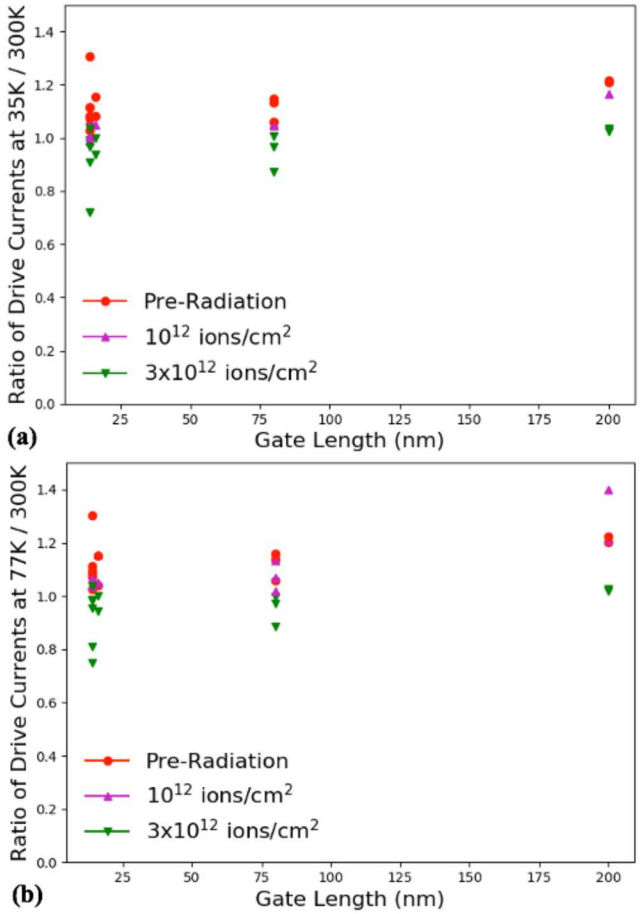

Fig. 5. Ratio of temperature dependent drive current with respect to gate length. (a) The drive current at 35 K divided by the drive current at 300 K. (b) The drive current at 77 K divided by the drive current at 300 K.

Transconductance for small drain voltage is proportional to the carrier mobility, μ, at the semiconductor surface. The transconductance for large drain voltages is proportional to the effective surface mobility, μ_{eff}. From the I_{ds} vs V_{gs} curves, shown in Fig. 1, the transconductance was found by taking the derivative of the current with respect to bias. This is shown in the inset of Fig. 3. The maximum transconductance value was extracted and used for comparison in Fig. 6. Figure 6 presents the ratio of transconductance at 35 K divided by the transconductance at 300 K where Fig. 6a is for a high drain bias (V_{ds} = 800 mV) and 6b is for a low drain bias (V_{ds} = 50 mV). This ratio is larger than 1 for unirradiated devices as expected [18], [19]. However, this ratio degraded with irradiation, providing evidence of a scattering mechanism that cannot be frozen-out which is degrading mobility. We claim this scattering mechanism is due to a disruption of the lattice caused by the heavy-ion bombardment during irradiation. While the data suggest that the heavy ions are inducing DD effects, we recognize that a substantial ionizing dose is also being deposited during the irradiations. Thus, it is possible that the observed effects may be attributable to a TID mechanism such as radiation-induced short channel effects [13]. In the final paper, results of TID experiments at ultra-high doses will be presented to further investigate DD and TID effects in this

FinFET technology. To further characterize the effects of irradiation on the device behavior, and help reveal the role of interface traps, we will carry out noise measurement as a function of fluence. These results will also be presented in the final paper.

In addition to experimental work, 3-D finite-element simulations have been performed in Silvaco's TCAD suite of tools. A 3-D 14/16-nm FinFET was constructed to match a PDK data set. To investigate the observed radiation response, lattice dislocation defects were inserted at various locations in the device. Preliminary simulation results have produced matching qualitative behavior of the experiments discussed earlier: drive current degradation, threshold shift, and subthreshold slope degradation. We will present these results in the final paper. We also plan to have simulation results of TID effects as well to further compare the difference between TID and DD in this FinFET technology node.

V. CONCLUSION

Heavy ion irradiation of n-type 14/16-nm process FinFET transistors has been studied where we report changes in the threshold voltage, subthreshold slope, drive current, and leakage current. As the gate length of the FinFET decreases, the degradation effects became worse. Low temperature measurements were conducted to verify mobility degradation due to an increase in scattering from radiation-induced disorder in the silicon lattice. Decreased mobility with an elongated or stretched-out subthreshold slope are the dominate responses of heavy ion testing and point to displacement damage as the primary degradation mechanism.

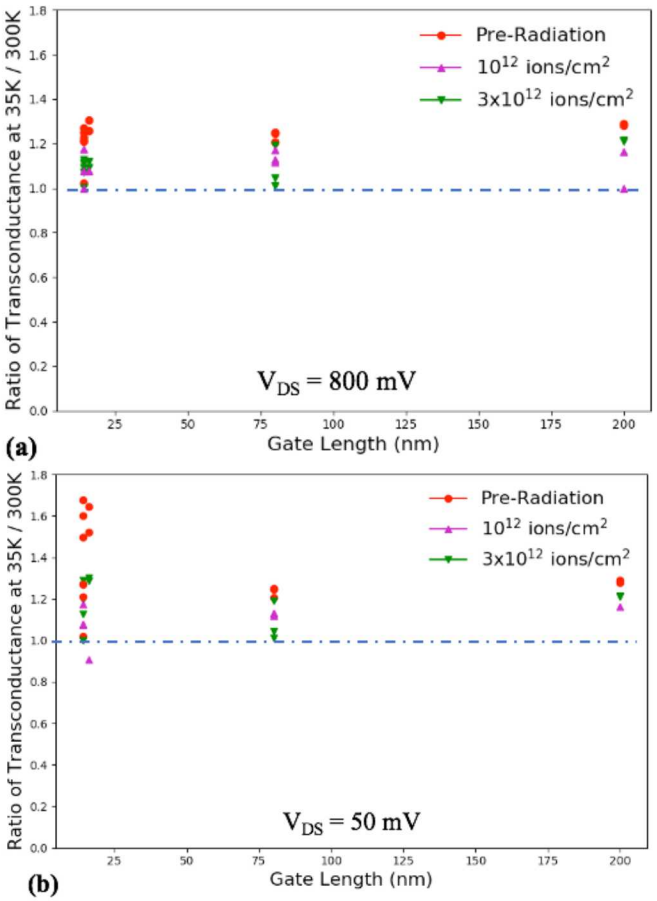

Fig. 6. Ratio of transconductance at 35 K compared to 300 K with varied fluences as a function of gate length for (a) large drain voltage and (b) small drain voltage. The dashed line indicates a ratio of 1.

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