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Evidence of Interface build-up in irradiated 14nm Bulk FinFET Technologies

A. Privat, *Member, IEEE*, H. J. Barnaby, *Fellow, IEEE*, L. Clark, *Senior Member, IEEE*, J. Brunhaver, A. Duvnjak, K. E. Holbert, *Senior Member, IEEE*, M. L. McLain, *Senior, IEEE,* M. J. Marinella, *Senior, IEEE*, and M. P. King, *Member, IEEE*

Abstract **–** The total ionizing dose response of 14nm bulk-Si FinFETs has been studied with specially designed test chips containing several logic gates. TCAD simulations were performed and are consistent with the experimental data.

Keywords – Device modeling, TCAD, FinFET, Total Ionizing Dose, leakage current, 14nm bulk technology

Corresponding (and Presenting) Author:

A. Privat, School of Electrical, Computer and Energy Engineering, Arizona State University, Tempe, AZ, 85287-5706, aprivat@asu.edu

Contributing Authors:

H. J. Barnaby, School of Electrical, Computer and Energy Engineering, Arizona State University, Tempe, AZ, 85287-5706, hbarnaby@asu.edu

K. E. Holbert, School of Electrical, Computer and Energy Engineering, Arizona State University, Tempe, AZ, 85287-5706, Keith.Holbert@asu.edu

L. T. Clark, School of Electrical, Computer and Energy Engineering, Arizona State University, Tempe, AZ, 85287-5706, lawrence.clark@asu.edu

J. Brunhaver, School of Electrical, Computer and Energy Engineering, Arizona State University, Tempe, AZ, 85287-5706, john.brunhaver@asu.edu

A. Duvnjak, School of Electrical, Computer and Energy Engineering, Arizona State University, Tempe, AZ, 85287-5706, aduvnjak@asu.edu

M. L. McLain, Sandia National Laboratories, Albuquerque, NM, 87185, USA, mlmclai@sandia.gov
M. J. Marinella, Sandia National Laboratories, Albuquerque, NM, 87185, USA, mmarine@sandia.gov
M. P. King, Sandia National Laboratories, Albuquerque, NM, 87185, USA, mpking@sandia.gov

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I. Introduction

Over the past decade, sustained advancements in semiconductor technology and fabrication processes have improved the performance of CMOS integrated circuits. These advancements include the use of high-k gate dielectrics and metal-gates as well as the development of non-planar Metal-Oxide-Semiconductor Field-Effect-Transistors (MOSFETs). Among the most promising non-planar MOSFETs is the Fin-based Field-Effect-Transistor (FinFET). The FinFET's unique structure enables it to operate at higher speeds with higher drive currents, lower junction leakage, and better short channel effect (SCE) control compared to traditional planar devices [1]. Today, the FinFET is the dominant MOSFET structure used in CMOS technologies at or below the 14nm node [2], [3].

Scaling of planar MOSFETs has generally led to increased Total Ionizing Dose (TID) tolerance in advanced CMOS technologies. The combination of thinner gate oxides and higher doping concentrations associated with technology scaling has suppressed traditional TID threats such as threshold voltage (V_{TH}) shifts and changes in the on-state drain current [4]–[6]. Depending on the design process, the accumulation of trapped charges in thick isolation oxide layers such as the STI (Shallow Trench Isolation) upon exposure to ionizing radiation can induce drain-to-source leakage paths through the "sub-fin" structure of the bulk FinFET [7], [8]. Fig. 1 illustrates the drain-to-source leakage path upon radiation exposure, noted as (1). This intra-device leakage was previously observed in the past in CMOS technologies [9] and was considered the dominant post-irradiation effect in a recent study on bulk FinFET technologies [10], [11].

In this paper, our test results on specially designed test structures fabricated in a 14nm bulk FinFET process provide strong evidence of interface trap (N_{IT}) build-up in the sub-fin region of the device during irradiation. These defects can give rise to a second radiation-induced leakage path, noted as (2) on Fig.1, from n^+source or n^+drain to p-substrate. Previous studies such as [12] observed N_{IT} build-up in Silicon On Insulator (SOI) FinFETs but there has not been any publications showing N_{IT} build-up in irradiated bulk FinFET technologies. Interface traps, which are related to the oxide quality of semiconductor devices, might affect the performance and the reliability of scaled bulk FinFETs [12]. In order to characterize the effects of radiation-induced N_{IT} build-up forward bias current-voltage measurements across the n^+source to p-substrate diode were performed [13]. The results revealed a distinct increase in the forward bias junction recombination current, which is a strong indicator of N_{IT} build-up [14]. We also report the results of drain-to-source current (I_{DS}) versus gate-to-source voltage (V_{GS}) measurements on nominal FinFET transistors fabricated in the same 14nm process. 3D Technology Computer-Aided Design (TCAD) simulations [15] are also presented to support analysis of the identified TID mechanisms.

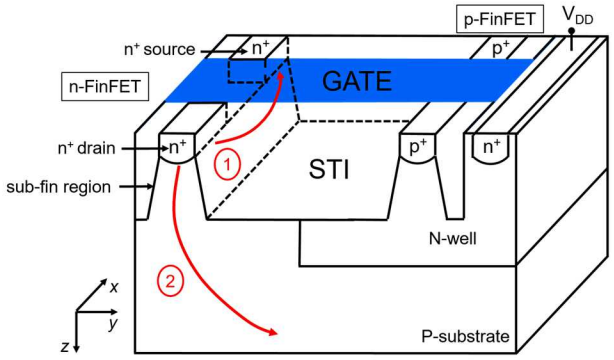

Fig. 1. 3D cross-sectional diagram of the FinFET device showing leakage current upon radiation exposure between the n+ source region and n+ drain region of the same n-channel FinFET (1). The interface traps build-up created in the sub-fin region lead to a second leakage path (2).

II. Experimental Details

A. Test structure design

The 14nm bulk-Si FinFET is one of the first widely available (through foundry manufacturing) non-planar CMOS technologies. For this study a special test structure was designed to characterize TID effects in this technology. The structure includes several modified-in-layout logic gates (i.e., Inverter, NAND, and NOR gates).

Fig. 2 is a representative layout of the structure. It consists of five parallel p-type Pull-Up (PU) and five n-type Pull-Down (PD) networks, which are modified versions of the standard library cells (i.e., INV, NAND2, NAND3, NOR2, and NOR3 gates). The ten networks were altered to provide independent access to each output (drain). For example, the drain of the p-channel (PU) FinFET in the Inverter was bonded out independently of the n-channel (PD) FinFET drain. The gate, V_{DD} (n-well contact), V_{SS} (p-substrate), P_{SOURCE} and N_{SOURCE} are shared between all of the modified logic gates in a single structure. All transistors are designed with four fins in parallel. The width of each fin is W=48nm and its length is L=14nm.

B. Irradiation test plan

Radiation testing was performed at Arizona State University (ASU) using a Co^{60} gamma-ray source. One chip was exposed at a dose rate of 255 rad[Si]/s to several total dose levels. The maximum dose level is 900krad[Si]. The test chip containing the TID structure shown in Fig. 2 was irradiated at room temperature with terminals unbiased during irradiation.

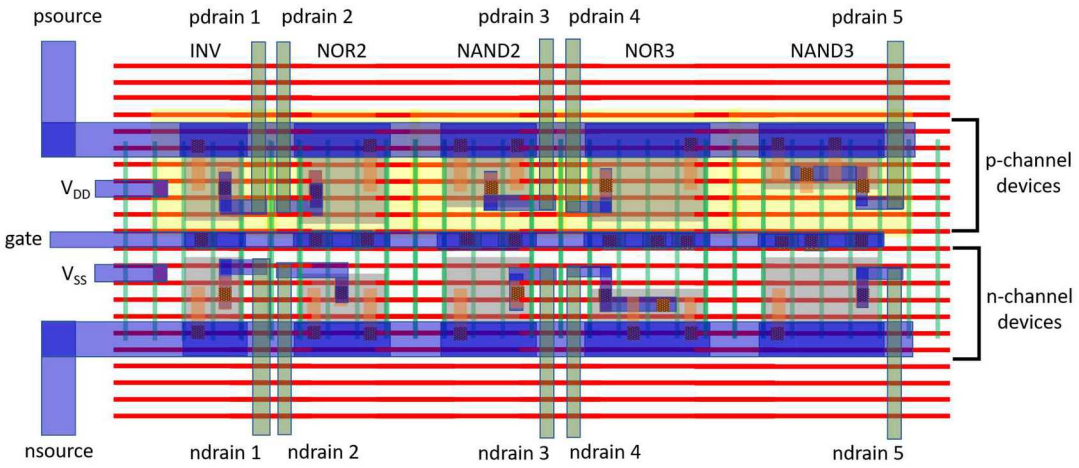

Fig. 2. Simplified layout of the elementary structure containing Inverter, NAND2, NAND3, NOR2, and NOR3 gates.

The electrical characteristics were obtained using a probe station and a Keithley parametric analyzer before and after each step of irradiation.

C. Experimental results

Fig. 3 shows the pre- and post-irradiation I_{DS} vs. V_{GS} characteristics of the n-channel (PD) FinFET device from the modified Inverter structure. The *I-V* curves are plotted from V_{GS}= -0.3V to 0.8V with V_{DS}= 0.8V. The data show no significant increase in the off- and on-state drain currents as a function of gate-to-source voltage (V_{GS}) up to 900krad[Si]. Previous data showed minimal TID effects on the same FinFET bulk technology [8], [10]. It should be noted that since the device was not biased during exposure, this would not likely be representative of the worst case response. Similar results, i.e., no measurable drift in *I-V*, were observed for the p-channel (PU) FinFET device from the Inverter (not shown here). These data, in addition to the response under various other irradiation bias conditions, will be provided in the full paper.

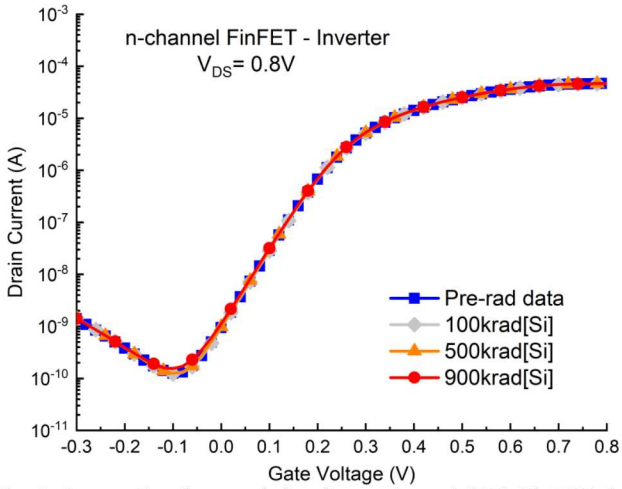

Fig. 3. I_{DS} vs. V_{GS} characteristic of an n-channel (PD) FinFET device after TID exposure. V_{DS}= 0.8V.

Fig. 4 shows the pre- and post-irradiation forward bias current-voltage characteristic of the n^+source to p-substrate diode. Recall that all the sources of the five n-channel (PD) logic gates are connected together, in parallel. The N_{SOURCE} terminal was swept from 0 to -0.8V with V_{SS}= V_{DD}= 0V. All the other contacts were floating during electrical characterization. The experimental data show an increase of the source current as a function of the N_{SOURCE} voltage when the structure is exposed to TID.

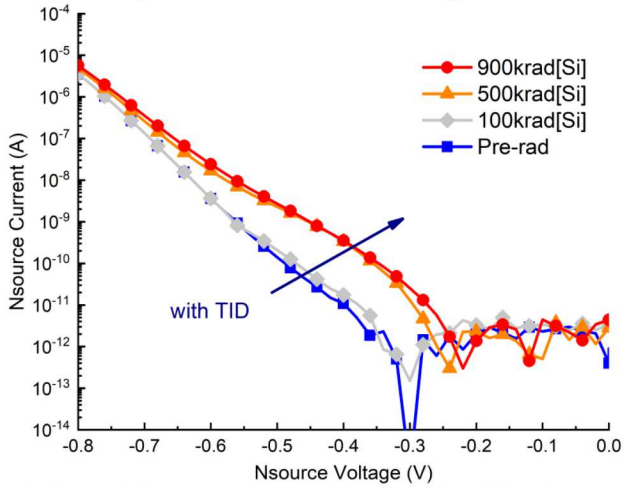

Fig. 4. Forward bias current-voltage characteristic of the n+source/p-substrate diode after TID exposure.

The increase of the current with ionizing dose is characteristic of enhanced carrier recombination in the space-charge region (SCR) of the n^+source/p-substrate diode. Radiation-induced traps at the Si/SiO_2 interface lead to an increase in surface recombination current [14].

Fig. 4 indicates that the buildup (or effect) of N_{IT} saturates after 500krad[Si]. Indeed, no significant change in the source current is observed between 500krad[Si] and 900krad[Si] (red solid line with full symbol). In the next section we report the results of 3D TCAD simulations, which suggest that the radiation-induced interface traps

being measured by these diode characteristics are found in the STI oxide adjacent to the pn junction formed by the n^+source and p-type sub-fin region.

III. TCAD STRUCTURE

A. 3D TCAD FinFET structure

Fig. 5 shows the 3D TCAD FinFET structure including the PU and PD FinFETs (1 fin). The device dimensions and doping concentration levels were obtained from literature [16]–[19] and are provided in Table I. The TCAD structure is representative of a typical 14nm bulk FinFET process.

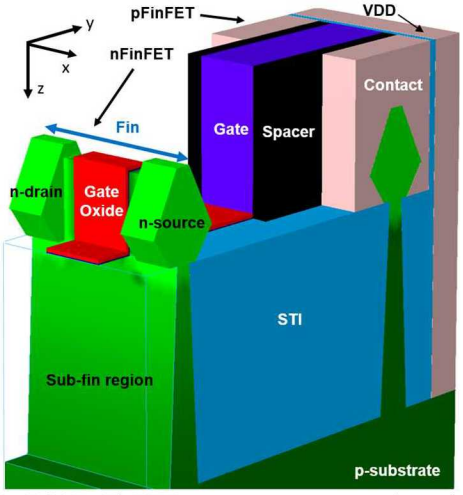

Fig. 5. 3-D TCAD FinFET structure representative of the actual device. The sub-fin region is located below the fin which is surrounded by STI (SiO_2). Some sections were removed for a better view.

TABLE I
MAIN DEVICE PARAMETERS [16]–[19]

Parameter	Value	Unit
Channel length	25.0	nm
Fin Height	37.0	nm
Fin Width	8.0	nm
Spacer width	16.0	nm
STI depth	100.0	nm
Gate thickness	30.0	nm
Total Oxide gate thickness	2.3	nm
Source/drain doping	$5x10^{20}$	cm^{-3}
Bulk doping	$1x10^{16}$	cm^{-3}

The primary steps involved in building the TCAD structures were as follows: 1) fin and STI definition, 2) gate oxide formation, 3) spacer and source/drain epitaxy formation, 4) doping profile definition, and 5) contact formation. The STI region, which isolates the bulk silicon sub-fin from an adjacent transistor, is composed of silicon dioxide (SiO_2). As shown in Fig. 5, the sub-fin region is surrounded by STI. The fin, spacers (nitride), contacts (aluminum), and high-k metal gate are generated using rectangular "box" shapes to reduce the mesh size and simplify the simulations. For the high-k gate dielectric, two oxide monolayers (oxide nitride and HfO_2) are assumed. The source/drain epitaxy (silicon) was generated using polyhedron shapes according to measured cross-sections [19]. Due to high doping concentrations and relatively small device dimensions, the simulations use bandgap narrowing, band-to-band tunneling, Shockley-Read-Hall (SRH) recombination using concentration dependent lifetimes, doping- and temperature-dependent low-field mobility, high field velocity saturation, and transverse-electric-field dependent models.

B. Pre- and post-irradiation simulation results

Fig. 6 shows the pre- and post-irradiation simulated I_{DS} vs. V_{GS} characteristics for the nFinFET (Fig.5). The gate work function was modified to adjust the device threshold to match the pre-irradiation value obtained from the vendor supplied SPICE model [19]. The pre-irradiation simulation results obtained with TCAD (blue dashed line with square empty symbol) and pre-irradiation SPICE model results (blue full line with square full symbol) are well matched. Pre- and post-irradiation simulated I_{DS} vs. V_{GS} characteristics for the pFinFET will be provided in the full paper.

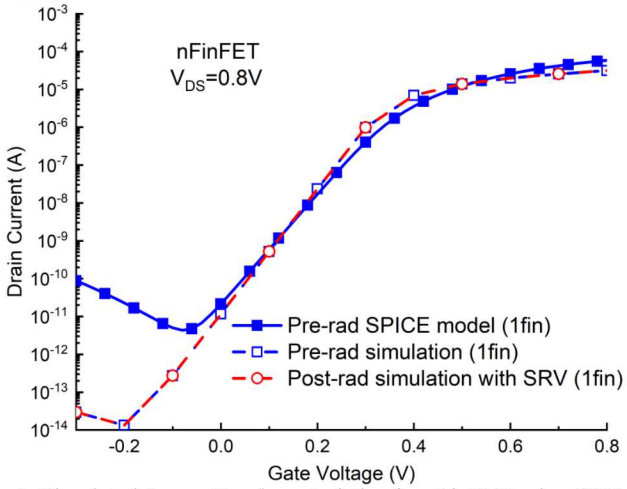

Fig. 6. Simulated I_{DS} vs. V_{GS} characteristics for nFinFET using SRV to model the interface trap build-up at the Si/SiO_2 interfaces. Pre-rad SPICE model is provided for comparison. V_{DS} = 0.8V.

Ionizing radiation exposure causes N_{IT} to build up at $Si\text{-}SiO_2$ interfaces, which will increase surface recombination velocity (SRV) [14]. The variable SRV is expressed as

$$SRV \approx \sigma_S \Delta N_{IT} v_{th}, \quad (1)$$

where σ_S is the carrier capture cross-section for carriers at the surface, v_{th} is the carrier thermal velocity, and ΔN_{IT} is the increase in interface trap density with dose. In our case, TCAD simulations were performed using surface carrier recombination to simulate the effects of N_{IT} buildup. Our simulation results show no change in the off- and on-state drain currents as a function of V_{GS} by

increasing the surface carrier recombination at the Si/SiO_2 interfaces (Fig. 6).

Fig. 7 shows the pre- and post-irradiation simulated forward bias current-voltage characteristics of the n^+source/p-substrate diode. Pre-irradiation experimental data are provided for comparison (blue full line with square full symbol) and match with the pre-irradiation simulation result (blue dashed line with square empty symbol). An increase in the source current as a function of the N_{SOURCE} voltage is observed by increasing SRV at the Si/SiO_2 interfaces. However, at high values of SRV a saturation of the source current occurs. This behavior correlates with the experimental data (Fig. 4).

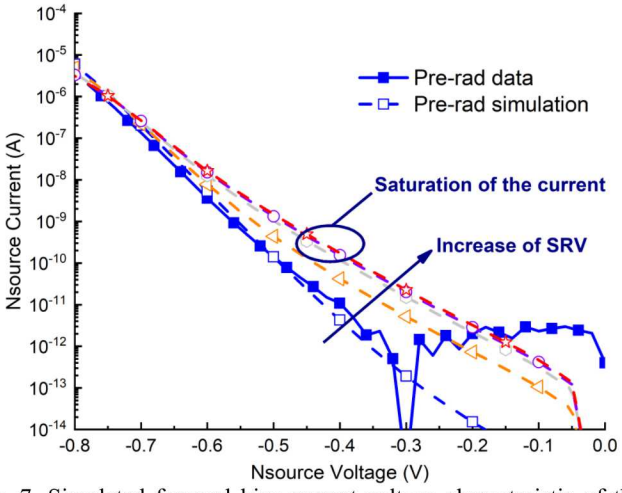

Fig. 7. Simulated forward bias current-voltage characteristic of the diode using SRV to model the traps build-up at the Si/SiO_2 interfaces.

Fig. 8 shows contour plots of the simulated recombination rate in the sub-fin region of the nFinFET at a source voltage of -0.4V. It is shown here that the origin of the increase of source current is due to carrier recombination at interface traps created in the sub-fin region of the device during irradiation.

IV. CONCLUSION

An experimental study on specially designed test structures was performed to investigate the impact of the ionizing dose on 14nm bulk FinFETs. The paper shows evidence of interface trap buildup in irradiated 14nm bulk FinFET technologies. These defects, likely found in the STI oxide adjacent to the sub-fin region of the n-channel FinFET, could lead to an undesirable increase in leakage current of any digital circuit. 3D TCAD simulations were used to investigate this mechanism and simulated results presented in this work correlate qualitatively to the experimental data. To complete the study, further physical investigation and analysis will be performed and reported in the final paper.

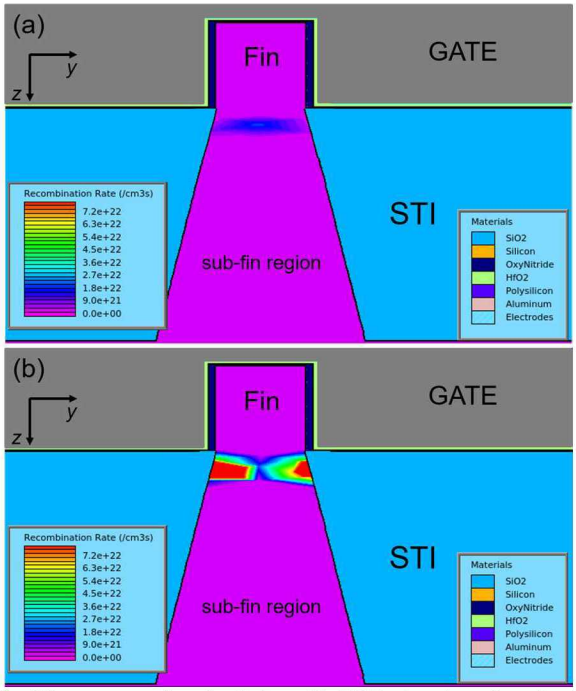

Fig. 8. 2D cross-sectional of the nFinFET showing the simulated recombination rate (a) at pre-irradiation and (b) using SRV to model the traps build-up at the Si/SiO_2 interfaces. V_{SOURCE}= -0.4V. The cutline was done at the middle of the fin.

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