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Process Variation Model and Analysis for Domain Wall-Magnetic Tunnel Junction Logic

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***Abstract* — The domain wall-magnetic tunnel junction (DW-MTJ) is a spintronic device that enables efficient logic circuit design because of its low energy consumption, small size, and non-volatility. Furthermore, the DW-MTJ is one of the few spintronic devices for which a direct cascading mechanism is experimentally demonstrated without any extra buffers; this enables potential design and fabrication of a large-scale DW-MTJ logic system. However, DW-MTJ logic relies on the conversion between electrical signals and magnetic states which is sensitive to process imperfection. Therefore, it is important to analyze the robustness of such DW-MTJ devices to anticipate the system reliability before fabrication. Here we propose a new DW-MTJ model that integrates the impacts of process variation to enable the analysis and optimization of DW-MTJ logic. This will allow circuit and device design that enhances the robustness of DW-MTJ logic and advances the development of energy-efficient spintronic computing systems.**

Keywords* — *domain wall; magnetic tunnel junction; device model; spintronic logic; process variation

I. Introduction

Spintronic devices have been widely explored for applications in memory [1]–[6], Boolean logic [7]–[11], and neuromorphic computing [12]–[15] due to their low-energy consumption, fast transition speed, compact size, and non-volatility. One specific spintronic device, the domain wall-magnetic tunnel junction (DW-MTJ) [16]–[22] is of particular interest because it is one of the few spintronic devices for which direct logic cascading has been experimentally demonstrated. This indicates that DW-MTJs could be exploited to implement large-scale, post-CMOS logic systems.

Two device models have been previously proposed [16], [18], [23] to simulate and analyze DW-MTJ logic; however, the reliability of DW-MTJ circuitry remains unexplored. In this device, the magnetic domain wall is controlled by spin-transfer torque (STT) current, and fabrication imperfections can alter the device behavior. Previously proposed models of DW-MTJs enable the simulation of ideal devices and circuits, and process variations are not taken into account. Therefore, further design and optimization of DW-MTJ logic systems is inhibited without a thorough analysis of the device imperfections due to process variations.

To perform thorough and efficient analysis of the reliability of DW-MTJ circuits, it is necessary to have a model capable of simulating device imperfections. Here, we summarize the operating mechanisms of DW-MTJs and propose a new SPICE model based on [23] that incorporates process variations. Using this novel model for the DW-MTJ, we analyze the robustness of a DW-MTJ circuit under process variations and indicate potential solutions.

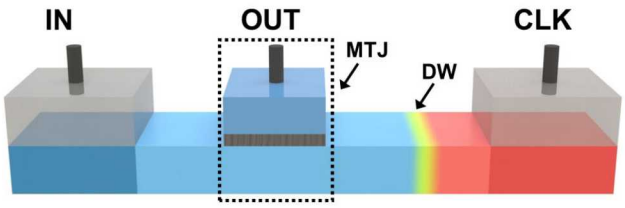

Fig. 1. Device diagram of DW-MTJ.

II. Operation and Modeling of DW-MTJ Logic

The DW-MTJ shown in Fig. 1 is a spintronic device that encodes information with the position of the domain wall (DW) and the corresponding resistance of the MTJ. A ferromagnetic nanowire track at the bottom of the DW-MTJ connects with two antiferromagnetic contacts on the left and right ends. Spin-polarized current flowing through this nanowire track can shift the position of the DW in the direction of electron flow. (For simplicity, all of the currents and voltages described throughout this paper are inverted such that the DW moves in the direction of positive current flow; the model considers the true direction of the currents and voltages.) A tunnel barrier and a fixed ferromagnetic layer on top of the nanowire track form the MTJ, and the MTJ's resistance is determined by the magnetization direction of the portion of the track immediately beneath it.

To transfer data into the device, an input current is used to displace the DW via STT. The MTJ resistance depends on the relative magnetization directions between the top ("fixed") and bottom ("free") layers of the MTJ. Layers with parallel (anti-parallel) magnetization vectors produce a low (high) resistance. These are denoted as P and AP respectively. The DW-MTJ device can be used to represent binary logical states and is able to drive other DW-MTJs. While a DW-MTJ can be configured to implement numerous logic functions [16], [18], two simple logic gates are illustrated in Fig. 2. For DW-MTJ logic, a logic "1" ("0") is defined as an input current that has a current density larger (smaller) than the depinning current density threshold (J_{th}) of the DW. For the buffer in 2(a), an input of '1' ('0') moves the

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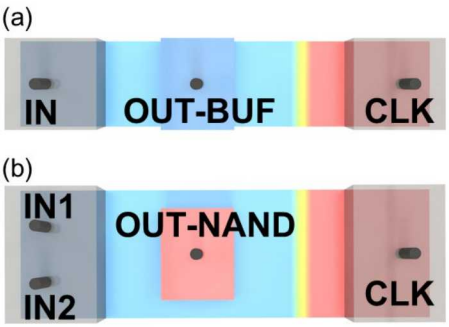

Fig. 2. DW-MTJ (a) buffer and (b) NAND gate. Note that the domain walls have been moved to the right by an STT current.

DW right (does not move the DW), forcing a P (AP) state at the MTJ. When read, this produces a logic '1' ('0'). Similarly, for the NAND gate in Fig. 2(b), a current density of '1' on a single input port will not move the DW, but an input of '1' on both inputs will provide sufficient current to depin the DW and produce an output of logic '0'.

A multi-phase clock is illustrated in the DW-MTJ shift register circuit [16], [18] shown in Fig. 3. The output port (top port) of each DW-MTJ device is connected to the input port (left port) of the next device in the ring. The DW-MTJ logic operation has two phases: the write phase and the read phase. During the write phase, a Boolean current is inputted into the DW-MTJ. During the read phase, a clock signal is applied to the right port of the device, resetting the DW position and generating an output pulse to stimulate the next cascaded stage. If the resistance of the MTJ formed by the magnetizations of the ferromagnetic nanowire track and the fixed layer is low (high) the output current pulse generated by the clock signal will (will not) cause DW depinning in the next stage. While the DW-MTJ is being reset, it is important to ensure that the clock signal is removed before the DW passes across the MTJ in order to prevent a signal glitch or faulty output.

Fig. 4 shows a one-bit full adder [16], [18] implemented with DW-MTJs. As in the shift register circuit, three-phase clocks are applied to different stages to control the data flow direction and enable pipelined computation. This circuit will be analyzed in more detail in section IV.

III. Process Variation -Aware DW-MTJ Model

As described above, DW-MTJ logic requires precise control of the timing between the DW motion and the clock to prevent glitchy or faulty outputs. Likewise, DW-MTJ fabrication imprecision could result in modified width and thickness of the ferromagnetic nanowire track; this would impact the depinning current threshold (I_{th}) and track resistance (R_{track}). Similarly, the MTJ resistances (R_P, R_{AP}) can be impacted by process variations to the MTJ width, length, and thickness. Because the fabrication technology for DW-MTJs has not sufficiently matured, it is

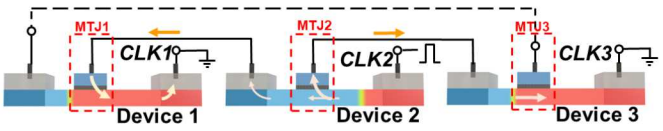

Fig.3. Schematic of DW-MTJ based shift register.

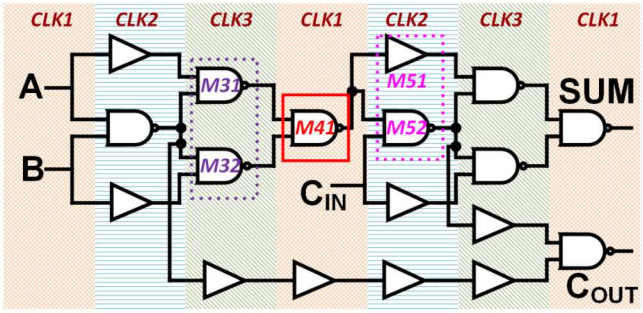

Fig. 4. Circuit schematic of DW-MTJ one-bit full adder.

crucial that DW-MTJ circuit designers are aware of how process variation affects circuit performance and functionality.

No previous model of DW-MTJ devices includes the ability to simulate these variations. Therefore, based on the model of [23], a new SPICE-only model is proposed in this paper that enables the analysis of the robustness of DW-MTJ circuits with the integration of process variation. This new model file will be made available online following publication of this work.

To simulate the reliability of the DW-MTJ circuit under different process mismatches/imperfections, the new model randomizes several critical parameters. This randomization is done uniformly within user-specified bounds and is applied to the parameters in the initial step of each simulation. In this paper, the process variation is applied to several different parameters including track width, track thickness, R_P, interconnect resistance R_{INT}, and J_{th} to analyze the overall circuit sensitivity to different parameter variations.

IV. Device Parameter Range for Functionality

Because the DW-MTJ is driven by STT current and generates an output through an MTJ with limited tunneling magnetoresistance (TMR), the device is sensitive to MTJ resistance variation that could lead to undesired DW pinning or depinning in cascaded devices. Furthermore, the fact that current is used to transmit information between devices creates an issue when there are multiple devices in the fan-out of a DW-MTJ. This is because the output current is divided across the cascaded devices. Therefore, parameter variation in one device may affect the performance of other devices within the same clock phase. As shown in the schematic of the one-bit full adder illustrated in Fig. 4, each DW-MTJ drives one or more devices in the next phase. Taking the DW-MTJ (M41) as an example (highlighted in the red solid box), this device is driven by two other DW-MTJs: M31 and M32 (highlighted in the purple dashed box) and drives two DW-MTJs: M51 and M52 (highlighted in the pink dashed box).

During the read phase of M41, a clock pulse is applied to its right port that generates a current pulse through the output MTJ of M41 to drive the inputs of M51 and M52. While the output MTJ of M41 is in the parallel state, a portion of its output current flows through the ferromagnetic nanowire track of M51 and moves its DW toward the right, resulting in a parallel MTJ state. For the current magnitude to satisfy this switching, the upper boundary of the MTJ parallel state resistance R_P of M41 follows (1)-(2):

$$V_{\mathrm{CLK}} = I_{\mathrm{M41}} * \left((R_{\mathrm{track-M51}} \parallel R_{\mathrm{track-M52}}) + R_{\mathrm{R-M41}} + R_{\mathrm{P-M41}}\right), \quad (1)$$

$$I_{\mathrm{M51}} * R_{\mathrm{track-M51}} = I_{\mathrm{M52}} * R_{\mathrm{track-M52}}, \quad (2)$$

where

$$R_{\mathrm{R-M41}} = \left(1 - \frac{(x_{\mathrm{MTJL}} + x_{\mathrm{MTJR}})}{2 * Length_{\mathrm{DW-track}}}\right) * R_{\mathrm{track-Dual}}, \quad (3)$$

$$R_{\mathrm{track-M51}} = R_{\mathrm{INT}} + R_{\mathrm{track-Single}}, \quad (4)$$

$$R_{\mathrm{track-M52}} = R_{\mathrm{INT}} + R_{\mathrm{track-Dual}}, \quad (5)$$

and

$$I_{\mathrm{M41}} = I_{\mathrm{M51}} + I_{\mathrm{M52}}, \quad (6)$$

while V_{CLK} is the applied clock pulse magnitude; I_{M41} is the current through the ferromagnetic track of M41; I_{M51} and I_{M52} are the currents flowing into M51 and M52, respectively, from M41; $R_{\mathrm{R\text{-}M41}}$ is the M41 track resistance to the right of the MTJ; $R_{\mathrm{P\text{-}M41}}$ is the MTJ parallel state resistance of M41; R_{INT}, $R_{\mathrm{track\text{-}Single}}$, and $R_{\mathrm{track\text{-}Dual}}$ are the interconnect, single-input track, and dual-input track resistances of the circuit, respectively; x_{MTJL} and x_{MTJR} are the x-coordinates of the left and right edges of the MTJ of M41, respectively; and $Length_{\mathrm{DW\text{-}track}}$ is the length of the whole track of M41, as in the model of [23].

In order to move the DW on the buffer device, M51, the output current from M41 to M51 should follow (7):

$$I_{\mathrm{M51}} > I_{\mathrm{th-Single}}, \quad (57$$

where I_{M51} is the current flow through the track of M51, and $I_{\mathrm{th\text{-}Single}}$ is the threshold current of M51 as in the model of [23]. When the input current (from C_{IN}) to M52 is logic "0" (low current), a single high current from M41 should not switch the DW position of M52. Therefore, the lower boundary of $R_{\mathrm{P\text{-}M52}}$ is defined by (8), which produces (9) and (10):

$$I_{\mathrm{M52}} + I_{\mathrm{CIN-AP}} < I_{\mathrm{th-Dual}}, \quad (8)$$

where I_{M52} is the current flowing through M52 from M41, $I_{\mathrm{CIN\text{-}AP}}$ is the input current for logic "0", and $I_{\mathrm{th\text{-}Dual}}$ is the threshold current of a dual-input DW-MTJ as in the model of [23]; the initial value of the parameters under process variation and other key parameters are listed in Table I.

TABLE I. MODEL PARAMETERS

Name	Value	Name	Value	Name	Value
R_{AP}	55 kΩ	$R_{\mathrm{Interconnect}}$	1.8 kΩ	$Width_{\mathrm{Dual}}$	7.5 nm
$I_{\mathrm{th\text{-}Dual}}$	5.4 μA	$R_{\mathrm{track\text{-}Dual}}$	2.6 kΩ	$Width_{\mathrm{Single}}$	5 nm
$I_{\mathrm{th\text{-}Single}}$	3 μA	$R_{\mathrm{track\text{-}Single}}$	3.9 kΩ	$Length_{\mathrm{DW\text{-}track}}$	120 nm

Depending on the circuit structure and device type, each DW-MTJ device has a different output tolerance range. The increased connectivity leads to a dramatically increased complexity of the circuit behavior analysis. While it is possible to analyze a single device within a small circuit, it is nearly impossible to analyze the variation tolerance range of every device in a large-scale system. The new model proposed in this work therefore provides the critical capability to rapidly simulate and analyze the impact of process variations on a large-scale DW-MTJ system. This model has also been applied to large-scale circuit analysis [24].

V. ANALYSIS OF TOLERANCE TO PROCESS VARIATION

To analyze the reliability of the device and logical computing system, a Monte Carlo technique is applied to the one-bit DW-MTJ full adder circuit (Fig. 4) using the randomization process described in section III. The ideal device parameters used here are those used in [16], [18], where the circuit was initially proposed. Three randomly generated input sequences are applied to the input ports over 1000 cycles, and before every cycle, the selected device parameter is randomly set with a uniform random distribution over a defined variation range.

The scatter plots in Fig. 5 and Fig. 6 demonstrate that the output error rate increases with increased variation, with the error bars showing the standard deviation of the mean over the 1000 samples. As can be seen in the figure, $Width_{\mathrm{track}}$ and J_{th} have similar degrees of impact on the circuit error rate, while the circuit has a lower sensitivity to variations in the resistance. In addition, C_{OUT} of the DW-MTJ one-bit full adder is more robust to process variations than the Sum output.

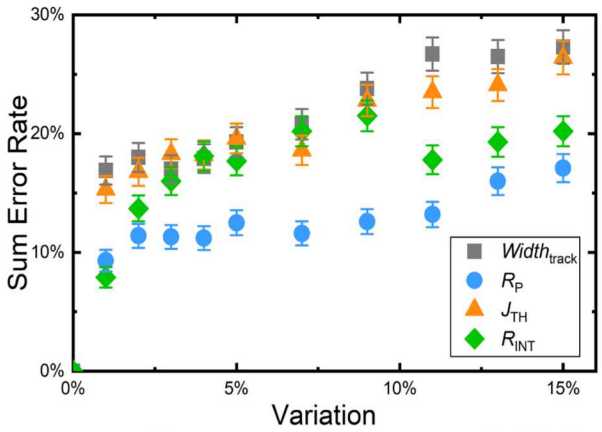

Fig. 5. Error rate of the Sum output of a DW-MTJ one-bit full adder as a function of process variation magnitude.

$$R_{\mathrm{P-M41}} < \frac{\frac{V_{\mathrm{CLK}}}{I_{\mathrm{th-Single}}} - (R_{\mathrm{track-M51}}) - R_{\mathrm{R-M41}}\left(1 + \frac{R_{\mathrm{track-M51}}}{R_{\mathrm{track-M52}}}\right)}{\left(1 + \frac{R_{\mathrm{track-M51}}}{R_{\mathrm{track-M52}}}\right)} \quad (9)$$

$$R_{\mathrm{P-M41}} > \frac{\frac{V_{\mathrm{CLK}}}{I_{th-\mathrm{Dual}} - \frac{V_{\mathrm{CLK}}}{R_{\mathrm{AP}}}} - (R_{\mathrm{track-M52}}) - R_{\mathrm{R-M41}}\left(1 + \frac{R_{\mathrm{track-M52}}}{R_{\mathrm{track-M51}}}\right)}{\left(1 + \frac{R_{\mathrm{track-M52}}}{R_{\mathrm{track-M51}}}\right)} \quad (10)$$

For a deeper understanding of these errors, the error rate for various input combinations is explored in Fig. 7 and Fig. 8; it should be noted that due to the clocking style used by this non-volatile logic family, the error rates are independent of previous input combinations. For the same level of process variation, some input combinations produce vastly larger error rates, indicating that the circuit is particularly sensitive to process variations for these input combinations.

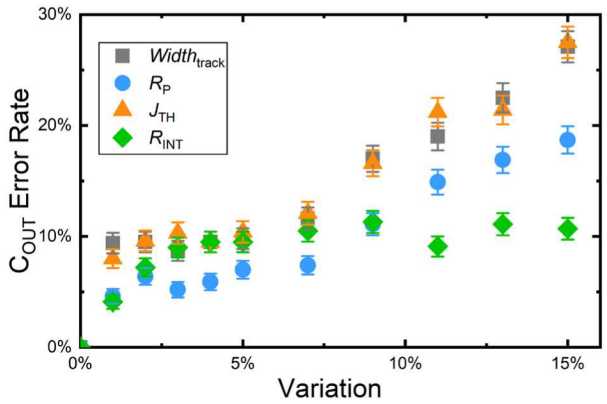

Fig. 6. Error rate of the C_{OUT} output of a DW-MTJ one-bit full adder as a function of process variation magnitude.

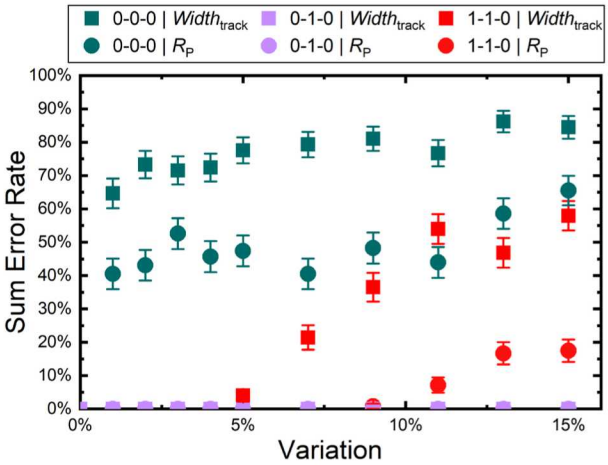

Fig. 7. Error rate for the Sum output of a DW-MTJ one-bit full adder as a function of input combination and $Width_{track}$ and R_P process variation.

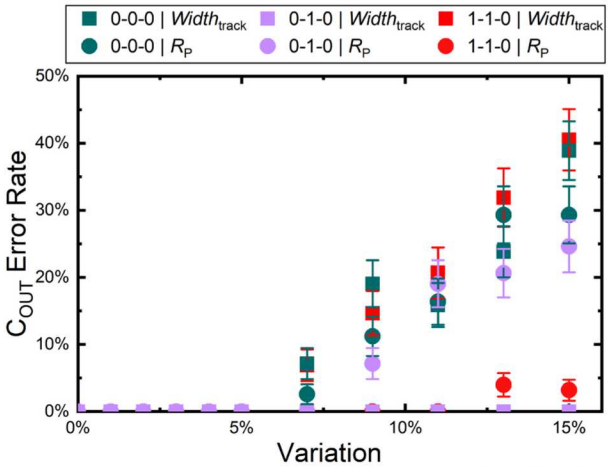

Fig. 8 Error rate for the C_{OUT} output of a DW-MTJ one-bit full adder as a function of input combination and $Width_{track}$ and R_P process variation.

The sensitivity of the error rate to input combination is particularly clear in Fig. 7, as the full adder has a high error rate for the Sum output even with small process variations for the 0-0-0 input combination; this results from the fact that some parameters are already close to the functionality boundaries for this input combination. While the parameters used in this model are designed to represent the results from [16], [18], it is possible to reduce the error rate by optimizing the device parameters. Also, by detecting the critical parameters of the circuit using the proposed model, this model enables device and circuit optimization to enhance circuit robustness by tuning device parameters to balance the error rates across all input combinations.

VI. Conclusions

The DW-MTJ is one of the few spintronic devices for which direct logic cascading has been experimentally demonstrated without any external buffering/amplification stages, enabling purely-spintronic non-volatile computing systems with no need for CMOS circuitry between devices. To advance the development of this technology, this paper proposes a SPICE-only DW-MTJ model with random parameter fluctuations that supports investigation of the robustness of the DW-MTJ system to process variations. The error rate of the DW-MTJ one-bit full adder is evaluated with Monte Carlo simulations using this model, which are thoroughly analyzed under various types and magnitudes of process variations. This model also enables the identification of the most critical device parameters and input signal combinations, thereby providing the understanding necessary for device and circuit optimizations for robust and efficient operation of DW-MTJ computing systems.

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