ITRW: Formulating a Roadmap for WBG and UWBG Materials and Devices

by Victor Veliadis, Robert Kaplar, Jon Zhang, Sameh Khalil, Jack Flicker, Jason Neely, Andrew Binder, Stanley Atcitty, Peter Moens, Mietek Bakowski, and Mark Hollis

Introduction

The purpose of the *International Technology Roadmap for Wide-Bandgap Power Semiconductors (ITRW)* Materials and Devices Working Group, which considers the materials science of Wide- and Ultra-Wide-Band-Gap (WBG and UWBG) semiconductors, in addition to device design, fabrication, and evaluation, is to formulate a long-term, international roadmap for WBG and UWBG materials and devices, consistent with the packaging and applications working groups of ITRW. The working group is co-chaired by Victor Veliadis (primarily representing silicon carbide (SiC) and related materials) and Robert Kaplar (primarily representing gallium nitride (GaN) and related materials, as well as emerging ultra-WBGs) and is split into four sub-working-groups, which are:

1. SiC materials and devices (co-chairs Jon Zhang and Mietek Bakowski)
2. Lateral GaN materials and devices (co-chairs Sameh Khalil and Peter Moens)
3. Vertical GaN materials and devices (co-chairs TBD)
4. Emerging UWBG materials and devices (co-chairs Mark Hollis)

The first two subgroups represent technology that is far more mature than that of the latter two, and devices are available as commercial products in power applications. The primary focus of this article will be on developments in subgroups 1 and 2, with only brief descriptions of the latter two sub-groups, including future activities as they mature technologically.

SiC Materials and Devices

The SiC Materials and Devices sub-Working-Group (SiC-MDWG) of the ITRW was formed in 2018 and is composed of experts from industry and academia with specialization in SiC materials and devices. The team is documenting SiC power devices at different development stages. This includes desired device types (e.g. MOSFET, JFET, IGBT, GTO, etc.) for specific applications, operating conditions, and required voltage and current ratings in the short-term (~1-5 years), and long-term (~6-10 years). The cost target in $/A is key for SiC devices to be widely adopted in power systems, and will be emphasized. In 2018, a technical questionnaire for SiC materials and devices was created. The questionnaire was distributed internationally (US, Asia, and Europe) to collect feedback from SiC experts in academia and industry. The roadmap on SiC materials and devices incorporates feedback from this questionnaire and from other communications with SiC experts. The roadmap outlines key markets and application areas for SiC power electronics, the performance targets SiC technologies are expected to meet over time, technical barriers to achieving those targets, and activities needed to overcome those barriers.

With respect to SiC substrates and epitaxy, 150 mm wafers are commercially available, and the majority of commercial devices are produced on wafers of this area. 200 mm wafers have been demonstrated at trade shows, and their market introduction in the near future is expected to lead to cost reductions and to improved competitiveness with Si. 650 to 1700 V SiC planar metal-oxide-semiconductor field-effect transistor (MOSFETs) are commercially available from several vendors, and certain voltage ratings also have trench MOSFET offerings. 3.3 kV MOSFETs are

rigorously investigated for near term product release. 6.5 and 10 kV MOSFETs have been demonstrated and are next in line for commercialization. The issue of MOSFET degradation with body diode current conduction is being addressed by multiple vendors, and this will accelerate 3.3 to 10 kV MOSFET product releases. The SiC IGBT is the device of choice for applications requiring +15 kV power conditioning. Work in tailoring the ambipolar lifetime to optimize performance is underway, and large-scale commercialization of these devices is about 10 years away.

Market Forecast of SiC Power Devices and Applications

Prices for SiC devices have been declining rapidly in the past few years, helping fuel the recent market growth. SiC MOSFET prices, for example, dropped 50% between 2012 and 2015 according to IHS Markit [1]. Although prices rose in 2017 due to wafer supply shortages, a growing number of wafer suppliers and improved wafer quality should allow prices to stabilize in 2019 and then continue to decline in the foreseeable future. This improvement in cost competitiveness is helping SiC dislodge Si in certain applications (e.g. hybrid and electric vehicles). In addition, leading manufacturers now have trillions of hours of field device experience to assuage any reliability concerns that might dampen growth. A recent study by IHS Markit projects annual SiC revenues will reach $10 billion by 2027, with hybrid and electric vehicles making up the vast majority of sales. Across these applications, discrete power devices will account for most of the growth as they are expected to take off faster than power modules and integrated circuits. A separate forecast by Cree Inc. also predicts that EVs will present a tremendous growth opportunity for WBG materials, particularly SiC [2]. To date, automakers have announced plans to spend $150 billion in the EV market. Cree estimates that even modest EV adoption – approximately 10% of total vehicles sales by 2027 – could result in SiC revenues of $6 billion. The same forecast places the total SiC PE market at over $5 billion by 2022, largely driven not only by EV adoption but also by industrial and telecom applications. SiC technology has already proven its technical advantages over Si, and recent decreasing prices are fueling adoption.

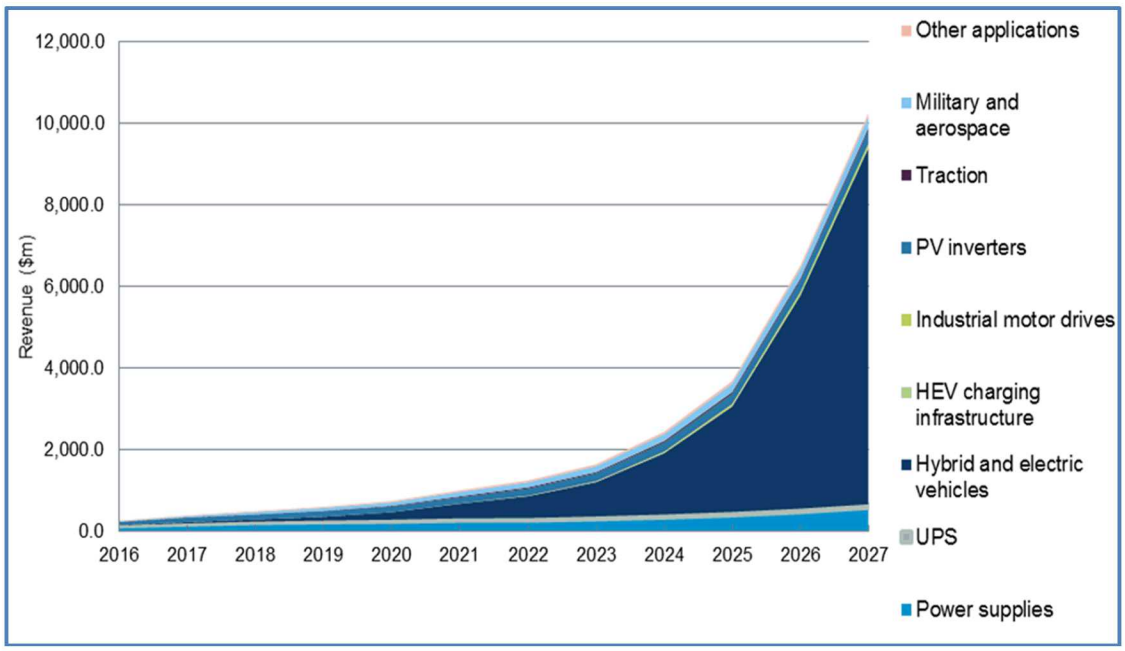

Figure 1: The world market for SiC power devices.

Figure 1 shows various SiC device applications and their potential market size over time [3]. The key near-term application with large market penetration size is EV/HEV inverters, and its revenue could reach $10 billion in 2017. According to the Electric Vehicles Initiative, over 20 million electric vehicles may be on the road in 2020, climbing to over 200 million by 2030 in the most ambitious scenario. Motor drive inverters with high power density and efficiency at elevated temperatures are essential to EVs. SiC semiconductors are ideal for such applications because of their advantages over Si in high-temperature and -frequency operation. Lower system costs and vehicle design simplifications will improve PE device integration with vehicles. The cost competitiveness of SiC semiconductors is the main hurdle in EV/HEV inverter adoption. UPS, power supply, PV, and traction are currently big markets for SiC power devices as well, and their market penetration is expected to further increase in the coming years.

Performance Targets for SiC Power Devices in Various Applications

To accelerate SiC technology adoption, the PE community must focus on applications that are most likely to deliver immediate (within 5 years) improvements in efficiency, reliability, and total cost of ownership. These in turn will encourage further market growth and industry demand. For long-term applications, SiC power devices normally have higher voltage ratings than their near-term counterparts. Fabricating high-voltage devices at high yields in large volumes will remain a challenge for at least the next few years. Table 1 shows SiC MOSFET performance targets for some of the near term and long-term applications.

Table 1. Performance targets for SiC applications [4].

Performance Target	Year 1-5	Year 6-10
Electric Vehicle Inverters		
Rated Current for MOSFET [A]	> 50	> 100
Cost [$/A]	< 0.3	Cost parity to Si IGBT
PV Inverters		
Rated Current for MOSFET [A]	> 50	> 100
Cost [$/A]	< 0.3	< 0.2
SiC, 650V: Data center		
Rated Current for MOSFET [A]	> 50	> 100
Cost [$/A]	~ 0.1	~ 0.1
Grid-tied energy storage (SiC, 3.3-10kV))		
Rated Current for MOSFET [A]	> 10	> 50
Cost [$/A]	< 5	< 2
Heavy-duty vehicle (SiC, 1.7-3.3kV))		
Rated Current for MOSFET [A]	> 50	> 100
Cost [$/A]	< 2	< 1

SiC Power Devices Pricing Comparison

Figure 2 compares the cost of various Si and SiC power devices. The data were obtained in December of 2017 from the Digikey distribution price list. SiC diode and MOSFET devices listed in PowerAmerica's Device Bank were also included in the comparison, although the number of comparable devices was limited. In general, SiC power devices become increasingly more expensive than their Si counterparts as voltage rating increases. For example, at 1200 V, the price of SiC diodes is 2.5-3x higher than that of their Si counterparts. At 10 kV, SiC diodes can cost as much as $20/Amp. For 600 V SiC switches, there is approximate cost parity with Si. Above 900 V, SiC device prices are 2-4x higher than those of Si IGBTs. The price differential is primarily attributed to the higher material cost of the SiC substrate/epitaxy and the higher cost of SiC devices with larger chip area. Devices with larger chip areas and thicker epitaxy experience lower yields due to the presence of material and processing defects, which reduce yield thereby increasing cost.

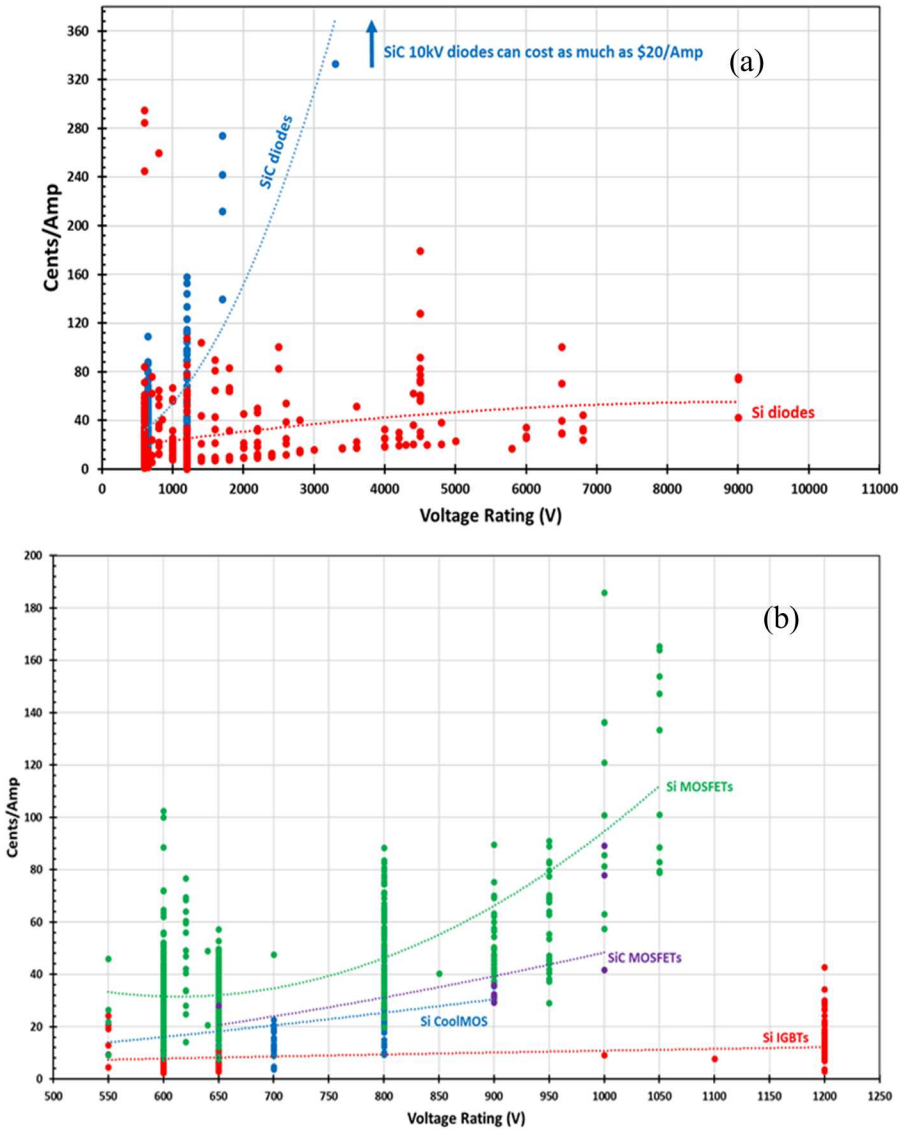

Figure 2: Cost comparison between SiC and Si power devices (a) diodes, and (b) switches [4].

In addition to higher quality SiC wafer material to increase yield and reliability, other areas of improvement include wafers with higher planarity to accommodate processing in high volume foundries, higher quality gate oxides to improve threshold voltage stability and mobility, and improvements in short-circuit performance and ruggedness to rival those of Si devices. Better understanding of degradation/failure mechanisms under harsh conditions (i.e. high voltages and/or high temperatures) will drive device design optimization. Development of SiC-specific high voltage/frequency/temperature reliability standards will facilitate system insertion. Finally, to increase fabrication throughput and yields, innovations in SiC doping will focus on room temperature implantation with minimal generation of killer defects.

Lateral GaN Materials and Devices

Current State-of-the-Art: HEMTs

The adoption of normally-off lateral GaN power devices in the commercial market has so far been limited to p-GaN gate devices and d-mode GaN HEMTs in cascode configuration with an e-mode Si MOSFET. Panasonic's gate injection transistor (GIT) is one such example of a p-GaN gate device, with a demonstrated drain current of 200 mA/mm, on-state resistance of 2.6 mΩ-cm^2, and an off-state breakdown of 800 V [5]. To solve the issue of current collapse, the GIT structure was modified to include a hybrid drain (HD-GIT), shown in Figure 3, which is used to compensate for hole emission in the buffer and has been demonstrated to eliminate current collapse phenomena up to 980 V [6,7]. More work has been done on the HD-GIT structure to reduce process variation associated with gate-recess, and V_T standard deviation has been reduced significantly as a result of a new process named "through recess and regrowth gate" [6].

In the cascode configuration, a low-voltage normally-off Si MOSFET is paired with a normally-on high-voltage GaN HEMT to produce an effective e-mode power device (Figure 4 (a)). This cascode approach offers the advantage of improved switching speed and reduced switching loss due to the mitigation of the Miller effect. Recent work has shown progress for monolithically integrated cascode structures, including an all-GaN integrated structure (shown in Figure 4 (b)) [8]. This not only reduces package parasitics between the Si and GaN devices of the conventional cascode but also reaps the benefits of the native e-mode GaN device and the reduced circuit instability caused by device mismatch.

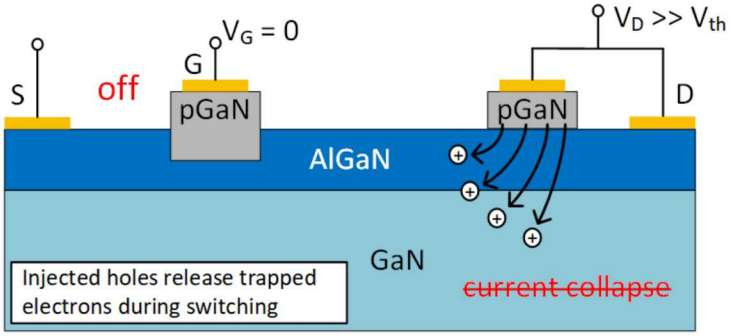

Figure 3. Example of HD-GIT structure showing injection of holes in the off-state to eliminate current collapse.

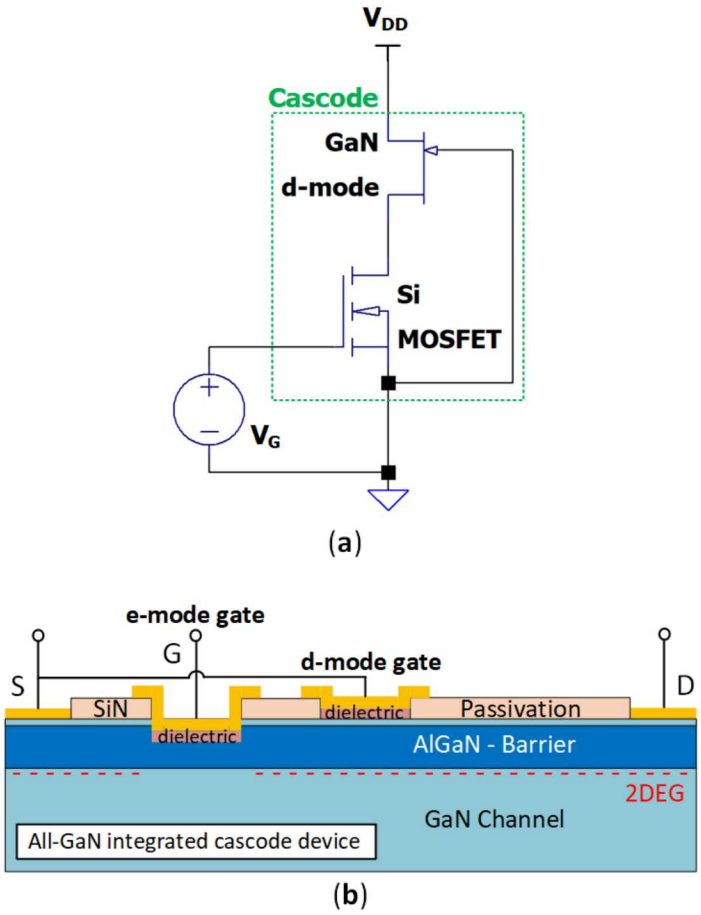

Figure 4. (a) Conventional GaN+Si cascode circuit diagram, and (b) Example of an all-GaN monolithically integrated cascode device.

To enable growth of GaN on large-diameter Si wafers, it is necessary to reduce bowing and growth stress. The improvement of crystallinity in epitaxial films and precise management of growth stress are critical to the success of large-diameter GaN processing, which allows for cost reductions. Recent work with superlattice structures has demonstrated crack-free 2 µm GaN layers grown on 200 mm Si using AlN/GaN superlattice layers [9]. With a superlattice buffer structure, compressive and tensile stresses can be precisely adjusted resulting in controllable wafer bow (Figure 5). The caveat is that compared to a graded buffer structure, a superlattice structure (SLS) suffers from poorer thermal performance. From this perspective, it is desirable to further improve the thermal performance of superlattice structures or to reduce inherent growth stress and defect density in graded buffer structures.

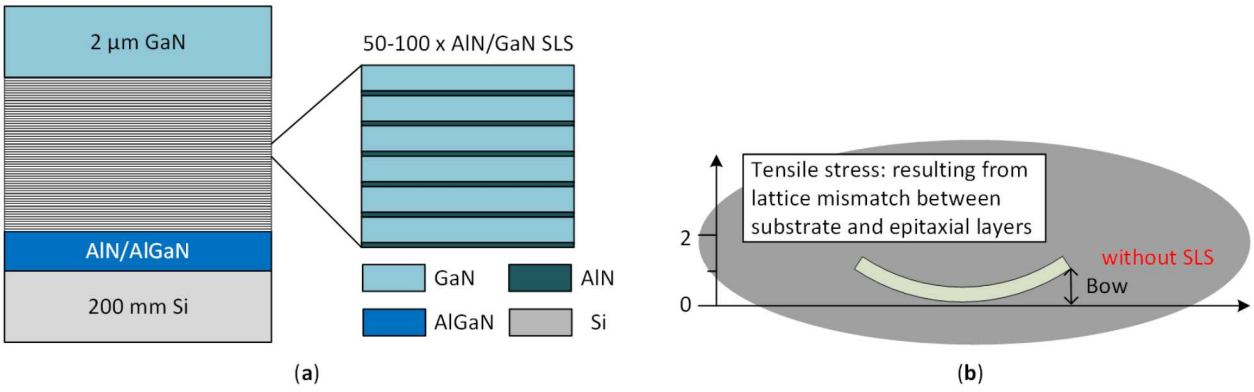

Figure 5. (a) Examples of a superlattice buffer structure used to mitigate growth stress, and (b) tensile stress that occurs in the absence of an SLS due to lattice mismatch.

Current collapse is still a critical issue for commercial GaN power devices, although progress has been made recently in mitigating this issue. As mentioned, Panasonic's HD-GIT structure is known to eliminate current collapse by compensating for hole emission in the buffer. Another method to suppress current collapse is to compensate for surface interface traps resulting from dangling bonds and nitrogen vacancies. Recent work by Tang *et al.* [10] demonstrates that a charge-polarized AlN passivation layer can suppress current collapse so long as the polarization charge density is higher than the interface trap density. In addition, the use of a nitrided interfacial layer via *in-situ* plasma nitridation prior to deposition of the gate dielectric or passivation has proven successful for compensating nitrogen vacancies and passivating Ga dangling bonds, creating a high-quality interface and reducing interface traps [11].

Foundation Keystones

The foundational requirements for GaN devices and materials fall mainly into three categories: improved heterostructure growth, robust normally-off device designs, and refined reliability characteristics. As GaN power HEMTs are transitioning in commercial production from 6" to 8" Si wafers, minimizing wafer bow and the associated growth stress becomes increasingly critical to creating a high-yield and uniform process. Revisions to the heterostructure design and growth processes are necessary not only to reduce stress but also to decrease material defects and to improve thermal performance. GaN technology enables a significant improvement in power density and with an associated reduction in die size. This introduces thermal management challenges like effectively extracting heat from the system. These challenges must be addressed both at the materials and at packaging levels.

Recent advances in normally-off device designs, including the HD-GIT, have produced more robust outcomes, but more progress must be made in the areas of both process uniformity and reliability. Recently, device reliability has been studied extensively , resulting in significant improvements in this area. However, additonal work must be done to fully understand degradation mechanisms and further improve reliability. Two areas of note include studying circuit and mixed-mode reliability, as well as expanding device ruggedness and safe operating area to rival those of Si. Circuit designers need to be confident in the long-term reliability of GaN power devices – otherwise adoption will be limited and slow.

Lateral GaN Concluding Remarks

The Lateral GaN Materials and Devices sub-Working-Group (L-GaN-MDWG) of the ITRW covers a similar scope as the SiC-MDWG described earlier in this document, but with a focus on Lateral GaN power devices (AlGaN/GaN High Electron Mobility Transistors, HEMTs) as outlined in the previous section. Such devices are now beginning to play an important role in power electronics due to their superior intrinsic material properties as compared to those of present silicon-based power devices. This is based on several key technical advances, listed below along with representative seminal publications on each topic:

- Epitaxial growth of GaN layers on Si substrates up to 8" diameter [12]
- Device processing in CMOS-compatible fabrication lines [13]
- Achievement of normally-off operation using approaches such as p-gates or a cascode configuration [14]
- Extension of breakdown voltage using edge termination techniques such as field plates [15]
- Mitigation of reliability concerns such as dynamic on-resistance, threshold voltage shift, and time-dependent dielectric breakdown [16]

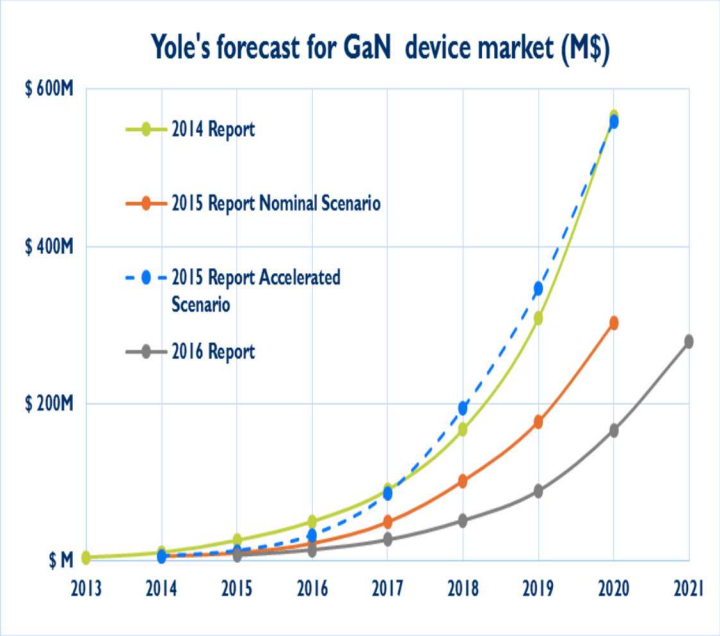

Figure 6. GaN Market Forecast [17]. Source: Yole Développement

GaN-based Radio-Frequency (RF) devices have already demonstrated commercial success valued at more than $100M, and while GaN power device R&D efforts have nearly reached their 15-year mark, revenue forecasts have been lowered over the last few years as shown in Figure 6, signaling market penetration slower than originally projected. However, the fundamentals of the value proposition remain strong, and several key industry-wide efforts are underway to advance the technology including ITRW as well as JEDEC and JETTA that seek to standardize reliability testing, qualification, parametric testing, and datasheets. These efforts will contribute to the widespread adoption of GaN power electronics technologies. In parallel with these efforts, much

research remains to be done to address issues such as device robustness (since GaN power HEMTs do not exhibit avalanche breakdown), reliability concerns (such as hard-switching reliability), and integration with gate drive circuitry and other components (reactive and/or thermal management) at the package/module and chip levels.

Vertical GaN Development

Availability of native 2- and 4-inch GaN substrates [18,19] are enabling breakthroughs in vertical GaN devices. Compared to their lateral counterparts, vertical GaN devices can deliver higher breakdown voltage and higher power density. In addition, vertical GaN promises higher reliability as a result of shifting the peak electric field from the surface to the bulk, which also serves to minimize trapping effects and to reduce dynamic on-resistance. Another key benefit is that unlike lateral GaN, vertical GaN devices can survive and operate in the avalanche region; avalanche energy capability has been demonstrated at 1000 mJ [20]. Fabricating vertical devices on CTE- and lattice-matched bulk GaN is the best way to maximize the potential of GaN so that device performance fully exploits the excellent intrinsic material properties.

There has been recent progress both in vertical GaN diodes and transistors grown on native substrates. High breakdown voltages have been reported, with p-n diode breakdown voltage demonstrated at over 4 kV [21], and a reported blocking voltage of 1.6 kV for vertical GaN trench MOSFETs [22]. However, much work remains to be done to reach a higher breakdown target. One such challenge is the design of effective junction termination extension (JTE) structures in GaN. These structures are necessary to alleviate electric field crowding at the edge of the junction, which causes premature breakdown. In vertical Si and SiC power devices, this can be done by implanting a p-region at the edge of the junction that is charge balanced to the drift region. However, this single zone JTE design is sensitive to interface charge, dose, and process variations. If the single-zone JTE is not effectively charge-balanced then its efficiency can be severely impacted. More complex structures can be designed to help compensate for this, however, even in Si and SiC this poses a challenge. In GaN, the problem becomes more severe due to the present limitations in selective-area p-type doping. Activation of an implanted p-type dopant in GaN requires an annealing temperature of over 1300 °C, which causes decomposition of GaN at atmospheric pressure [19,23]. As a result, Mg implantation suffers from low activation efficiency, and a limited effective range of implantation energy and dose [19,23].

Vertical GaN power devices show promise for high voltage, high current opeartion, in which they can potentially outperform lateral GaN as well as vertical SiC devices. Many challenges in vertical GaN still need to be overcome at the materials and processing levels, as this technology is far less mature than lateral GaN and SiC.

Ultra-Wide-Bandgap Semiconductors

Beyond vertical GaN, a new class of materials known as ultra-wide-bandgap (UWBG) semiconductors is presently being investigated [24]. The leading materials in this class are Aluminum Nitride / Aluminum Gallium Nitride, Gallium Oxide, and Diamond, although others are also being investigated.. The potential advantage of these materials, as with the wide-bandgap materials, lies in their ability to withstand higher electric fields without going into avalanche breakdown.Just like SiC and GaN have an advantage over Si in this respect, UWBG

semiconductors may have an advantage over SiC and GaN. However, work on these materials is still in an early research phase, and fundamental challenges such as the growth of large-area substrates, the ability to effectively dope the materials, the ability to form low-resistance ohmic contacts, the ability to integrate the semiconductors with other materials such as dielectrics, and the understanding of the intrinsic breakdown mechanisms largely remain to be addressed. Nevertheless, work on these materials has ramped up significantly over the past couple of years, and working device prototypes have been demonstrated that suggest that the materials may indeed one day out-perform SiC and GaN.

Concluding Remarks

This IEEE ITRW effort addresses the SiC and GaN HEMT device roadmaps in close collaboration with the module / packaging working group as well as the SiC and GaN applications working groups. Additionally, key recent publications in the literature have been consulted, for example, the recent review article by H. Amano *et al*. [25]. The article takes a top-down approach where key power electronics applications and high-value markets are identified and prioritized. SiC devices are expected to target high-value applications with voltage ratings above 900 V, and lateral GaN devices are expected to address high-value applications at 650 V and below. However, some overlap in the 650 to 900 V range is likely to occur. In the long term, vertical GaN devices, and even ultra-WBG devices composed of materials such as gallium oxide, aluminum nitride, and diamond may compete with SiC, although such devices are still in the research phase. Metrics defining the value proposition for high-value applications will drive device design, packages and modules, and circuit topologies. Example device parameters are shown in Table 2. The device specifications and reliability requirements are driven by market needs: such as in consumer, industrial, or automotive markets. Other performance metrics may influence adoption as well. For example, GaN may be favored earlier in some niche applications, such as in satellite power systems, due to its intrinsic resilience to space irradiation. Charting a roadmap with short-, medium-, and long-term projections for GaN power devices should be informed by the targeted performance, application space, reliability, cost per Amp, efficiency, frequency, and power density.

Table 2. Key device metrics for benchmarking power devices [26].

	Silicon	**SiC**	**GaN**
Concept	Super junction	Planar MOSFET	e-mode HEMT
Blocking voltage	600V	900V	600V
On-state resistance (typ.)	56 mOhm	65 mOhm	55 mOhm
Reverse recovery charge	6000 nC	130 nC	0 nC
Energy stored in C_{oss} @ 400V	8.1 µJ	8.8 µJ	6.4 µJ
Charge stored in C_{oss} @ 400V	420 nC	70 nC	40 nC
Turn-off loss @ 10A / 400V	15 µJ	10 µJ	10 µJ

Path Forward

The ITRW materials and devices working group convenes periodically at major industry events, such as the Applied Power Electronics Conference (APEC) and the Workshop on Wide-bandgap Power Devices and Applications (WiPDA) to present its strategy for defining the SiC, GaN, and emerging power device roadmaps. This initial version of the roadmap will be continuously updated

via these meetings, coupled with additional communications within and between the different working groups.

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