

Silicon Electrolyte Interface Stabilization (SEISta)

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Background

This quarter, we have focused on characterizing the electrochemical of native oxide and “pristine” silicon surfaces by electrochemical cycling for various conditions, starting with either a freshly etched Si surface, or varying amounts of oxide on the surface (either native grown or deposited). These changes can be used to determine if the pristine surface evolves differently than those that have been modified (Q1 milestone). We are also developing new diagnostics (microcalorimetry and stress measurement in-situ) to determine how the nature of the silicon surface affects the composition, function, and thickness of the SEI (Q2 milestone).

Results

Cycling studies (Q1 milestone)

The performance of 50 nm grown SiO₂, bare silicon, and native oxide on silicon were studied in 2032 coin cells. The cells cycled at a rate of C/3 between 1.5 V and a minimum of 0.05 V. The lower voltage cutoff was supplemented by a 5-hour time limit to continue cycling in the event the cells did not reach 0.05 V. The lower voltage was typically ~ 0.15 V. The electrodes were composed of a degenerately doped silicon wafer with copper on the bottom for electrical contact with 20 nm titanium adhesion layer, 500 nm copper, and 50 nm silicon thin film on the surface. A new hydrofluoric acid treatment station was set up and used to remove the native oxide of the silicon samples. The capacity and coulombic efficiency, to date, are shown in Figure 1. Within error, all three sample types performed equivalently. The observed capacities are all above the theoretical capacity achievable at room temperature (3579 mAh/g). This trend continues past the SEI formation cycles, suggesting that the underlying silicon substrate is being lithiated, in addition to the silicon thin film. This makes the assumed active mass of the electrode incorrect, leading to inaccurate capacities. New electrodes, with silicon thin films on copper foils, are being designed to address this issue. Because this issue has shown itself across several different experiments at the various laboratories when using a “thick” silicon sample, we are preparing new sample standards for the program that remove this based upon the initial work done by Kostecki, where a solid Cu ram was polished, and Si was deposited on the polished surface to a fixed thickness. While this sample prep is compatible with the T-cell standards available throughout the program, it is less compatible with the coin cell standards, and will not support additional integration into some of the standard test cells being developed for in-situ analysis. A new standard sample,

based upon an evaporated 50nm Si backed by a 2um evaporated Cu foil is being developed, and should eliminate the issue with anomalous lithiation seen with Si handle substrates.

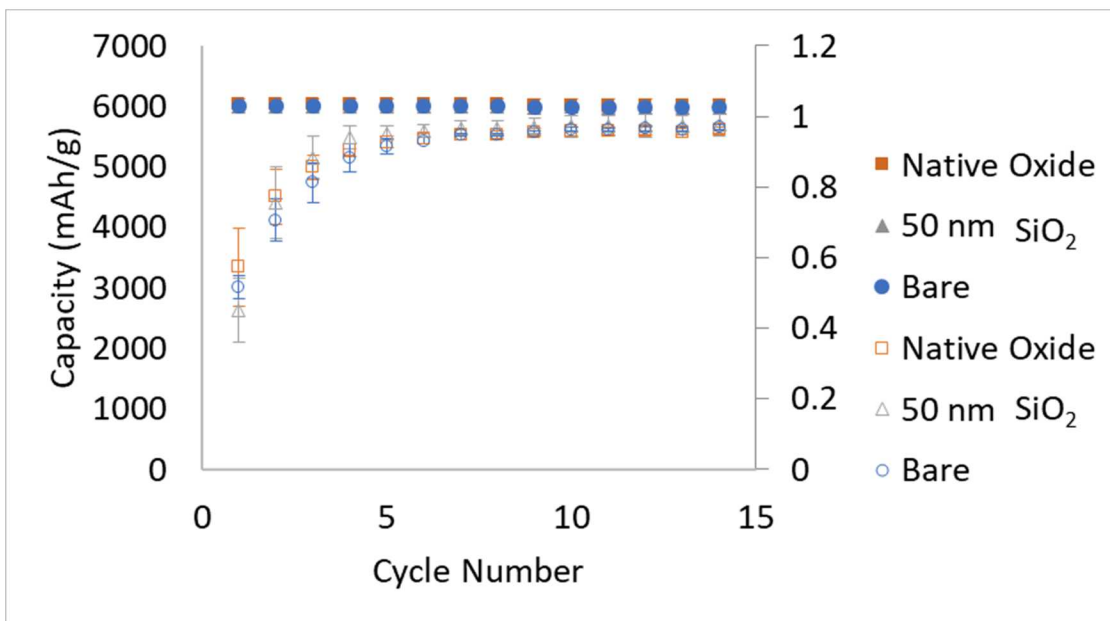


Figure 1 Capacity (solid fill) and coulombic efficiency (outline) for the native oxide (squares), 50 nm SiO₂ (triangles), and bare silicon (circles). The capacities are well above the theoretical, room temperature capacity of silicon. This is attributed to lithiation of the underlying silicon substrate.

Interfacial Stress Measurement for Q2 milestones

The new electrodes are designed for use in an in-situ cell setup for Moiré interferometry. The cell will be used in future measurements of strain in the SEI under varying conditions. The current cell design is shown in Figure 2a, featuring a PEEK body and metal heating block. Two chambers are utilized to allow for pressure equalization to prevent the thin electrodes from rupturing. The electrodes are 2 um copper foils with a 50 nm Si thin film, held in place by an O-ring and washer. The thin foil electrodes are intended to enable magnified changes in stress in the electrode, leading to the easier measurement of strain.

For characterization of the electrodes, an FTIR was obtained and placed in an argon-filled glovebox for future compositional analysis and a Moiré interferometer was constructed in-house. The first half of the custom microscope is displayed in Figure 2b, including the optical illumination arm, objective, and camera. A schematic of what the finished interferometer will consist of is shown in Figure 2c. The Moiré illumination arm, containing the reference grating, is currently in progress.

Microcalorimetry and Powder Studios

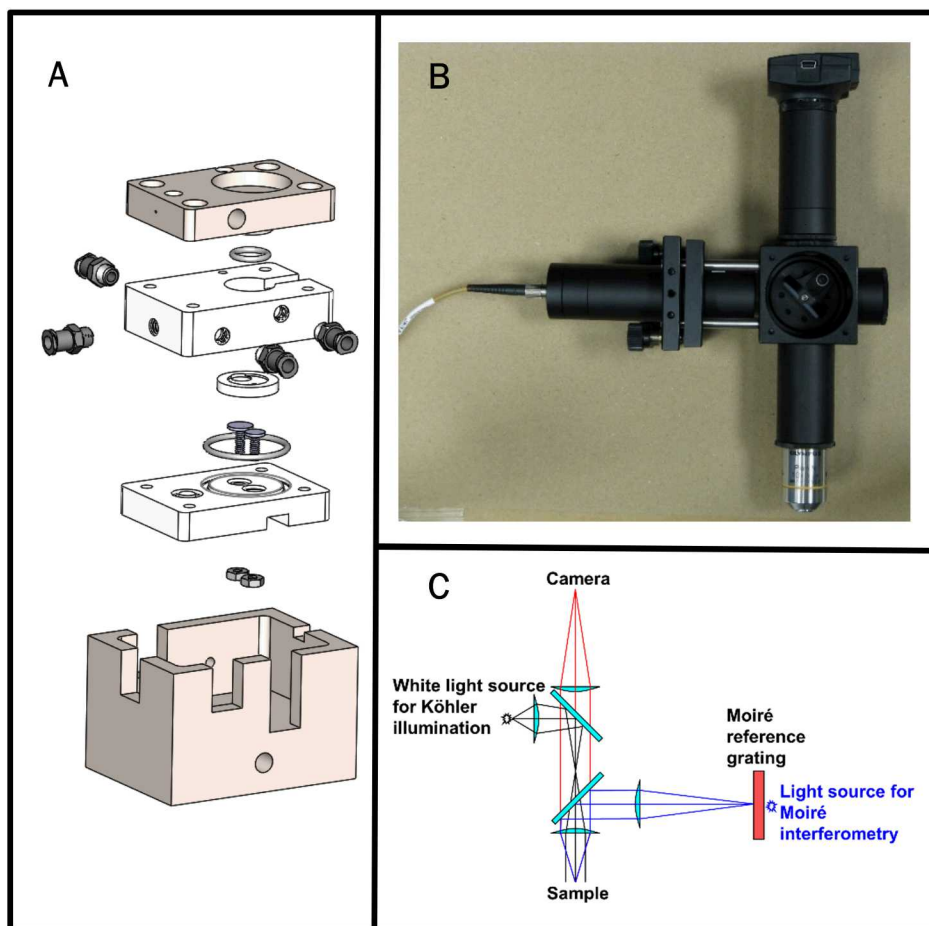


Figure 2: A) Moiré in situ cell design with PEEK pieces in white and the metal heating elements in beige. B.) Current custom microscope with optical illumination arm complete. C.) Schematic of the targeted design of the final Moiré microscope.

When processed and incorporated into electrodes, silicon active material surfaces are altered from their pristine conditions in a way that likely influences SEI formation and function. To understand the difference between model silicon systems and powders incorporated into electrodes, microcalorimetry has been employed to measure the heat generated from the aqueous processing of silicon powders with LiPAA binders and carbon additives. Based on knowledge of Si surface reactivity and supported by measurement of H_2 gases released during processing, it is assumed that the heat generated during electrode slurry processing is primarily attributable to the reaction of silicon and water to form SiO_2 on the silicon particle surfaces. Microcalorimetry curves in Figure 3 show the heat flow from a select silicon powder in a slurry mixture over time, as well as fit curves that are used to estimate the total heat generated from the slurries. The energy generated from these slurries is significant, but as shown in Table 1 still amounts to a relatively small capacity loss of $< 4\%$, even under the extreme case of processing the material for 96 hours. While data is still preliminary, coin cell cycling correlates moderately well showing, for example, an initial coulombic efficiency reduction of 2.67% at 96 hours aging, very close to our predicted value.

Quantification of signal to noise for perfusion testing of silicon and other electrode materials is still underway, with plans to install a fixed temperature bath and isolated, valved tubing system to reduce sampling noise during liquid perfusion into the microcalorimeter.

Conclusions

Evidence regarding the performance of differing layers of SiO₂ on Si standards seem to show what has been observed by other groups, that the SiO₂ layer thickness does not seem to affect either the capacity or the coulombic efficiency of the cells, which suggests that the SEI oxide layer rides on top of the lithiation and delithiation of the substrate. Given that these are flat samples, it is possible that this layer gives a substantively different response from what would be seen on a particle, in which the increasing internal volume would fracture the oxide and give rise to additional consumption of the electrolyte. Stress measurements to be made will confirm this thinking in the next quarter.

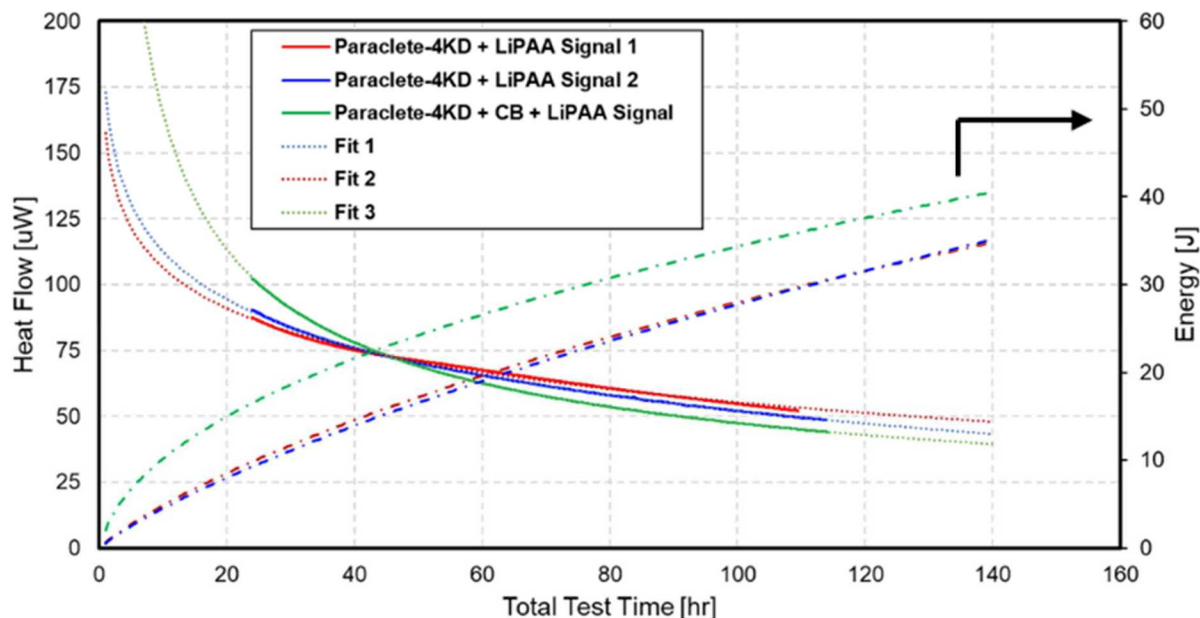


Figure 3 Microcalorimeter heat flow curves measured for select silicon slurry mixtures along with fit curves to predict the overall degree of reaction in each sample.

Table 1: The quantified energy generation based on the fit curve of the Paraclete-4KD + CB sample in Figure 1 as well as predicted material and performance loss based on the formation of silica

Duration (hr)	Energy Generated (J)	SiO ₂ Formed (mol)	Silicon Loss (%)	Specific Capacity Retained (%)	ICE Reduction (%)
0	0	0	0	100	0
24	16.522	5.74e-05	.79	98.31	1.35
48	23.372	9.25e-05	1.13	97.58	1.93
96	33.656	1.17e-04	1.61	96.57	2.73

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