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Draft Electric Rule 21 Test Protocols for Advanced Inverter Functions

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Abstract

Disclaimer: The following document includes draft certification protocols and should not be viewed as a consensus-based performance standard.

Distributed energy resources (DERs), such as photovoltaic (PV) systems, when deployed in a large scale, are capable of significantly influencing the operation of bulk and local power systems. Looking to the future, European and American stakeholders are working on standards to make it possible to manage the potentially complex interactions between DER and the power system. One of the jurisdictions considering modifications to the DER interconnection requirements is California. To determine what changes could improve electric grid reliability and allow greater penetrations of renewable energy, the California Public Utilities Commission (CPUC) and the California Energy Commission (CEC), in conjunction with consultant Frances Cleveland, convened the Smart Inverter Working Group (SIWG) in January 2013. The SIWG—composed of state agencies, utility engineers, national laboratories, manufacturers, trade associations, and advocacy groups—provided the CPUC a set of recommendations in early 2014[1]. The recommendations included specific advanced DER functions and interoperability requirements, along with a proposed timeline, for California to add new capabilities to grid-interconnected DER. On August 18, 2014 the three California Investor-Owned Utilities (IOUs)—Pacific Gas and Electric Company (PG&E), Southern California Edison Company (SCE) and San Diego Gas & Electric Company (SDG&E)—drafted a Advice Letter filing to the CPUC setting forth revisions to Electric Tariff Rule 21 to conform to the seven recommendations made by the Working Group[2]. After a comment period, the CPUC issued an update to the IOU recommendations[3]. At the time of this publication, there was no final legal ruling on the CPUC Rulemaking (R.) 11-09-011 ("Order Instituting Rulemaking on the Commission's Own Motion to improve distribution level interconnection rules and regulations for certain classes of electric generators and electric storage resources").

In the U.S., Nationally Recognized Test Laboratories (NRTLs) independently verify products to safety and functional standards. PV inverters are certified to Underwriters Laboratories (UL) Standard 1741[4]. However, new advanced inverter functions described in the SIWG and IOU proposals are not included in this standard, so there is a critical need to develop test protocols for these functions in preparation of a positive ruling by the CPUC. Through a California Solar Initiative Grant, Sandia National Laboratories (Sandia or SNL), Underwriters Laboratories (UL), Electric Power Research Institute, Inc. (EPRI), Xanthus Consulting, SunSpec Alliance, Loggerware, and utility and PV inverter manufacturers have collaborated to draft this certification protocol for the Rule 21 SIWG Phase 1 advanced inverter functions. This report also includes test procedures for Phase 2 and Phase 3 functions that will be demonstrated later in the CSI4 project. This collaborative effort was performed in close junction with the UL 1741 Standards Technical Panel (STP) working group. This document represents a snapshot of the draft testing protocols at the time of publication and not a consensus certification protocol for advanced inverters.

[1] California Public Utilities Commission, "Recommendations for Updating the Technical Requirements for Inverters in Distributed Energy Resources, Smart Inverter Working Group Recommendations," Filed 7 Feb 2014.
[2] J.J. Newlander, R.G. Litteneker, S.W. Walter, M. Dwyer, Joint motion of Pacific Gas and Electric Company (U 39 E), Southern California Edison Company (U 338 E) and San Diego Gas & Electric Company (U 902 E) regarding implementation of smart inverter functionalities, Rulemaking 11-09-011 Advice Letter, 18 July, 2014.
[3] J.T. Sullivan, CPUC Rulemaking11-09-011 Agenda ID #13460, 13 Nov, 2014.
[4] Underwriters Laboratories Std. 1741 Ed. 2, "Inverters, Converters, Controllers and Interconnection System Equipment for use with Distributed Energy Resources," 2010.

ACKNOWLEDGEMENTS

This document compiles a number of draft protocols from the Underwriters Laboratories 1741 Standards Technical Panel working groups. The collaborative process of drafting consensus certification procedures is a difficult, time-consuming effort and the dedication of this group cannot be overstated. The authors would particularly like to thank Tim Zgonena from UL for leading this process; John Berdner from Enphase Energy for leading the ride-through working group; Taylor Hollis from Schneider Electric for leading the volt-var and fixed power factor working group; Sigifredo Gonzalez at Sandia for leading the anti-islanding working group; and Jay Johnson at Sandia for leading the ramp rate and soft-start ramp rate working group.

Sandia National Laboratories acknowledges the support of the California Solar Initiative and U.S. Department of Energy (DOE) Office of Electricity (OE) program for sponsoring the development of this protocol.

CONTENTS

ACRONYMS

AMI	Advanced Metering Infrastructure
ANSI	American National Standards Institute
CPUC	California Public Utilities Commission
CEC	California Energy Commission
DER	Distributed Energy Resources
DMS	Distribution Management System
DOE	Department of Energy
ECP	Electrical Coupling Point
EMS	Emergency Management System
EPRI	Electric Power Research Institute
EPS	Electric Power System (electric utilities or their surrogates)
EUT	Equipment Under Test
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
NEC	National Electrical Code
NFPA	National Fire Protection Association
NIST	National Institute for Standards and Technology
NTP	Network Time Protocol
PV	Photovoltaic
RLC	Resistive/Inductive/Capacitive
SEP	Smart Energy Profile
SEPA	Solar Electric Power Association
SGIP	Smart Grid Interoperability Panel
SOC	State Of Charge
SNL	Sandia National Laboratories
SNTP	Simple Network Time Protocol
TCP/IP	Transmission Control Protocol/Internet Protocol
UL	Underwriters Laboratories

Introduction

Advanced inverter functions have the ability to assist with bulk system frequency problems, distribution-level voltage deviations, and provide additional protection and resiliency to the electric power system. These capabilities come at limited cost but can greatly increase the penetration of photovoltaic and other renewable energy on the grid. To harness these new capabilities and help California meet its aggressive renewable energy targets[5], the California Public Utilities Commission ordered a review of distribution-level interconnection rules and regulations for certain electric generators and electric storage resources[6]. To assist with this process the California Public Utilities Commission (CPUC) and the California Energy Commission (CEC) convened a Smart Inverter Working Group (SIWG) in January 2013. The SIWG—composed of state agencies, utility engineers, national laboratories, manufacturers, trade associations, and advocacy groups—provided the CPUC a set of recommendations in January 2014. The recommendations included a specific advanced Distributed Energy Resource (DER) functions and interoperability requirements along with a proposed timeline for California to add new capabilities to grid-interconnected DER. On August 18, 2014 the three California Investor-Owned Utilities (IOUs)—Pacific Gas and Electric Company (PG&E), Southern California Edison Company (SCE) and San Diego Gas & Electric Company (SDG&E)—drafted a Advice Letter filing to the CPUC setting forth revisions to Electric Tariff Rule 21 to conform to the seven recommendations made by the Working Group. After a comment period, the CPUC issued a minor update to the IOU recommendations on November 13, 2014. Since no legal ruling has been issued, the latest CPUC recommendations were used for the basis of the following draft certification procedures for the Electric Rule 21 advanced inverter functions.

In the U.S., Nationally Recognized Test Laboratories (NRTLs) independently verify products for safety and performance. PV inverters are certified to Underwriters Laboratories (UL) Standard 1741, which has been harmonized with IEEE 1547-2003 and IEEE 1547.1-2005. Since California is going beyond the national requirements set out in IEEE 1547-2003 and the new IEEE 1547a-2014, it is the responsibility of the UL 1741 Standards Technical Panel (STP) to develop the new advanced inverter performance test protocols to list these advanced devices for interconnection in California. The UL 1741 STP is composed of dozens of experts from industry, utilities, and government. Through a California Solar Initiative (CSI) Grant "EPRI Standard Communication Interface CSI4 Project," Sandia National Laboratories and other CSI participants contributed to drafting the new advanced inverter function certification procedures. This effort was performed in close junction with the UL 1741 Standards Technical Panel (STP) working group. The results of this effort are included in this report: certification protocols for all seven Rule 21 Phase 1 advanced inverter functions, two Phase 2 functions, and two Phase 3 functions which will be demonstrated in the latter stages of the EPRI CSI4 project. Also note that many of the proposed Rule 21 Phase 3 functions are based on the International Electrotechnical Commission (IEC) Technical Report (TR) 61850-90-7, so the previous Sandia IEC 61850-90-7 testing protocols[7-8] could be used as the basis for the UL 1741 certification protocols.

This document is structured with separate appendices for Rule 21 advanced inverter functions. The functions included in this document are displayed in Table 1, however the Rule 21 Phase 2 and Phase 3 functions are not defined fully by the SIWG or the IOUs, so these certification protocols must be updated based on future SIWG discussions surrounding these functions. Abbreviations for the protocols are labeled R21-x-y, where x is the phase and y is the function designator; for instance, R21-1-AI is Anti-islanding Protection in Rule 21 Phase 1. The

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[5] Office of Governor, Governor Brown Signs Legislation to Boost Renewable Energy, 4-12-2011. URL: http://gov.ca.gov/news.php?id=16974

[6] CPUC, Rulemaking 11-09-011, "Order Instituting Rulemaking on the Commission's Own Motion to improve distribution level interconnection rules and regulations for certain classes of electric generators and electric storage resources," Filed September 22, 2011.

[7] J. Johnson S. Gonzalez, M.E. Ralph, A. Ellis, and R. Broderick, "Test Protocols for Advanced Inverter Interoperability Functions – Main Document," Sandia Technical Report SAND2013- 9880, Nov 2013.

[8] J. Johnson S. Gonzalez, M.E. Ralph, A. Ellis, and R. Broderick, "Test Protocols for Advanced Inverter Interoperability Functions–Appendices," Sandia Technical Report SAND2013-9875, Nov 2013.

function designator is matched to IEC TR 61850-90-7 nomenclature when there is a synonymous function, e.g., L/HVRT, INV3, VV11, and DS93.

Table 1: Phase 1 and select Phase 2 and 3 Advanced DER functions in the Rule 21 SIWG recommendations.

Appendix	Function or Communication Verification	Protocol Abbreviation
1	Anti-Islanding Protection (AI)	R21-1-AI
2	Low/High Voltage Ride-through (L/HVRT) and Low/High Frequency Ride-through (L/HFRT)	R21-1-L/HVRT R21-1-L/HFRT
3	Normal Ramp Rate and Soft-Start Ramp Rate	R21-1-RR R21-1-SS
4	Fixed Power Factor and Volt-Var Mode with Watt-Priority	R21-1-INV3 R21-1-VV11
5	Communication Interface	R21-2-CI
6	Data Model	R21-2-DATA
7	Monitor Alarms	R21-3-A
8	Monitor DER Status and Output	R21-3-DS93

The order of the appendices does not define a default testing order of the functions. Different test sequences may be used upon agreement between the equipment manufacturer and the NRTL.

Appendix 1 – R21-1-AI
Anti-islanding Protection

Version 1.0 31 May 2014 – Original Version (Harmonized with UL 1741)
Version 2.0 7 Oct 2014 – Harmonized with UL 1741 version 11 from 9/12/14
Version 2.1 25 Nov 2014 – CSI4 team edits

Recommended UL Test Procedure for Unintentional Islanding

Underwriters Laboratories Std. 1741-2010 Section 40, Utility Interaction, references the requirements from IEEE 1547-2003, Standard for Interconnecting Distributed Resources with Electric Power Systems, and IEEE 1547.1-2005, Standard for Conformance Test Procedures for Equipment Interconnecting Distributed Resources with Electric Power Systems. This document is written to match the IEEE 1547.1 Section 5.7, Unintentional Islanding, format but expected to be inserted into Section 40 of the UL 1741 Standard.

1.1 Unintentional Islanding with EPS Support Functions Enabled

This unintentional islanding test procedure addresses unintentional islanding evaluation on the Equipment Under Test (EUT) with Electric Power System (EPS) support functions enabled. This test differs from IEEE 1547.1-2005 Section 5.7.1 by including grid interactive functions, i.e. commanded real power level, commanded reactive power level, voltage/frequency ride-through functions, and autonomously implemented voltage and frequency EPS support functions.

1.1.1 Unintentional Islanding test

1.1.1.1 Purpose

The purpose of this test is to verify that the DER ceases to energize the EPS as specified in an applicable requirements document or manufacturer specification when an unintentional islanded condition is created and the DER is verified to be compliant both with and without EPS support functions enabled. The applicable requirements document must determine the trip time response for the test conditions specified herein.

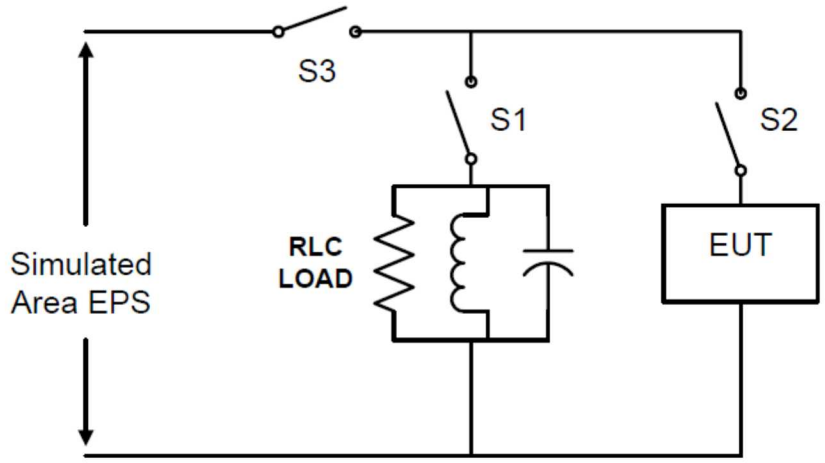
Note: when considering multiple requirements documents, the manufacturer and NRTL may use engineering judgment when testing. For example, where a unit has been evaluated over a wider parameter/function range, all other requirements inside that range will be certified.

1.1.1.2 Procedure

This test procedure is designed to be universally applicable to all DRs, regardless of output p.f. Any reactive power compensation by the EUT should remain on during the test.

Where the EUT manufacturer requires an external or separate transformer, the transformer is to be connected between the EUT and resistance, inductance, and capacitance (RLC) load specified in Figure 1[9] and is to be considered part of the product being tested.

[9] Notes in text, tables, and figures are given for information only and do not contain requirements needed to implement this standard.



NOTES
1—Switch S1 may be replaced with individual switches on each of the RLC load components.
2—Unless the EUT has a unity output p.f., the reactive power component of the EUT is considered to be a part of the islanding load circuit in the figure.

Figure 1: Unintentional islanding test configuration.

a) For a single-phase EUT, the test circuit shall be configured as shown in Figure 2. The neutral connection (grounded conductor) of the RLC load, the simulated area EPS, and the EUT shall be unaffected by the operation of switch S3. For a multiphase EUT, the balanced load circuit shown in Figure 2 is to be applied between each phase to neutral for a four-wire configuration or between phases for a three-wire configuration. Switch S3, as shown in Figure 2, shall be gang-operated and multi-pole.
b) Connect the EUT according to the instructions and specifications provided by the manufacturer.
c) Set all EUT input source parameters to the nominal operating conditions for the EUT.
d) Set and verify the EUT parameters are at maximum adjustable voltage and frequency ranges, maximum adjustable response durations, and EPS support functions are set as described below.
    i. For each of the functions to be verified as compatible with unintentional islanding compliance, the manufacturer shall identify parameters that adversely affect islanding detection and state the worst-case condition for the EUT to be anti-islanding compliant. Additional definition of worst-case conditions shall be identified by the manufacturer and test laboratory.

    Note: This condition is likely to exist when the voltage and frequency ranges and detection times are adjusted to the maximum adjustable settings with L/HVRT and the L/HFRT functions enabled[10]. If a Volt-Var function is to be certified under this procedure, the worst-case parameter values are likely to minimize the deadband, maximize the var production, and maximize the slope of the volt-var curve. If a var-priority volt-var function is to be certified, this function will be enabled over a watt-priority Volt-Var function.
    ii. Given the function configuration to be certified, unintentional islanding tests shall be performed to certify each unique combination of functions grouped together which can be simultaneously enabled as stated by the manufacturer. Functions, which may be grouped within unique function combination groupings, are not required to be retested.
    iii. For example, to test the EUT for hypothetical functions A, B, and C which can be enabled simultaneously, those functions shall be enabled and tested as a group. If the EUT passes the test

[10] Time parameters are set to the largest value within their range of adjustability, the low voltage/frequency parameters are set to the minimum value within their range of adjustability, and the high voltage/frequency parameters are at the maximum value within their range of adjustability.

for this grouping then no additional tests or combinations of A, B, and C required. However, to certify another function D which is mutually exclusive with C, then the grouping A, B, D must tested as well.

e) Set the EUT (including the input source as necessary) to provide 100% of its rated output power.[11]
f) Record all applicable settings.
g) Set the Simulated EPS to the EUT nominal voltage ± 2% and nominal frequency ± 0.1 Hz.
h) Adjust the islanding load circuit in Figure 2 to provide a quality factor Q_f of 1.0 ± 0.05 (when Q_f is equal to 1.0, the following applies: $P_{qL} = P_{qC} = 1.0 \times P$).[12] The value of Q_f is to be determined by using the following equations as appropriate:

$$Q_f = R\sqrt{\frac{C}{L}}$$

or

$$Q_f = \frac{\sqrt{P_{qL} \times P_{qC}}}{P}$$

where

Q_f is the quality factor of the parallel (RLC) resonant load,
R is the effective load resistance (Ω),
C is effective load capacitance (F),
L is effective load inductance (H),
P_{qL} is the reactive power per phase consumed by the inductive load component (VARS),
P_{qC} is the reactive power per phase consumed by the capacitive load component (VARS),
P is the real output power per phase of the unit (W),
f is frequency.

The inductance and capacitance are to be calculated using the following equations:

$$L = \frac{V^2}{2 \times \pi \times f \times P \times Q_f}$$

$$C = \frac{P \times Q_f}{2 \times \pi \times f \times V^2}$$

where

L is effective load inductance (H),

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[11] EUT provided with or intended for use with specific defined input sources that can not provide the input power range described in this test shall be tested within the limitations of the specified or supplied input source. Under these circumstances the test may be performed with the actual source or a simulated source. Test results will be applicable only to the combination of the EUT and specified source, and the test report should reflect this limitation.

[12] Based on the equation $Q_f = \text{Tan}(\text{ArcCos}(\text{d.p.f.}))$, where d.p.f is the displacement power factor, a Q_f of 2.5 is equivalent to an uncorrected load d.p.f of 0.37, a Q_f of 1.8, uncorrected load d.p.f. of 0.48, and a Q_f of 1, uncorrected load d.p.f. of 0.707. Area EPS circuits typically operate above 0.75 d.p.f. in steady-state conditions; therefore, $Q_f = 1$ (d.p.f.=0.707) is below the load d.p.f. that the DR is expected to be islanded with. For a point of comparison, the current draft of IEC 62116 uses a Q_f of 0.65 (d.p.f. of 0.84). A lower value of Q will allow DR manufacturers to use perturbation schemes that are potentially less detrimental to power quality.

V is the nominal voltage across each phase of the RLC load (V) (for loads connected phase to phase, V is the nominal line voltage; for loads connected phase to neutral, V is the nominal phase voltage),
P is the real output power per phase of the unit (W),
Q_f is the quality factor of the parallel (RLC) resonant load,
C is the effective load capacitance (F),
f is frequency.

The reactive load is balanced so that the resonant frequency f of the island circuit is within the underfrequency and overfrequency trip settings of the EUT and as close to nominal frequency as possible.

When tuning for the current balance in this step with a nonunity output p.f. EUT, there will be an imbalance between the L and C load components to account for the EUT reactive current. The EUT reactive output current shall be measured and algebraically added to the appropriate reactive load component when calculating Q_f.

i) Close switch S1, switch S2, and switch S3, and wait until the EUT produces the desired power level.
j) Adjust R, L, and C until the fundamental frequency current through switch S3 is less than 2% of the rated current of the EUT on a steady-state basis in each phase.[13]
k) Open switch S3 and record the time between the opening of switch S3 and when the EUT ceases to energize the RLC load.
l) The test is to be repeated with the reactive load (either capacitive or inductive) adjusted in 1% increments or alternatively with the reactive power output of the EUT adjusted in 1% increments from 95% to 105% of the initial balanced load component value. If unit shutdown times are still increasing at the 95% or 105% points, additional 1% increments shall be taken until trip times begin decreasing.
m) After reviewing the results of the previous step, the 1% load setting increments that yielded the three longest trip times shall be subjected to two additional test iterations. If the three longest trip times occur at nonconsecutive 1% load setting increments, the additional two iterations shall be run for all load settings in between.
n) Repeat steps d) through m) with the test input source adjusted to limit the EUT output power to 66%.
o) This value is allowed to be between 50% and 95% of rated output power and is intended to evaluate the EUT at less than full power and under the condition where the available output is determined or limited by the input source. If the EUT does not provide this mode of operation, then set the EUT to control the output power to the specified level.
p) Repeat steps d) through m) with the EUT output power set via software or hardware to 33% of its nominal rating with the test input source capable of supplying at least 150% of the maximum input power rating of the EUT over the entire range of EUT input voltages. For units that are incapable of setting or commanding an output power level, the EUT output power shall be limited via the input power source. For units that are incapable of operating at 33%, the EUT shall be tested at the lowest output power the EUT will support. This step is intended to evaluate the EUT at low power and under the condition where the available output is determined or limited by the EUT control setting. If the EUT does not provide this mode of operation, then set the input source to meet the specified output power level.

1.1.1.3 Requirements

Where the EUT requires a separate test input source to conduct this test, that source shall be capable of supplying at least 150% of the maximum input power rating of the EUT over the entire range of EUT input voltages.

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[13] Certain anti-islanding algorithms will sufficiently perturb the fundamental frequency current through switch S3 so that the 2% limit cannot be achieved on a continuous basis. Averaging of the rms current over a number of cycles in a manner that captures the quiescent magnitude of this current shall be utilized for determination of matched load during this quiescent period.

The RLC load shall be tuned so that the fundamental frequency current through switch S3 is less than 2% of the rated current of the unit under test on a steady-state basis in each phase.

The test and measurement equipment shall record each phase current and each phase-to-neutral or phase-to-phase voltage, as appropriate, to determine fundamental frequency real and reactive power flow over the duration of the test. Anti-aliasing filters and sampling frequencies appropriate to the measurement of the fundamental frequency component shall be applied. The minimum measurement accuracy shall be 1% or less of rated EUT nominal output voltage and 1% or less of rated EUT output current.

The equations for Q_f are based upon an ideal parallel RLC circuit. For this reason, noninductive resistors, low loss (high Q) inductors, and capacitors with low effective series resistance and effective series inductance shall be utilized in the test circuit. Real and reactive power should be instrumented in each of the R, L, and C legs of the load so that these parasitic parameters (and parasitics introduced by variacs or autotransformers) are properly accounted for when calculating Q_f. Iron core inductors, if used, shall not exceed a current THD of 2% when operated at nominal voltage. Power ratings of resistors should be conservatively chosen to minimize thermally induced drift in resistance values during the course of the test.

1.1.1.4 Criteria

A test is successful[14] when the DR ceases to energize the test load within the timing requirements of IEEE Std 1547 after switch S3 is opened.

If any of these tests results in islanding for longer than the specified time, the unit fails the test.

The actual trip time for each test shall be recorded.

A single failure of any of these tests is considered a failure of the entire test sequence.

If a non-compliant condition is discovered, this test may be repeated with the settings adjusted differently (e.g., less aggressively) for the EPS support function causing non-compliance. If the adjustment of the EPS support function produces compliance, the EUT range of adjustment for the support function must be modified for the EUT.

Unevaluated combination of functions and features and or ranges of adjustments shall not be accessible to the end user or installer.

Manufacturers desiring to obtain the UL Special Inverter certification, e.g. SA, must pass the unintentional islanding tests with the following EPS support functions enabled.

- R21-1-L/HVRT, Low/High Voltage Ride-Through
- R21-1-L/HFRT, Low/High Frequency Ride-Through
- R21-1-INV3, Commanded Power Factor
- R21-1-VV11, Volt-Var Function with Watt Priority
- R21-1-RR, Normal Ramp Rate
- R21-3-FW21, Freq-Watt Function
- OPT, indicates a non-mandatory function for SA certification.

Table 2 depicts the unique combinations of advanced functions must be enabled to qualify a unit for Rule 21 SA compliance. The functions in Table 2 must be activated with the worst-case parameter sets, as defined by the manufacturer. R21-1-RR is not expected to support the Area EPS or reduce the EUT sensitivity to detect the island; however, if the manufacturer or NRTL determine ramp rate limitation can impact anti-islanding detection, it must

[14] IEEE-1547-2003 and IEEE 1547a-2014 define compliance as ceasing to energize the Area EPS within 2 seconds of the formation of the island.

also be enabled and tested, as shown in Tests 4-5. If the EUT is certifying a Frequency-Watt function, it must be tested as well, as shown in Table 3.

Table 2: Test Matrix for R21-1-AI Anti-Islanding certification.

Test	R21-1-L/HVRT	R21-1-L/HFRT	R21-1-INV3	R21-1-VV11	R21-1-RR
1	X	X			
2	X	X	X		
3	X	X		X	
4	X	X	X		X
5	X	X		X	X

Table 3: Test Matrix for R21-1-AI Anti-Islanding certification with R21-3-FW21 Frequency-Watt.

Test	R21-1-L/HVRT	R21-1-L/HFRT	R21-1-INV3	R21-1-VV11	R21-1-RR	R21-3-FW21
1	X	X				X
2	X	X	X			X
3	X	X		X		X
4	X	X	X		X	X
5	X	X		X	X	X

1.1.1.5 Comments

An area EPS source means any source capable of maintaining an island within the recommended voltage and frequency window. An engine-generator with voltage and frequency control and without islanding protection can be considered an area EPS source for the purpose of this test. However, because of the uncertainty associated with the need to sink both real and reactive power from the DR, this test can be performed most conveniently with an area EPS connection, rather than a simulated area EPS.

Harmonic currents flow between the area EPS, the capacitor, and the DR, complicating the situation by making it appear that current is flowing when the fundamental frequency component of current has been reduced to zero. Thus it is important, when adjusting inductive and capacitive reactance, to use instruments that can display only the fundamental frequency component of current and power.

It is often advantageous to adjust the inductance first because that measurement is low in harmonics. The capacitance is added second so that the voltage is stable when the resistance is added. The resistive parallel load is then added and adjusted. Note that this resistance will be in addition to the resistance that will inherently be part of the inductive load.

The maximum recorded trip times may prove useful in area EPS system protection coordination studies and should be presented with other EUT product literature.

The worst-case parameter sets for the Rule 21 ride-through functions are when the operating and ride-through windows are maximized. There is no adjustability in the L/HVRT function described by the CPUC Electric Rule 21

Nov 14, 2014 draft, but there is a range of adjustability for L/HFRT. The worst-case settings for R21-1-L/HFRT are shown in Table 4.

Table 4: Settings for R21-1-L/HFRT during R21-1-AI Anti-Islanding testing.

System Frequency	Ride-Through Until (s)	Ride-Through Operational Mode	Trip Time (s)
$f > 64$	No Ride-Through	Not Applicable	0.16
$60.5 < f \leq 64$	299	Mandatory Operation	300
$58.5 < f \leq 60.5$	Indefinite	Continuous Operation	Not Applicable
$53.0 < f \leq 58.5$	299	Mandatory Operation	300
$f \leq 53.0$	No Ride-Through	Not Applicable	0.16

The worst-case parameter settings for Volt-Var functions such as R21-1-VV11 are most likely from a minimized deadband, e.g., max(V_2) and min(V_3), maximized var production, e.g., max(Q_1) and min(Q_4), and maximize the slope of the volt-var curve, e.g., max(V_1) and min(V_4). An example of these settings is shown in Figure 2.

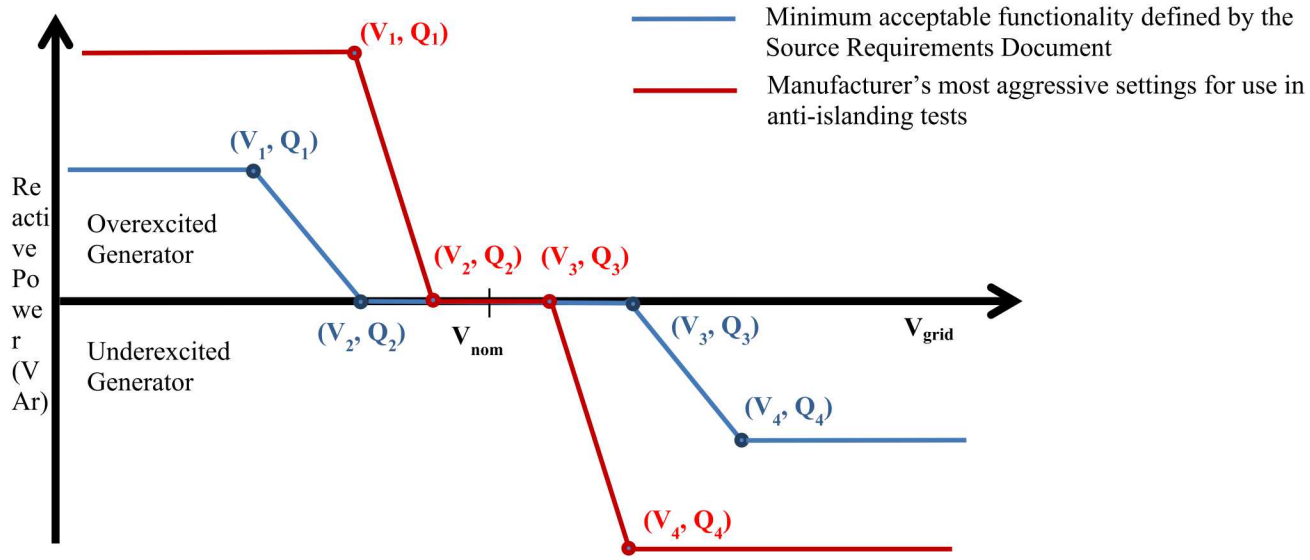


Figure 2: Example R21-1-VV11 settings for R21-1-AI anti-islanding certification.

The worst-case parameter settings[15] for Frequency-Watt functions such as R21-3-FW21 are most likely from a minimized HzStart, maximized WGra, hysteresis enabled and a minimized HzStop. An example of these settings is shown in Figure 3.

[15] Settings defined in IEC Technical Report IEC 61850-90-7, "Communication networks and systems for power utility automation–Part 90-7: Object models for power converters in distributed energy resources (DER) systems," Edition 1.0, Feb 2013.

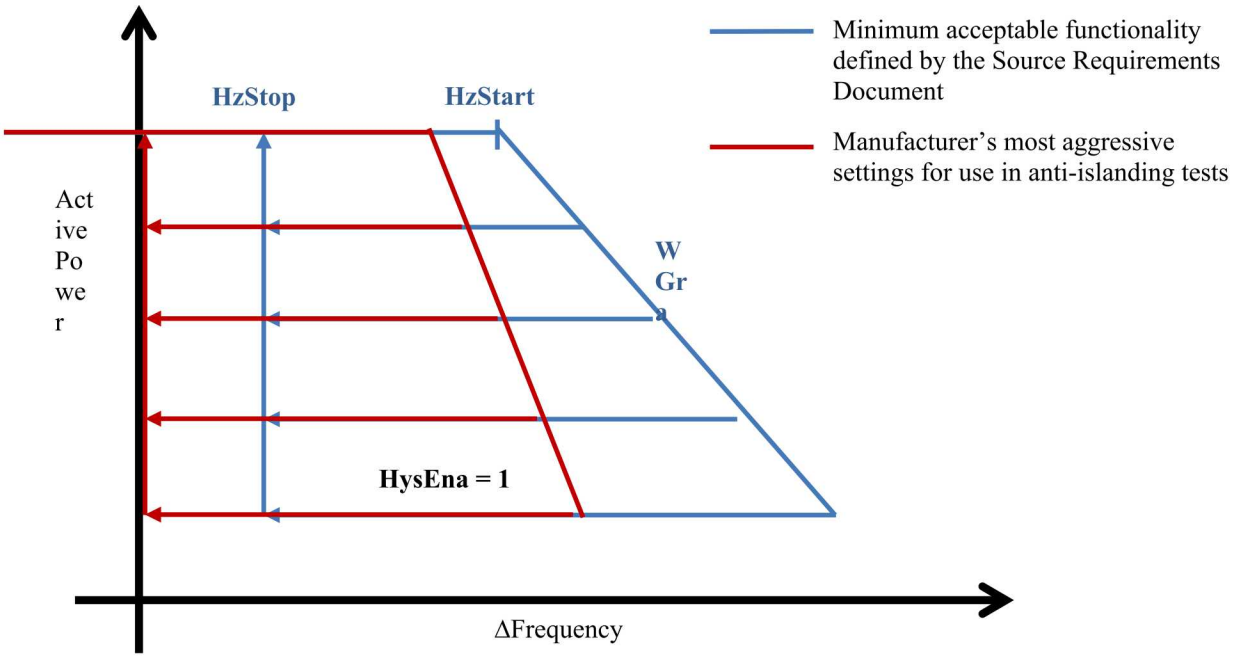


Figure 3: Example R21-3-FW21 settings for R21-1-AI anti-islanding certification.

Appendix 2 – R21-1-L/HVRT
Low and High Voltage Ride-Through
and
R21-1-L/HFRT
Low and High Frequency Ride-Through

Version 1.0 31 May 2014 – Copied from Sandia Test Protocols
Version 2.0 7 Oct 2014 – Harmonized with UL 1741 STP 0.3 draft and rev 3 MSC Diagrams Appendix
Version 2.1 25 Nov 2014 – CSI4 group edit for Rule 21
Version 3.0 1 Dec 2014 – Sandia National Labs Edit

Recommended UL Test Procedure for L/HVRT and L/HFRT

The CPUC Electric Rule 21 Nov 14, 2014 draft defines the R21-1-L/HVRT requirements according to Table 5 and the R21-1-L/HFRT requirements according to Table 6.

Table 5: Rule 21 L/HVRT.

Region	Voltage at PCC (% Nominal Voltage)	Ride-Through Until	Operating Mode	Maximum Trip Time (s)
High Voltage 2 (HV2)	$V \geq 120$			0.16 sec.
High Voltage 1 (HV1)	$110 < V < 120$	12 sec.	Momentary Cessation	13 sec.
Near Nominal (NN)	$88 \leq V \leq 110$	Indefinite	Continuous Operation	Not Applicable
Low Voltage 1 (LV1)	$70 \leq V < 88$	20 sec.	Mandatory Operation	21 sec.
Low Voltage 2 (LV2)	$50 \leq V < 70$	10 sec.	Mandatory Operation	11 sec.
Low Voltage 3 (LV3)	$V < 50$	1 sec.	Momentary Cessation	1.5 sec.

Table 6: Rule 21 L/HFRT.

Region	System Frequency Default Settings	Minimum Range of Adjustability (Hz)	Ride-Through Until (s)	Ride-Through Operational Mode	Trip Time (s)
High Frequency 2 (HF2)	$f > 62$	62.0 – 64.0	No Ride-Through	Not Applicable	0.16
High Frequency 1 (HF1)	$60.5 < f \leq 62$	60.1 – 62.0	299	Mandatory Operation	300
Near Nominal (NN)	$58.5 < f \leq 60.5$	Not Applicable	Indefinite	Continuous Operation	Not Applicable
Low Frequency 1 (LF1)	$57.0 < f \leq 58.5$	57.0 – 59.9	299	Mandatory Operation	300
Low Frequency 2 (LF2)	$f \leq 57.0$	53.0 – 57.0	No Ride-Through	Not Applicable	0.16

2.1. Function L/HVRT – Low and High Voltage Ride-Through

2.1.1 Purpose

The purpose of this test is to verify the behavior of the DER system in response to low and high voltage excursions which are outside the normal range of operation of the area EPS. The test verifies behavior of the DER in *ride-through* and *must trip* regions. For EUT without ride-through regions, use the UL 1741 Ed. 2/IEEE 1547.1-2005 procedure. Note that the ride-through behavior can either be *Momentary Cessation*[16], where the EUT does not export power, or *Mandatory Operation*, where the EUT must continue to export power. An example of voltage and frequency ride-though and must trip regions are shown in Figure 4 and Figure 5 for Rule 21.

[16] Also known as gate-blocking in some regions.

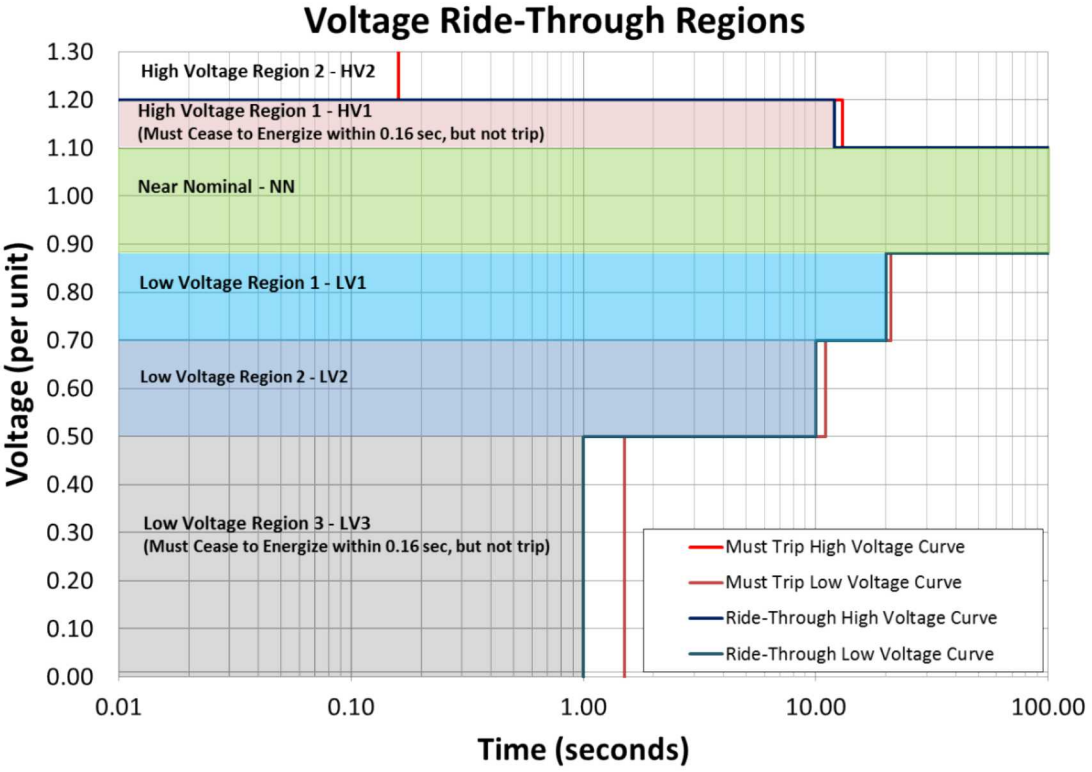


Figure 4: Rule 21 Ride-Through and Must Trip Regions in the Time-Voltage Domain.

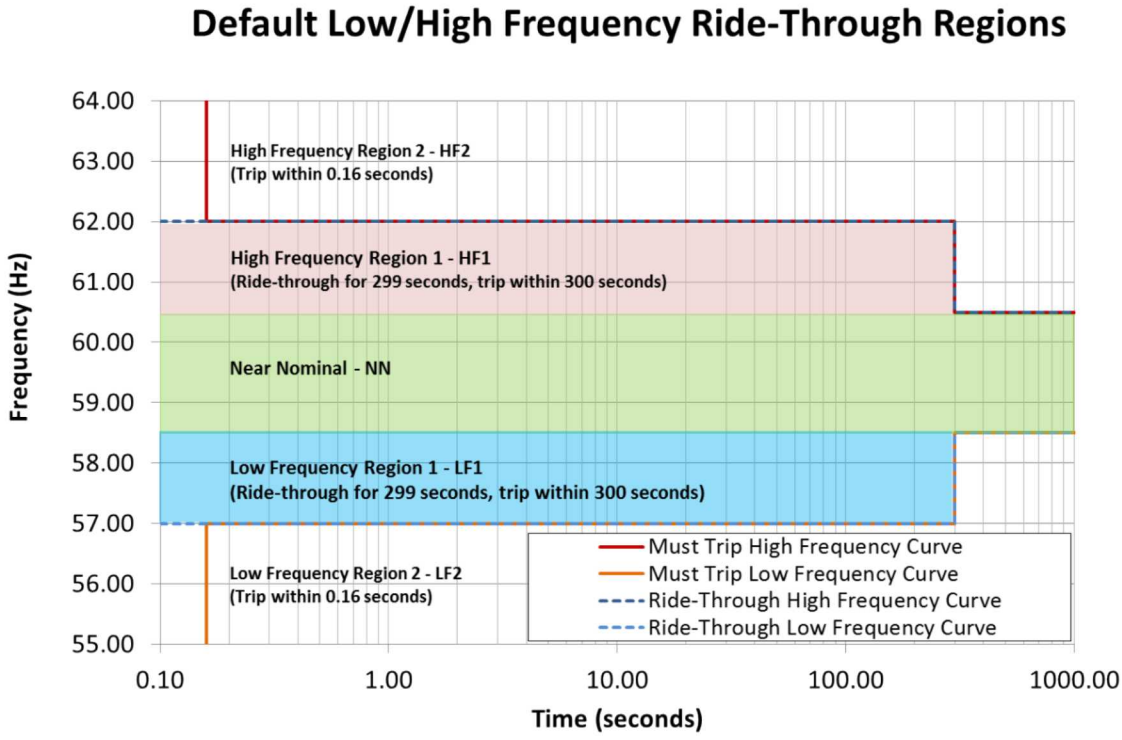
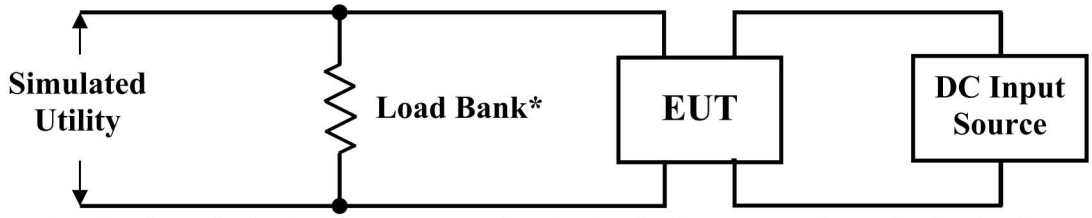


Figure 5: Rule 21 Default Ride-Through and Must Trip Regions in the Time-Frequency Domain.

2.1.2 Requirements

The test circuit for the low/high voltage ride-though magnitude and duration tests is shown in Figure 5. The simulated area EPS shall meet the requirements of IEEE 1547.1, Section 4.6.1. The measurement system shall meet the requirements of IEEE 1547.1, Section 4.6.2. The input source shall be capable of supplying 200% of the rated current of the EUT in accordance with UL 1741, Section 47.2.4



*Note: Load bank required only for non-regenerative simulated utilty sources. Some simulated utilty sources are unidirectional sources and therefore require a load bank to absorb the real and reactive power produced by the EUT during testing.

Figure 5: L/HVRT Test Circuit.

2.1.3 Voltage and Frequency Tests – Ride-Through Procedure

a) Record the trip voltage (magnitude) and time (duration) limits for each over voltage and under voltage operating region from the applicable requirements document. (See appendix 2A.)[17]
b) Determine and record the applicable EUT control parameters for each over voltage and under voltage region. (See appendix 2A.)
c) Record manufacturer's stated accuracy for ac voltage (magnitude) and time (duration) measurements for each over voltage and under voltage region. (See appendix 2A.)

These tests shall be performed at the terminals of the EUT. The tests shall be performed at full rated current and 10% rated operating current. Signal injection test methods shall not be used.

The test results obtained in R21-1-AI in Appendix 1 may be used to determine compliance with must trip requirements. However, if the EUT disconnects outside the tolerance of the must trip setting, then the must trip behavior must be verified by the separate ride-through test.

The ride-through behavior of the EUT shall be evaluated[18] using the following tests:

a) Ride-Through Magnitude and Duration, Section 2.1.3.1.
b) Must Trip Magnitude and Duration, Section 2.1.3.2.

2.1.3.1 Ride-Through Magnitude and Duration

[17] This testing procedure assumes that the regions do not contain any non-rectangular regions (e.g., the mandatory operation and must trip curves do not contain sloped lines). In the event, that a jurisdiction has a non-rectangular testing region, an alternative testing method will be required.
[18] If the EUT does not have the L/HVRT or L/HFRT capability, e.g., only the must trip curves, the UL 1741, Ed. 2 protocol shall be used.

a) Connect the EUT according to the instructions and specifications provided by the manufacturer.

b) Set all parameters for the DC input source to the nominal operating conditions for the EUT. The

c) Set (or verify) all EUT parameters to the default operating settings.

If the must ride-through setting is adjustable, set the EUT to the tightest[19] must ride-through setting, but no less than the nominal voltage/frequency plus twice the manufacturer's stated accuracy.

d) For over voltage/frequency tests:

i. Set the duration of the over voltage/frequency ride-through step function, t_e, to a value which is at the maximum duration specified in the first region of the Source Requirements Document[20] minus 1 times the manufacturers stated time accuracy.

ii. Set the voltage/frequency magnitude, P_T, of the voltage/frequency ride-through step function to maximum magnitude specified in the first region of the Source Requirements Document minus 1 times the manufacturers stated voltage/frequency accuracy.

For under voltage/frequency tests:

i. Set the duration of the over voltage/frequency ride-through step function, t_e, to a value which is at the maximum duration specified in the first region of the Source Requirements Document minus 1 times the manufacturers stated time accuracy.

ii. Set the voltage/frequency magnitude, P_T, of the voltage/frequency ride-through step function to minimum specified in the first region of the Source Requirements Document plus 1 times the manufacturers stated voltage/frequency accuracy.

e) Record applicable settings.

f) For single-phase units, adjust voltage/frequency of the simulated utility to starting point P_n, as defined in Annex 2A. The simulated utility source shall be held at this voltage/frequency for period of not less than t_d with t_r and t_d values less than 1 cycle. At the end of this period, initiate the step ride-through function specified in Annex 2A.

For multiphase units, adjust voltage on one phase of the simulated utility to the starting point P_n. The simulated utility source shall be held at this voltage for period of not less than t_d with t_r and t_d values less than 1 cycle. At the end of this period, initiate the step ride-through function specified in Annex 2A. Ensure that remaining phases are held at nominal.

For over voltage/frequency tests:

i. In Annex 2A, P_n shall be the minimum NN grid voltage/frequency magnitude plus the manufacturers stated voltage/frequency accuracy[21].

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[19] The *tightest* ride-through settings minimize the size of the over voltage and under voltage regions. The *widest* ride-through settings maximize the size of the over voltage and under voltage regions.

[20] The Source Requirements Document will depend on the jurisdiction. For example, interconnecting to the CA IOU EPS requires compliance with the Electric Rule 21 Requirements Document.

[21] This verifies the magnitude of the NN range and maximizes the voltage/frequency change during the test, which could result in unwanted tripping of the device to different internal safety functions, e.g., over current protection.

For under voltage/frequency tests:

i. In Annex 2A, P_n shall be the maximum NN grid voltage/frequency magnitude minus the manufacturers stated voltage/frequency accuracy[21].

g) Record all voltage magnitudes, rise times, fall times, hold times and dwell times of the ride-through step function.

h) Repeat steps f) through g) four times for a total of N_r = five repetitions.

i) Repeat steps d) through h) for each of the remaining over/under voltage/frequency regions.

j) If the ride-through curve settings are configurable, repeat steps d) through i) at the widest range of the adjustment and at mid-way between the tightest and widest settings.

During the above procedure, the settings of parameters for other functions, or voltage/frequency parameters for other voltage/frequency regions, shall be set so as not to influence the test results for the operating region being evaluated, or shall be disabled.

2.1.3.2 Must Trip Magnitude and Duration

The Must Trip curves for R21-1-L/HVRT and R21-1-L/HFRT are verified with the following procedure:

1. Disable all other advanced inverter functions, so they not to influence the test results for the operating region being evaluated.

2. Turn the momentary cessation option off for all regions.[22]

3. If the must trip curve settings are configurable, perform the IEEE 1547.1-2005 procedure at the tightest range of the adjustment.

4. Perform the must trip tests in accordance with IEEE 1547.1-2005 Section 5.2 *Test for response to abnormal voltage conditions* or Section 5.3 *Response to abnormal frequency conditions*, as referenced in UL 1741, Ed 2, Section 40 *Utility Interaction*.

5. If the must trip curve settings are configurable, repeat Step 4 at the middle and widest range of the adjustment.

2.1.3.4 Criteria

Each region shall have the applicable ride-through and must trip magnitudes verified[23]. For the ride-through magnitude tests with momentary cessation, the EUT must return to service using the *normal ramp rate* setting[24]. In the case of the must-trip tests, the EUT must trip, reconnect using the standard reconnection time, and ramp up using the *soft start ramp rate*[25].

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[22] In the event that the momentary cessation capabilities cannot be deactivated, the manufacturer shall provide a signal to indicate when a trip has occurred.
[23] In the case of Rule 21 L/HVRT, five must trip magnitudes will be verified: the upper bound of NN, upper bound HV1, the lower bound of NN, the lower bound of LV1, and the lower bound of LV2. Four ride-through magnitudes will be verified: the upper bound of HV1, lower bound of LV1, lower bound of LV2, and lower bound of LV3.
[24] Default value defined to be 100% of maximum current per second in Rule 21.

The required behavior of the EUT, e.g., ceasing to energize or mandatory operation, shall also be verified for all ride-through regions. For mandatory operation regions, the EUT shall be considered in compliance if it provides an average current greater than or equal to 90% of the pre-disturbance current during the ride-through event in each of the voltage ranges specified in the Source Requirements Document, and returns to the pre-disturbance current level within the time specified in the Source Requirements Document. For momentary cessation regions, the EUT shall be considered in compliance if it provides an average current less than or equal to 10% of the EUT rated current during the ride-through event in each of the voltage ranges specified in the Source Requirements Document, and returns to the pre-disturbance current level within the time specified in the Source Requirements Document. Where adjustable set points are used, the EUT shall be considered in compliance if it continues to energize the utility within the programmed setting +/- manufacturer's stated accuracy.

2.1.3.5 Comments

The test results from the R21-1-RR are used to verify the return to service behavior of the EUT.

[25] Default value defined to be 2% of maximum current output per second in Rule 21.

Annex 2A Ride-Through Test Signal (Step Function)

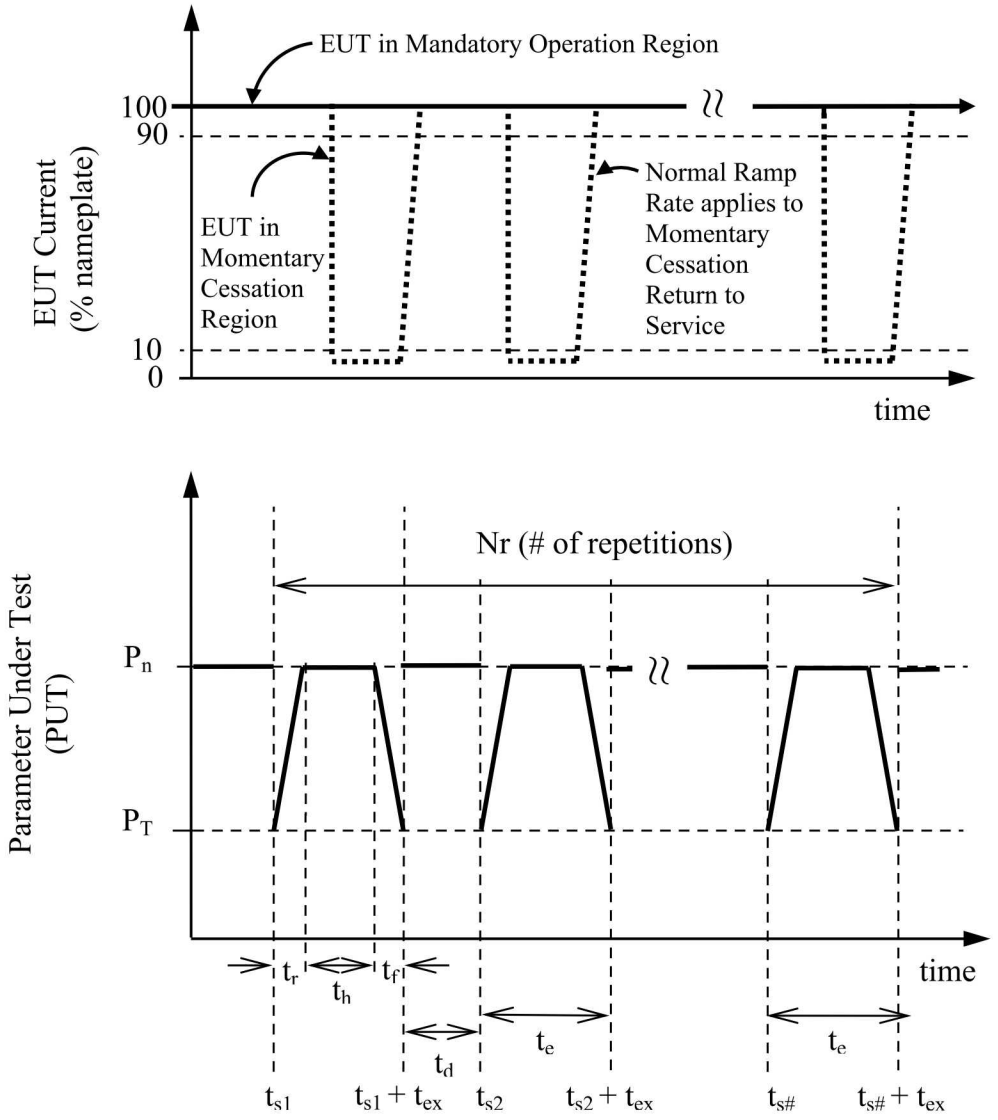


Figure A.1 – Graphical representation of the ride-through test step function.

The test signal described in this subclause is used to characterize the behavior of the EUT during ride-through events.

Vary the PUT according to the magnitude step function envelope defined herein. Only the PUT shall be varied. Therefore, all other parameters shall be held at default values. The ride-through test signal shall take the form described in Equation (A.1).

Equation A.1: $P(t) = A \times u(t_h) + P_n$

where:

P is the magnitude of the PUT
t_h is hold time (s)
t_{ex} is the total excursion time (s) of the PUT ($t_{ex} = t_r + t_h + t_r$)

t_r is rise time (s)[26]
t_f is fall time (s)[25]
t_d is dwell time (s) between pulses as specified by manufacturer
$t_{s\#}$ is the start time of the # repetition used for calculating the response time
N_r is the number of pulse repetitions per test sequence

A is a signed scaling factor

$u(t)$ is the unit step function,
P_n is the starting point of the step function (in units of the PUT)

[26] Rise and fall times are intended to be rapid to simulate an abnormal operating condition on the area EPS, i.e. a fault. When the rapid rise or fall times conflict with a design characteristic or settings of the EUT, longer rise and fall times agreeable to the manufacturer and the testing agency may be used. The rise time t_r and fall times t_f shall be less than the larger of 1 cycle or 1% of the time-delay setting of the PUT.

Annex 2B Definitions

Cease to Energize – In response to an abnormal excursion of the area EPS the DER shall, with no intentional delay, cease to provide real and reactive current to the area EPS in not more than the maximum specified time. Note: Cease to energize does not imply galvanic separation or a trip of the DER.

DER – Distributed Energy Resource. (Typically a PV inverter)

Mandatory Operation – In response to an abnormal excursion of the area EPS the DER shall provide maximum available real and reactive current to the area EPS. Note: Any protective functions needed to prevent damage to the DER shall be permitted during mandatory operation.

Momentary Cessation – In response to an abnormal excursion of the area EPS the DER shall, with no intentional delay, cease to provide real and reactive current to the area EPS in not more than the maximum specified time. If conditions on the area EPS return to a defined acceptable magnitude within the defined ride-through duration the DER shall, with no intentional delay,

Normal Operation – While the area EPS is within normal parameters the DER unit shall operate normally and provide maximum available real and reactive power to the area EPS.

Permissive Operation – In response to an abnormal excursion of the area EPS the DER may continue to provide real and reactive current to the area EPS or may cease to energize.

Ride-Through - In response to an abnormal excursion of the area EPS the DER may provide maximum available real and reactive current to the area EPS or, may cease to energize the area EPS, for not less than the minimum specified duration. During ride-through the DER shall not trip in less than that the minimum specified duration.

Return to Service – The criteria required for and behavior of the DER as it re-energizes the area EPS following an abnormal excursion resulting in a trip or ride-through operation of the DER.

Trip – In response to an abnormal excursion of the area EPS the DER shall cease to energize, or disconnect from, the area EPS. Following a trip, the DER must delay re-energizing the area EPS until the area EPS has returned to a normal operating condition for not less than the minimum specified time as specified in the return to service criteria.

Appendix 3 – R21-1-RR
Normal Ramp Rate
and
R21-1-SS
Soft-Start Ramp Rate

Version 1.0 31 May 2014 – Original Version from Sandia Test Protocols
Version 1.1 7 Oct 2014 – Minor changes.
Version 1.2 8 Dec 2014 – EPRI edits

Recommended UL Test Procedure for Ramp Rate Capabilities

This test confirms that an inverter meets a given response characteristic for providing ramp rate responses for normal and/or soft-start ramp rate commands.

DER can ramp the rate of increasing and/or decreasing their power output. These ramp rates are constrained by what the I-DER systems can physically do. For instance, if they are outputting their maximum power, they can ramp down but cannot ramp up, while a completely charged storage system may ramp up (discharge power into the Area EPS) but cannot ramp down.

3.1 Purpose

The purpose of establishing ramp-up and ramp-down rates for DER systems is to help smooth transitions from one output level to another output level. Although a single DER system might not impact the grid through a single sharp transition, aggregated DER systems responding to a specific event could cause significant rapid jumps in overall output if they do not ramp to the new level. Such sharp transitions could cause power quality issues such as voltage spikes or dips, harmonics, or oscillations.

Multiple ramp rates characteristics are possible for inverters. This test verifies two types of ramp rates, although they may optionally be implemented as one general ramp rate. Manufacturers must indicate the following types of ramp rates provided in their products during certification testing:

- Normal ramp rate (up and down) when the inverter is adjusting the output power, e.g., when a PV inverter is following the available power from the dc source.
- Soft-start ramp rate (up and down) which defines the behavior of the device to ramp from zero to operating power.

Ramp rates are expressed as a percentage of nameplate power per second. There can be a generic ramp rate for all cases, i.e., "normal ramp rate" and "soft-start ramp rate" or each of these could be defined individually. Similarly, the ramp-up and the ramp-down values for each of these may be defined independently or as a combined value.[27]

These ramp rate tests verify the performance of a single inverter when connected to an area EPS.

3.2 Procedure for Normal Ramp Rate Test

The manufacturer will state the following parameters of the EUT:

- Apparent Power Rating (VA) –S_{rated}
- Input Power Rating (W) – P_{rated}
- Minimum normal ramp rate up (%P_{rated}/sec) – $RR_{norm\_up\_max}$.[28]
- Maximum normal ramp rate up (%P_{rated}/sec) – $RR_{norm\_up\_min}$.[29]
- Minimum normal ramp rate down (%P_{rated}/sec) – $RR_{norm\_down\_max}$.
- Maximum normal ramp rate down (%P_{rated}/sec) – $RR_{norm\_down\_min}$.
- Active power range of function, i.e., 5- 100%.
- Ramp Rate Accuracy, RRA (%P_{rated}/sec)

[27] While the original IOU filing defined a soft disconnect ramp-down rate, this was removed by the CPUC in the 13 Nov, 2014 filing after the comment period. Both the soft start and the

[28] Ramp rates may be encoded as a single normal ramp rate, RR_{norm_max}.

[29] Ramp rates may be encoded as a single normal ramp rate, RR_{norm_min}.

Table 7: Normal Ramp Rate Test Parameters.

Test	Independent Normal Up and Down Ramp Rates		Single Normal Ramp Rate or a Single Generic Ramp Rate
	Up Ramp Rate RR_{norm_up} (% nameplate watts/sec)	Down Ramp Rate RR_{norm_down} (% nameplate watts/sec)	Ramp Rate RR_{norm} or RR (% nameplate watts/sec)
1	0 (Disabled)	0 (Disabled)	0 (Disabled)
2	$RR_{norm\_up\_min}$	$RR_{norm\_down\_min}$	RR_{norm_min}
3	$(RR_{norm\_up\_min} + RR_{norm\_up\_max})/2$	$(RR_{norm\_down\_min} + RR_{norm\_down\_max})/2$	$(RR_{norm\_min} + RR_{norm\_max})/2$
4	$RR_{norm\_up\_max}$	$RR_{norm\_down\_max}$	RR_{norm_max}
5[30]	$RR_{norm\_up\_max}$	$RR_{norm\_down\_min}$	N/A

The ramp rate test shall be carried out as follows:

1. Connect the EUT according to the Requirements in Sec. 3.2.1 and specifications provided by the manufacturer.

2. Set all AC source parameters to the nominal operating conditions for the EUT.

3. Set the DC source power level to provide nameplate AC power output from the EUT.

4. Turn on the EUT. Allow the inverter to reach steady state, e.g., maximum power point.

5. Set the EUT ramp rate parameters according to Test 1 in Table 7. If the EUT has RR_{norm_up} and RR_{norm_up}, the "Independent Normal Up and Down Ramp Rates" are used; if the EUT has a single RR_{norm}, the "Single Normal Ramp Rate or a Single Generic Ramp Rate" is used.

6. Begin recording the time domain response of the EUT AC voltage and current, and DC voltage and current.

7. Reduce the available DC power to the EUT according to the step function described in Annex 3A.

8. Stop recording the time domain response after the ramp duration plus a manufacturer-specified dwell time. Ramp duration is defined as $1/RR_{norm}$, or $1/RR_{norm\_up}$ as appropriate for the test settings.

9. Begin recording the time domain response of the EUT AC voltage and current, and DC voltage and current.

10. Increase the available DC power to the EUT according to the step function described in Annex 3A.

11. Stop recording the time domain response after the ramp duration plus a manufacturer-specified dwell time. Ramp duration is defined as $1/RR_{norm}$ or $1/_{RRnorm\_down}$ as appropriate for the test settings.

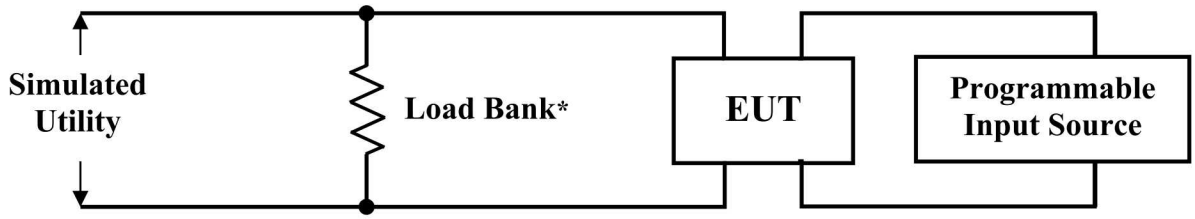
12. Repeat steps 6-11 four times for a total of 5 repetitions.

13. Repeat steps 4-12 for Tests 2-5 in Table 7.

[30] Test 5 verifies that the independent normal ramp rates are independent and associated correctly.

3.2.1 Requirements

Inverter shall be connected into a test circuit similar to that shown in Figure 6.



* Note: Load bank required only for non-regenerative simulated utility sources. Some simulated utility sources are unidirectional sources and therefore require a load bank to absorb the real and reactive power produced by the EUT during testing.

Figure 6: R21-1-RR Test Circuit.

Time domain current and voltages shall be sampled at rate above 1000 samples/sec.

3.2.2 Criteria

For each of the recorded time domain responses for the down-ramps, the EUT shall not exit a region defined by the ramp rate setting +/- stated ramp rate accuracy.

For each of the recorded time domain responses for the up-ramps, the EUT shall not exceed the ramp rate setting plus stated ramp rate accuracy.[31]

[31] The lower bound for the up-ramp is not enforced because the EUT behavior will depend on the MPPT algorithm.

3.3 Procedure for Soft-Start Ramp Rate Test

The manufacturer will state the following parameters of the EUT:

- Apparent Power Rating (VA) –S_{rated}
- Input Power Rating (W) – P_{rated}
- Minimum soft start ramp rate up (%P_{rated}/sec) – RR_{SS_max}.
- Maximum soft start ramp rate up (%P_{rated}/sec) – RR_{SS_min}.
- Active power range of function, i.e., 5- 100%.
- Ramp Rate Accuracy (%P_{rated}/sec).

Table 8: Soft-Start Ramp Rate Test Parameters.

Test	**Soft-Start Ramp Rate[32]** RR_{ss} (%P_{rated}/sec)
1	0 (Disabled)
2	RR_{SS_min}
3	$(RR_{SS\_min} + RR_{SS\_max})/2$
4	RR_{SS_max}

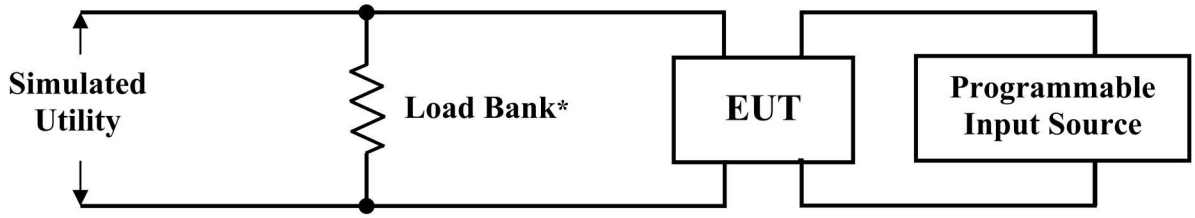
The commanded power factor test shall be carried out as follows:

1. Connect the EUT according to the Requirements in Sec. 3.3.1 and specifications provided by the manufacturer.
2. Set all AC source parameters to the nominal operating conditions for the EUT.
3. Set the DC source power level to provide nameplate AC power output from the EUT.
4. Turn on the EUT. Set the EUT ramp rate parameters according to Test 1 in Table 8.
5. Shut down the inverter by setting the DC source power level to zero.
6. Begin recording the time domain response of the EUT AC voltage and current, and DC voltage and current.
7. Step the DC source power to 120% of the nameplate DC power output of the EUT.
8. Stop recording the time domain response after the ramp duration plus a manufacturer-specified dwell time. Ramp duration is defined as 1/RR or 1/RR_{ss} as appropriate.
9. Repeat steps 5-8 for a total of 3 repetitions.
10. Repeat steps 4-9 for Tests 2-4 in Table 8.

[32] Range from 1-100% is from J.T. Sullivan, CPUC Rulemaking11-09-011 Agenda ID #13460, 13 Nov, 2014.

3.3.1 Requirements

Inverter shall be connected into a test circuit similar to that shown in Figure 7.



* Note: Load bank required only for non-regenerative simulated utility sources. Some simulated utility sources are unidirectional sources and therefore require a load bank to absorb the real and reactive power produced by the EUT during testing.

Figure 7: R21-1-RR Test Circuit.

Time domain current and voltages shall be sampled at rate above 1000 samples/sec.

3.3.2 Criteria

For each of the recorded time domain responses, the EUT shall not exceed the ramp rate plus stated ramp rate accuracy.[33]

[33] The lower bound for the up-ramp is not enforced because the EUT behavior will depend on the MPPT algorithm.

Annex 3A Ramp Rate Test Profiles

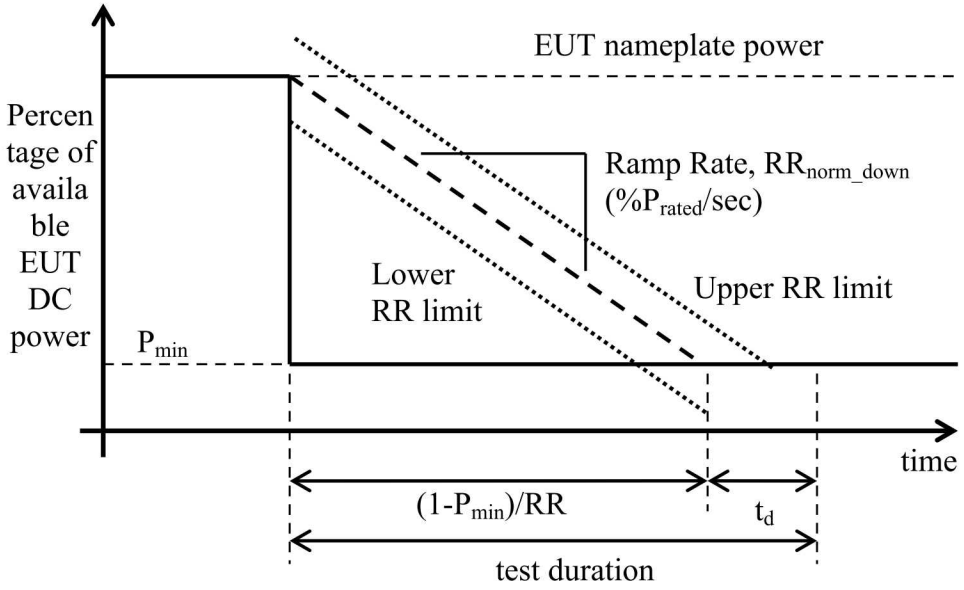


Figure 3A.1 – Graphical representation of the normal 'down' ramp rate test step function

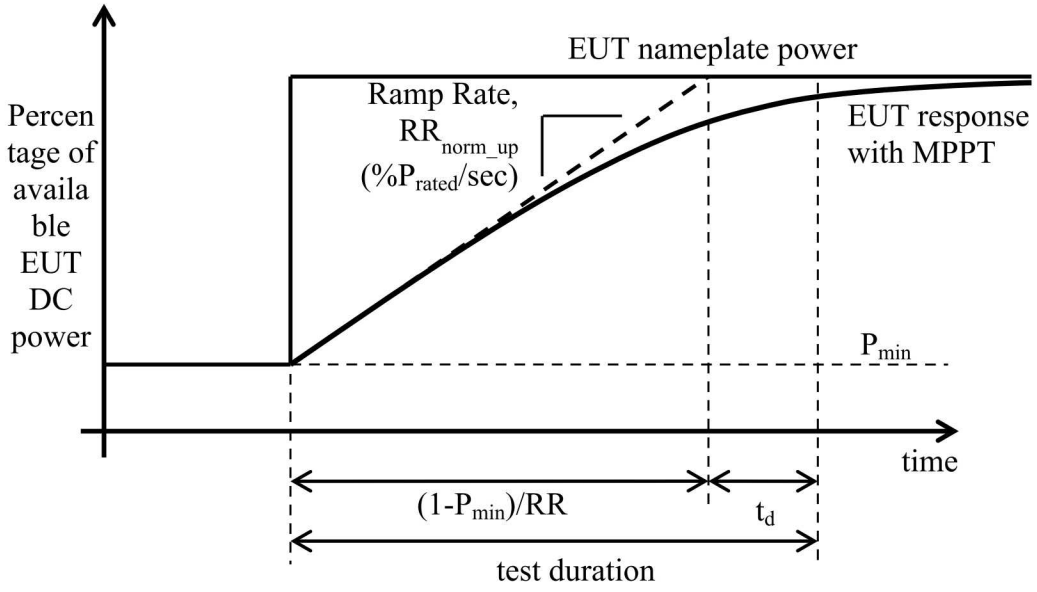


Figure 3A.2 – Graphical representation of the normal 'up' ramp rate test step function

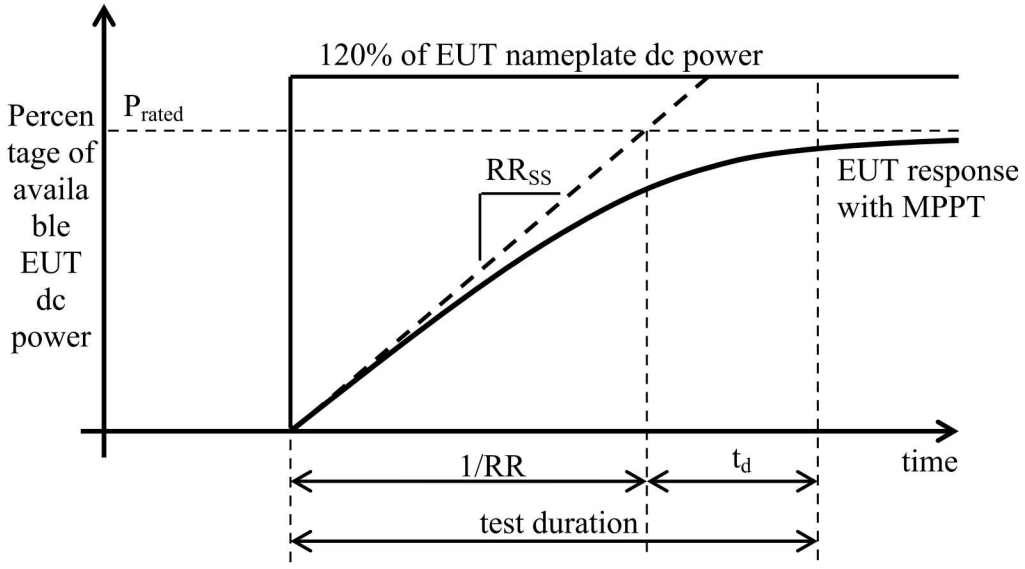


Figure 3A.3 – Graphical representation of the soft start ramp rate test step function

td is dwell time (s) between tests as specified by manufacturer

P_{min} is the minimum active power range of ramp rate function ($\%P_{limit}$)

RR is the ramp rate ($\%P_{rated}$/sec)

Upper RR limit, is the defined by a curve offset above the target RR, from the beginning of the test until the EUT reaches the P_{min}, by the following:

Upper RR limit offset ($\%P_{limit}$) = [(1-P_{min})/RR]* RRA

Lower RR limit, is the defined by a curve offset below the target RR, from the beginning of the test until the EUT reaches the P_{min}, by the following:

Lower RR limit offset ($\%P_{limit}$) = [(1-P_{min})/RR]* RRA

Appendix 4 – R21-1-INV3
Fixed Power Factor
and
RS21-1-VV11
Volt/Var Mode

Version 1.0 31 May 2014 – Original Version from Sandia Test Protocols
Version 2.0 7 Oct 2014 – Harmonized with the UL 1741 STP recommendations
Version 2.1 4 Dec 2014 – Sandia/CSI4 group edits
Version 2.2 8 Dec 2014 – EPRI edits

Draft UL Test Procedure for Reactive Power Capabilities of Inverters

This test confirms that an inverter meets the required response characteristics for providing reactive power in response to volt-VAr and power factor commands.

4.1 Purpose

Multiple methods of providing reactive power are possible for inverters. This test verifies two categories: fixed power factor and reactive power as function of voltage, i.e., Q(V).

Inverters can be set to prioritize reactive or real power production with Volt-VAr functions. This priority setting defines the inverter's behavior when the inverter reaches its kVA limits. When an inverter is set to real power priority and the inverter's kVA limit is reached, reactive power is reduced to maximize real power production. When an inverter is set to reactive power priority and the inverter's kVA limit is reached, real power is reduced to maintain reactive power production.

These reactive power tests verify the performance of a single inverter when connected to an area EPS. Performance of multi-inverter testing is beyond the scope of this test. These tests verify the inverter's dynamic response, but do not address the voltage stability of the Area EPS.

4.2 Procedure for Commanded Power Factor Test

The manufacturer will state the following parameters of the EUT:

- Apparent Power Rating (VA) –S_{rated}
- EUT Input Power Rating (W) – P_{rated}
- DC voltage range with function enabled (V)
- Nominal DC voltage (V)
- AC voltage range with function enabled (V)
- AC voltage accuracy (V) – MSA_{Vac}
- DC voltage accuracy (V) – MSA_{Vdc}
- Active power range of function[34], i.e., 20- 100%.
- Power Factor Accuracy
- Power Factor Settling Time (s)
- Minimum Inductive (Underecited) Power Factor[35] – $PF_{min,ind}$
- Minimum Capacitive (Overexcited) Power Factor – $PF_{min,cap}$

Additionally, the following parameters will be defined:

- PF, the inductive or capacitive signed power factor commanded for test.
- $PF_{mid,cap} = (1 - PF_{min,cap})/2$, half the EUT capacitive range.
- $PF_{mid,ind} = (-1 - PF_{min,ind})/2$, half the EUT inductive range.
- P_{limit}, the maximum output power either limited by the input supply or by a command to the inverter.

---

[34] At a certain low input power level, the EUT may be unable to accurately produce a fixed power factor.

[35] This test follows the IEEE Std-1459-2000 reactive power sign convention, in which a leading, capacitive, overexcited power factor is positive and a lagging, inductive, underexcited power factor is negative.

Table 9: R21-1-INV3 Test Parameters.

Test #	PF command
1	1
2	$PF_{min,ind}$
3	$PF_{mid,ind}$
4	$PF_{min,cap}$
5	$PF_{mid,cap}$

The commanded power factor test shall be carried out as follows:

1. Connect the EUT according to the Requirements in Sec. 4.2.1 and specifications provided by the manufacturer.

2. Set all AC source parameters to the nominal operating conditions for the EUT. Frequency is held at nominal throughout this test. Set the input power to P_{rated}.

3. Turn on the EUT. Set all R21-1-L/HVRT parameters to the widest range of adjustability possible with the R21-1-INV3 enabled.[36]

4. If the EUT has the ability to set 'Real Power Priority' or 'Reactive Power Priority', select 'Reactive Power Priority'.

5. Set the EUT power factor to unity.

6. Begin recording the time domain response of the EUT AC voltage and current, and DC voltage and current. Set the EUT power factor to the value in Test 1 in Table 9. Stop recording the time domain response after twice the settling time.

7. Repeat Steps 5-6 for four additional times for a total of 5 repetitions.

8. Repeat Steps 5-7 for Tests 2-5 in Table 9.

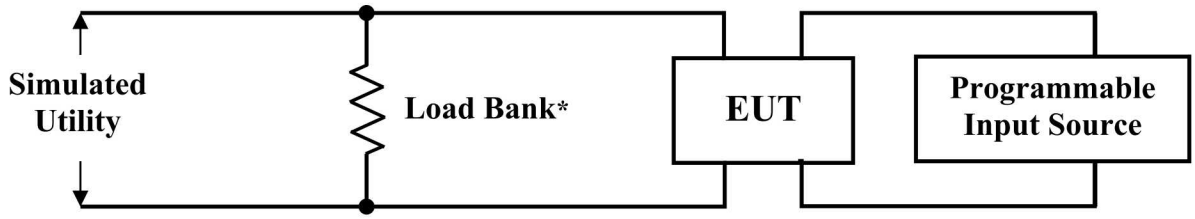
9. Repeat Steps 5-8 for P_{limit} values of 20% and 60% of P_{rated} by reducing the DC voltage of the Input Source.

10. In the case of bi-directional inverters, repeat Steps 5-8 for the second real power flow direction.

4.2.1 Requirements

Inverter shall be connected into a test circuit similar to that shown in Figure 8.

[36] The EUT's range of disconnect settings may depend on which function(s) are enabled.



* Note: Load bank required only for non-regenerative simulated utility sources. Some simulated utility sources are unidirectional sources and therefore require a load bank to absorb the real and reactive power produced by the EUT during testing.

Figure 8: R21-1-INV3 and R21-1-VV11 Test Circuit.

The simulated area EPS shall meet the requirements of clause 4.6.1 of IEEE Std 1547.1. The measurement system shall meet the requirements of clause 4.6.2 of IEEE Std 1547.1. These tests shall be performed at the terminals of the EUT.

For three phase inverter test, the simulated EPS voltage in these tests is balanced meaning each phase has the same magnitude and phases are separated by 120 degrees. For single-phase tests the voltage under consideration is the RMS voltage at the inverter terminals. Time domain current and voltages shall be sampled at rate above 1000 samples/sec.

4.2.2 Criteria

For each of the recorded time domain responses, the EUT shall move to within stated accuracy of the command power factor within the power factor settling time.

4.3 Procedure for Volt-Var "Q(V)" Test

The manufacturer will state the following parameters of the EUT:

- Apparent Power Rating (VA) –S_{rated}
- Input Power Rating (W) – P_{rated}
- DC voltage range with function enabled (V)
- AC voltage range with function enabled (V) – [$V_{min,}$ V_{max}]
- Active power range of function, i.e., 20- 100%
- Reactive Power Accuracy (% or VAr)
- Maximum Ramp Rate (VAr/s)
- Maximum Capacitive Reactive Power[37] – $Q_{max,ind}$
- Maximum Inductive Reactive Power – $Q_{max,cap}$
- Maximum Slope (VAr/V) –K_{VARmax}
- Deadband Range (V) – [$Deadband_{min}$, $Deadband_{max}$]

In the R21-1-VV11 tests, the Volt-VAr curve will be defined by four pointwise pairs (V, Q) as described in IEC TR 61850-90-7[38].

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[37] This test follows the IEEE Std-1459-2000 reactive power sign convention, in which a leading, capacitive, overexcited power factor is positive and a lagging, inductive, underexcited power factor is negative.

[38] International Electrotechnical Commission Technical Report IEC 61850-90-7, "Communication networks and

- Q_1 = the maximum capacitive reactive power setting
- Q_2 = the reactive power settingat the left edge of the deadband
- Q_3 = the reactive power setting at the right edge of the deadband
- Q_4 = the maximum inductive reactive power setting
- V_1 = the voltage at Q_1
- V_2 = the voltage at Q_2 V_3 = the voltage at Q_3
- V_4 = the voltage at Q_4

The following parameters will be calculated:

- $Q_{min,cap}$, = Minimum capacitive reactive power setting for Characteristic Curve 3, specified by the Source Requirements Document[39] or $Q_{max,cap}/4$
- $Q_{min,ind}$, = Minimum inductive reactive power setting for Characteristic Curve 3, specified by the Source Requirements Document or $Q_{max,ind}/4$
- $V_{avg} = (V_{min}+V_{max})/2$
- $K_{VARavg} = Q_{max,cap}/(2\cdot(Deadband_{avg}/2 – V_{avg}))$
- $K_{VARmin} = Q_{max,cap}/(4\cdot(Deadband_{max}/2 - V_{min}))$ or as specified by the Source Requirements Document
- $Deadband_{avg} = (Deadband_{max} + Deadband_{min})/2$

Table 10: R21-1-VV11 Test Parameters.

Test	Characteristic Curve	Volt/Var [V,Q] Array			
1	Characteristic 1 “Most Aggressive” Curve (Figure 9)	V1	$Q_1/K_{VARmax} + V_2$	Q1	$Q_{max,cap}$
		V2	$V_{nom} - Deadband_{min}/2$	Q2	0
		V3	$V_{nom} + Deadband_{min}/2$	Q3	0
		V4	$Q_4/K_{VARmax} + V_3$	Q4	$Q_{max,ind}$
2	Characteristic 2 “Average” Curve (Figure 10)	V1	$Q_1 /K_{VARavg} + V_2$	Q1	$0.50*Q_{max,cap}$
		V2	$V_{nom} - Deadband_{avg}/2$	Q2	0
		V3	$V_{nom} + Deadband_{avg}/2$	Q3	0
		V4	$Q_4 /K_{VARavg} + V_3$	Q4	$0.50*Q_{max,ind}$
3	Characteristic 3 “Least Aggressive” Curve (Figure 11)	V1	$Q_1/K_{VARmin} + V_2$	Q1	$0.25*Q_{max,cap}$[40]
		V2	$V_{nom} - Deadband_{max}/2$	Q2	0
		V3	$V_{nom} + Deadband_{max}/2$	Q3	0
		V4	$Q_4/K_{VARmin} + V_3$	Q4	$0.25*Q_{max,ind}$
4	Test for Capacitive Offset on Deadband Points 2 and 3[41]	V1	$Q_1 /K_{VARavg} + V_2$	Q1	$0.50*Q_{max,cap}$
		V2	$V_{nom} - Deadband_{avg}/2$	Q2	$0.05*Q_{max,cap}$
		V3	$V_{nom} + Deadband_{avg}/2$	Q3	$0.05*Q_{max,cap}$
		V4	$Q_4 /K_{VARavg} + V_3$	Q4	$0.50*Q_{max,ind}$
5	Test for Inductive Offset on Deadband Points 2 and 3	V1	$Q_1/K_{VARmin} + V_2$	Q1	$0.25*Q_{max,cap}$
		V2	$V_{nom} - Deadband_{max}/2$	Q2	$0.05*Q_{max,ind}$
		V3	$V_{nom} + Deadband_{max}/2$	Q3	$0.05*Q_{max,ind}$
		V4	$Q_4/K_{VARmin} + V_3$	Q4	$0.25*Q_{max,ind}$

systems for power utility automation–Part 90-7: Object models for power converters in distributed energy resources (DER) systems,” Edition 1.0, Feb 2013.

[39] Requirements based on the jurisdiction, e.g., Electric Rule 21 for interconnection to California IOU electricity grids.

[40] Or as required by the Source Requirements Document.

[41] Tests 4-5 are performed at the request of the NRTL.

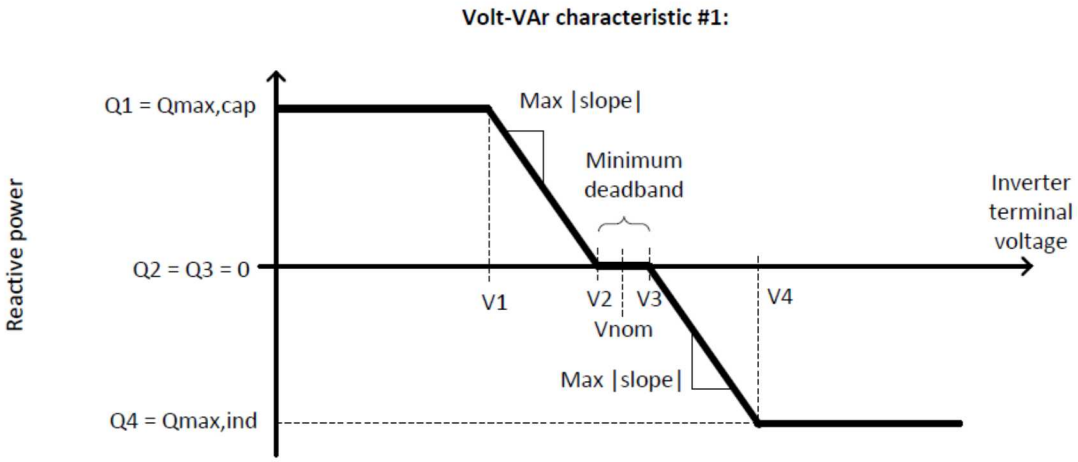

Figure 9: "Most Aggressive" Volt-VAr curve for R21-1-VV11, Test 1.

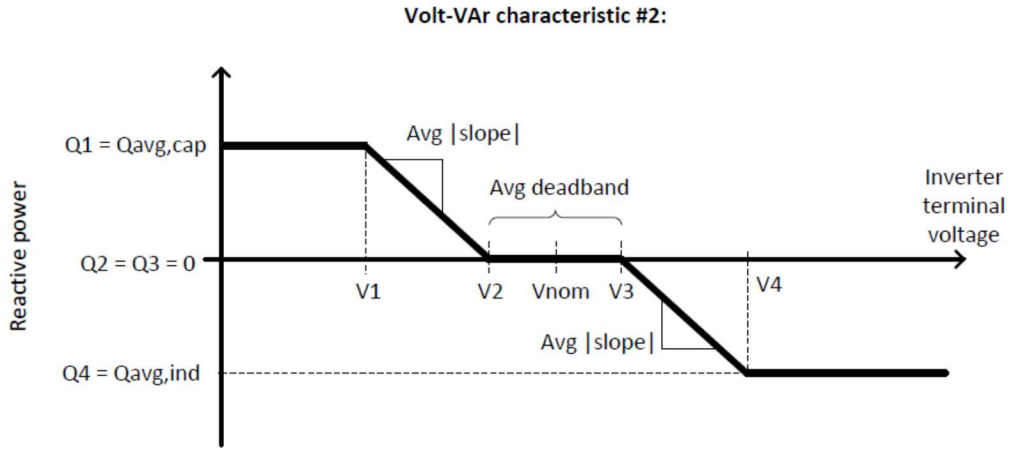

Figure 10: "Average" Volt-VAr curve for R21-1-VV11, Test 2.

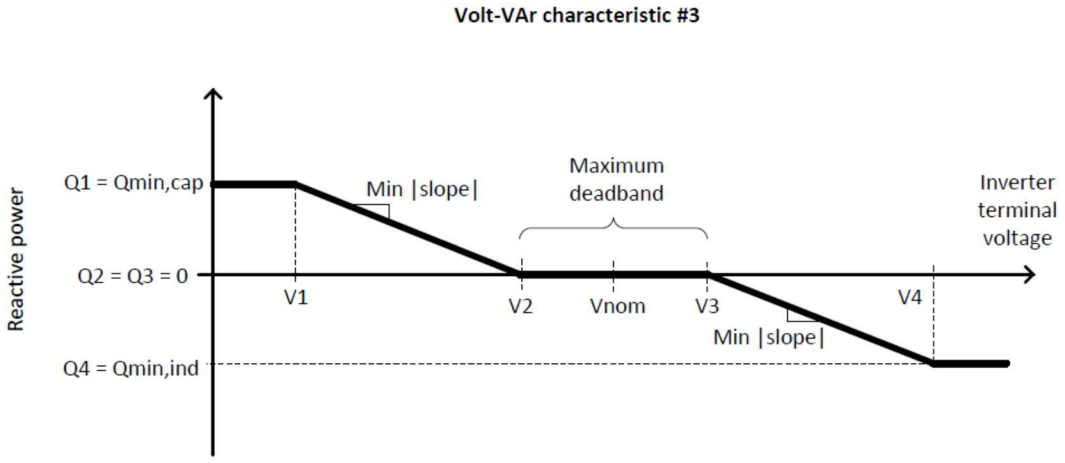

Figure 11: "Least Aggressive" Volt-VAr curve for R21-1-VV11, Test 3.

The Volt-VAr test shall be carried out as follows:

1. Connect the EUT according to the Requirements in Sec. 4.3.1 and specifications provided by the manufacturer.

2. Set all AC source parameters to the nominal operating conditions for the EUT. Frequency is set at nominal and held at nominal throughout this test. Set the input power to the value to P_{rated}.

3. Turn on the EUT. Set all R21-1-L/HVRT parameters to the widest range of adjustability possible with the R21-1-VV11 enabled.[42]

4. If the EUT has the ability to set 'Real Power Priority' or 'Reactive Power Priority', select 'Reactive Power Priority'.

5. Set the EUT to provide reactive power according to the Q(V) characteristic defined in Test 1 in Table 10.

6. Begin recording the time domain response of the EUT AC voltage and current, and DC voltage and current. Step down the AC voltage until at least three points[43] are recorded in each line segment of the characteristic curve or the EUT trips from the LVRT must trip requirements. Continue recording the time domain response for at least twice the settling time after each voltage step.

7. Repeat Step 6, raising the AC voltage until at least three points[44] are recorded in each line segment of the characteristic curve or the EUT trips from HVRT must trip requirements.

8. Repeat steps 6 – 7 four more times, for a total of five sweeps of the Q(V) curve.

9. Repeat test steps 5 - 8 at power levels 20% and 60% of P_{rated} by reducing the DC voltage of the Input Source.

10. Repeat steps 6 – 9 for the remaining tests in Table 10.[45]

4.3.1 Requirements

The inverter shall be connected into a test circuit similar to that shown in Figure 8. Measurements shall be performed at the terminals of the EUT. Time domain current and voltages shall be sampled at rate above 10000 samples/sec.

The simulated area EPS shall meet the requirements of clause 4.6.1 of IEEE Std 1547.1. The measurement system shall meet the requirements of clause 4.6.2 of IEEE Std 1547.1.

For three phase inverter test, the simulated EPS voltage in these tests is balanced meaning each phase has the same magnitude and phases are separated by 120 degrees. For single-phase tests the voltage under consideration is the RMS voltage at the inverter terminals.

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[42] The EUT's range of disconnect settings may depend on which function(s) are enabled.
[43] A minimum of three AC voltage settings will be used, but the NRTL and the manufacturer may agree on additional test points. The voltage between points should be large enough to resolve the VAr accuracy of the EUT for the function.
[44] A minimum of three AC voltage settings will be used, but the NRTL and the manufacturer may agree on additional test points. The voltage between points should be large enough to resolve the VAr accuracy of the EUT for the function.
[45] In the case of EUT without adjustable (V, Q) points, the manufacturer and NRTL may eliminate this step.

4.3.2 Criteria

For each voltage step, the EUT reactive power measurement should remain within the manufacturers stated accuracy of the Q(V) value except when the voltage is changing. The EUT shall obtain the Q(V) characteristic within its stated accuracy within the stated settling time.

Appendix 5 – R21-2-CI
Communications Interface

Version 1.0 31 May 2014 – Original Version
Version 2.0 8 Dec 2014 – Sandia Update

Draft UL Test Procedure for Inverter Communications Interfaces

5.1 Purpose

The communication interface is essential for the communications between the utility or third party and the EUT. The EUT must have a compliant communications interface in order for seamless DER interoperability.

5.2 Procedure for Communications Interface Evaluation

Verify the EUT is capable of including and/or adding the following communications media interfaces modules by installing and communicating using one of the following:

Must complete the SunSpec conformance procedure. Run the SunSpec procedure to perform read/write operations on the Modbus registers.

Plant-side of the gateway

- CEA-2045 with Modbus RTU pass-through
- Modbus RTU
- Modbus TCP

Network-side of the gateway

- Public Internet
- Utility private wide area network (WAN)
- Cellphone GPRS
- AMI Network
- Radio-based Network

Each of communications media shall be verified using the DS93 test protocol.

5.3 Requirements

Automated verification of the communications media must demonstrate compatibility.

5.4 Criteria

The NRTL interfacing device(s) must recognize the EUT communications interface.

Appendix 6 – R21-2-DATA
Data Model

Version 1.0 31 May 2014 – Original Version
Version 2.0 8 Dec 2014 – Sandia Update

Draft UL Test Procedure for Inverter Data Models

6.1 Purpose

This test verifies the EUT is capable of operating with the IEC 61850-90-7 data model.

5.2 Procedure for Communications Interface Evaluation

Verify the EUT is capable of operating with the IEC 61850-90-7 data model with the SunSpec Test tool.

6.3 Requirements

The certification tool must be connected through the communications interface and access the EUT data models.

6.4 Criteria

The NRTL interfacing device(s) must recognize the EUT data model.

Appendix 7 – R21-3-A
Monitor Alarms

Version 1.0 31 May 2014 – Original Version
Version 2.0 8 Dec 2014 – SNL Edit

Recommended UL Test Procedure for Monitoring Alarms

7.1 Purpose

Alarm event logs are maintained by the inverter-based DER systems to record key time-stamped events. The R21-3-A function reads the alarm event log to enable different users of the DER to retrieve event logs with relevant information for their purposes. Table 11 lists some of the alarm types, although specific alarms will depend on EUT manufacturer specifications and the Source Requirements Document, e.g., CA Electric Rule 21.

Table 11: R21-2-A Alarm Events.[46]

Domain	Part or Alarm	Attribute	Description
Communication	Messaging	Message Failed	Response – alarm invalid message. Value field contains type of error
	Network Interface	Comm. Failed	Alarm communications error. Value field contains type of error
PV System	Inverter GFPD[47]	Ground Fault Trip	Ground fault detected.
	Inverter AFCI[48]	Arc-Fault Trip	Arc-fault detected.
	Inverter DC Disconnect	Open	No DC power available to EUT.
	Manual Shutdown of Inverter	Activated	EUT shutdown locally.
	Inverter Cabinet Open	Open	EUT equipment being serviced.
	DC Over Voltage	High PV system Voltage	Too much DC voltage connected to EUT, e.g., from improper installation.
	Temperature	Limit Exceeded	Temperature limit exceeded.
Grid Power	No Grid Detected	No ECP Voltage	Inadequate grid voltage.
	AC Disconnect	Open	Inadequate grid voltage due to an open AC contactor.
	AC Over Voltage	Limit exceeded	High voltage limit (HVRT) exceeded.
	AC Under Voltage	Limit exceeded	Low voltage limit (LVRT) exceeded.
	Over Frequency	Limit exceeded	Voltage limit exceeded.
	Under Frequency	Limit exceeded	Voltage distortion limit exceeded.
	AC Current	Limit exceeded	Current limit exceeded.
	Power Quality	Limit exceeded	Harmonic limit exceeded.
Device Asset	Logs	Full	Inadequate system memory.
	Time	Clock Failed	Clock failure.
	Time	Synch Failed	Synchronization failed.
	Firmware	Data Error	Data error detected in firmware.

7.2 Procedure

The R21-3-A test shall be carried out as follows:

1. Connect the EUT according to the Requirements in Section 7.2 and specifications provided by the manufacturer.

2. Set all AC and DC source parameters to the nominal operating conditions for the EUT.

3. Turn on the EUT.

4. Record the time and artificially create an alarm.

[46] Alarms based on discussions during the SIWG call on 2 Oct, 2014.
[47] Ground fault protection device.
[48] Arc-fault circuit interrupter.

5. Read the alarm and the alarm timestamp.

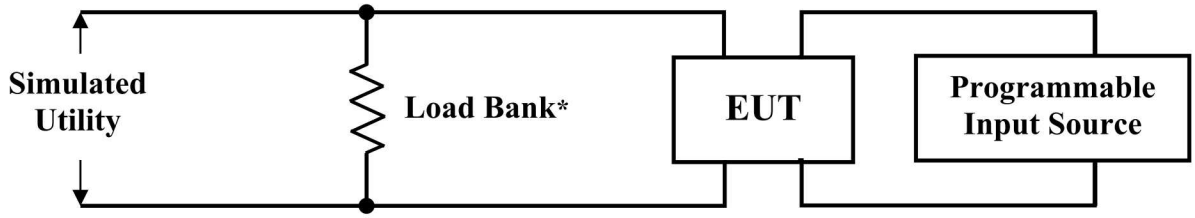
6. Repeat Steps 4 and 5 four additional times for a total of 5 events.

7. Repeat Steps 4-6 for additional alarms.[49]

7.3 Requirements

The manufacturer shall provide the accuracy of their timestamp in seconds.

Inverter shall be connected into a test circuit similar to that shown in Figure 12.



* Note: Load bank required only for non-regenerative simulated utility sources. Some simulated utility sources are unidirectional sources and therefore require a load bank to absorb the real and reactive power produced by the EUT during testing.

Figure 12: R21-3-A test circuit.

7.4 Criteria

The EUT shall report the correct alarm and alarm timestamp within the manufacturers stated accuracy.

[49] The number of total alarms will be determined by the manufacturer and NRTL based on the Source Requirements Document.

Appendix 8 – R21-3-DS93
Monitor DER Status and Output

Version 1.0 31 May 2014 – Original Version
Version 2.0 8 Dec 2014 – Sandia Revision

Draft UL Test Procedure for DER Status and Output Monitoring

8.1 Purpose

The DER provides current status, power system measurements, and other real-time data to the utility in order to support real-time and short-term analysis applications. The R21-3-DS93 function requests the current operational state of the PV/storage system in response to a command from the utility controller. Manufacturers are required to provide reporting status of one or more data elements on receiving a request. The manufacturer may also provide for status updates periodically or upon significant status change. The details of implementing the status reporting are left up to the manufacturers. Status value or data sets are left up to the manufacturer but it is recommended that they contain parameters shown in Table 12.

Table 12: Possible R21-2-DS93 Status and Output Data.[50]

Status Point	Description[51]
Header information for all messages.	
Unique DER System ID	Used to identify source or destination of information
Meter ID, Service Point ID, or other ECP ID	Used to identify source or destination of information
Utility ID	Used to identify source or destination of information
Timestamp of message and other header information	Dependent on protocol as well
Nameplate and/or "as installed" base information of DER System.	
DER system manufacturer	Mn, Manufacturer
DER system model	Md, Model
DER system version	V, Version
DER system serial number	SN, Serial Number
DER system type	DERTyp
Location (optional)	Longitude, latitude, street address
Basic information - May change due to upgrades, aging, reconfigurations, or customer decisions, etc.	
Operational authority	Role, name, and rights (used to authorize any actions)
Watt rating	WRtg
VA rating	VARtg
Var rating	VArRtg
Current rating	ARtg
PF rating	PFRtg
Monitored DER system analog measurements – may be instantaneous, average over period, max, min, first, last	
Watts	W, Real Power
VArs	VAr, Reactive Power
Power Factor	PF, Power Factor
Hz, Frequency	Hz, Frequency
VA, Apparent Power	VA, Apparent Power
A, Phase Currents	A, Phase Currents
PPV, Phase Voltages	PPV, Phase Voltages
TmpCab, Temperature (optional)	TmpCab, Temperature
Monitored DER system status	
DER Connection Status	PVConn, PV connection status

[50] Values taken from the SIWG discussion on 9 Oct, 2014.
[51] Often the description is the SunSpec Alliance Data Model Specification for the parameter.

Status Point	Description[51]
PCC or ECP Connection Status	ECPConn, inverter connection status
Inverter status	St, inverter status
Available watts	WAval, available watts
Available vars	VArAval, available vars
Status of limits	StSetLimMsk, Status of set limits reached
Active modes	StActCtl, status of active controls
Ride-through status	RtSt, active ride-through status
Metered DER system values	
DER Connection Status	PVConn, PV connection status
PCC or ECP Connection Status	ECPConn, inverter connection status
Inverter status	St, inverter status
Available watts	WAval, available watts
Available vars	VArAval, available vars
Status of limits	StSetLimMsk, Status of set limits reached
Active modes	StActCtl, status of active controls
Ride-through status	RtSt, active ride-through status
Metered DER system values	
Wh, Watt-hours, lifetime accumulated AC	Wh, Watt-hours, lifetime accumulated AC
VAh, VA-hours, lifetime accumulated	VAh, VA-hours, lifetime accumulated
VArh, VArh, lifetime accumulated	VArh, VArh, lifetime accumulated
Additional Advanced Inverter parameters for each of the available DER functions.[52]	

8.2 Procedure

The R21-3-DS93 test shall be carried out as follows:

1. Turn on the EUT according to the specifications provided by the manufacturer.
2. Record the time and measure the status using an appropriate data acquisition system. Request a data value with read permissions.
3. Record the EUT response.
4. Repeat Steps 2-3 four additional times for the data value, for a total of 5 status measurements.
5. Repeat Steps 2-4 for additional statuses.[53]

8.3 Requirements

The manufacturer will provide the maximum response time for the status reporting function, R21-3-DS93 and the accuracy of each of the status measurements.

8.4 Criteria

[52] Defined in the SunSpec Alliance Data Models located at sunspec.org.
[53] The number of total status measurements will be determined by the manufacturer and NRTL based on the Source Requirements Document.

The EUT shall report the status within manufacturers stated accuracy within the required response time as defined by the Source Requirements Document.

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