Analysis of a GaN-Based CRM Totem-Pole PFC Converter Considering Current Sensing Delay

Jingjing Sun
Min H. Kao EECS
The University of Tennessee
Knoxville, TN USA
jsun30@vols.utk.edu

Nathan N. Strain
Min H. Kao EECS
The University of Tennessee
Knoxville, TN USA
nstrain@vols.utk.edu

Daniel J. Costinett
Min H. Kao EECS
The University of Tennessee
Knoxville, TN USA
daniel.costinett@utk.edu

Leon M. Tolbert
Min H. Kao EECS
The University of Tennessee
Knoxville, TN USA
tolbert@utk.edu

***Abstract*—High-frequency soft-switched gallium-nitride (GaN) based critical conduction mode (CRM) totem-pole power factor correction (PFC) converter is one of the most potential candidates in data center power supplies. However, the high-speed cycle-by-cycle zero current detection (ZCD) brings challenges to zero-voltage-switching (ZVS) control. Current sensing delay (CSD) exists, and the ZCD circuit is sensitive to high di/dt switching noise. In this paper, mechanisms of the ZCD time error are elaborated, and impacts of the current sensing delay on converter switching frequency, inductor current, input current third harmonic distortion (THD), and power loss are analyzed. Qualification time is added within the controller for immunity to the swiching noise, and a CSD embedded converter model is proposed to compensate the ZCD time delay. Also, loss modeling of the CRM totem-pole PFC is conducted to aid in analysis of the proposed theory. A 1.5 kW single-phase CRM totem-pole PFC prototype is tested. Experimental results validiate the analysis, modeling, and the proposed compensation method for current sensing delay.**

Keywords— GaN, CRM, totem-pole PFC, soft switching, zero current detection (ZCD), current sensing delay

I. INTRODUCTION

To accommodate the fast growing data center market, high-efficiency and high-density AC-DC power supplies are required [1] [2]. Recently, the gallium-nitride (GaN) based totem-pole power factor correction (PFC) converter has become popular since it eliminates the conduction loss of the diode rectifier and the reverse recovery loss of the body diode [3] [4]. Although the hard-switched GaN-based totem-pole PFC has been demonstrated with high efficiency [5], switching frequency is usually limited below 120 kHz due to the switching loss, and power density is impacted. For GaN devices, the turn-off loss is much less than the turn-on loss [6]. Thus, minimizing the turn-on loss through zero voltage switching (ZVS) significantly decreases the switching loss, allowing higher switching frequency and power density of the converter. To realize soft switching, techniques such as critical conduction mode (CRM) control have been widely used [7] [8]. MHz GaN-based CRM totem-pole PFC converters have been demonstrated with very high efficiency and high power density [9] - [11].

For the CRM totem-pole PFC converter, ZVS is inherent only when $V_{in} \le 0.5V_o$. When $V_{in} > 0.5V_o$, ZVS cannot be passively achieved, resulting in partial hard switching loss. To achieve the full-line-cycle ZVS, conduction time of the synchronous rectifier (SR) switch is typically extended to obtain a negative current. One of the popular ZVS control methods is the model-based variable on-time control [12] [13]. Fig. 1 presents the control implementation based on a digital signal processor (DSP). The PI controller regulates the output voltage and generates the dominant on time (T_{on_c}) for the active switch. Meanwhile, based on the converter model and sensed signals (V_{in}, V_o), switching time intervals required for ZVS are calculated in real time.

In order to ensure ZVS in each switching cycle, a positive-to-negative zero current detection (ZCD) signal is used to synchronize the timer and limit the minimum current stress. As shown in Fig. 2, the time-based counter in the PWM module is reset every time the ZCD signal occurs. Based on the time reference, the SR switch is turned off after the extended conduction time for ZVS achievement at T_{sr_off}, then the active switch is turned on after the resonant time at T_{ac_on} and turned off after the on time at T_{ac_off}, and the SR switch is turned on after a short dead time at T_{sr_on}. In this way, the peak inductor current is controlled by the PI controller, and the valley inductor current is limited by the ZCD signal and the extended conduction time t_{sr_ex}. Also, synchronization between the inductor current and switching signals is maintained [13].

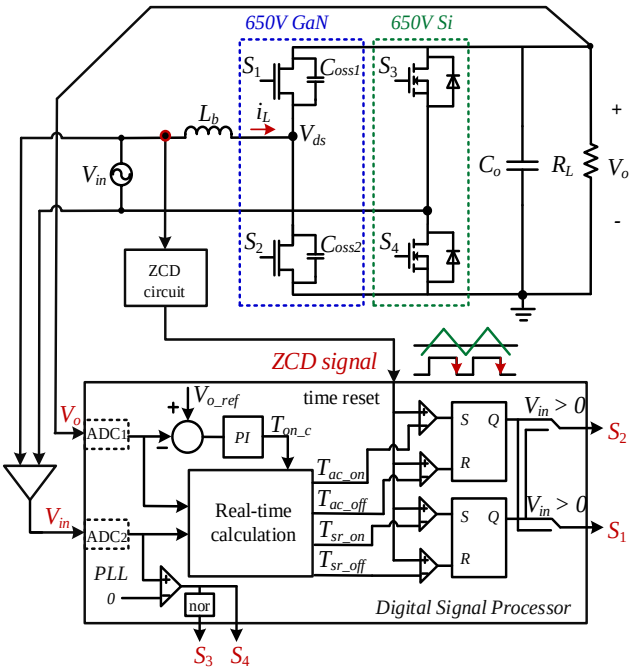


Fig. 1. GaN-based soft-switched CRM totem-pole PFC converter with digital-based variable on-time control.

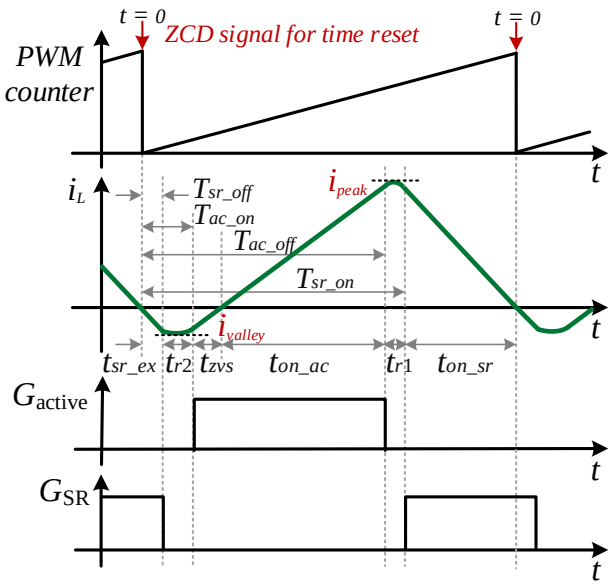


Fig. 2. Operation principle of the GaN-based CRM totem-pole PFC converter (t_{on_ac} - conduction time of active switch, t_{on_sr} - conduction time of SR switch, t_{sr_ex} – extended conduction time of SR switch, t_{r1}, t_{r2} - resonant time intervals, t_{zvs} - ZVS margin period).

As can be seen, the variable frequency CRM operation and cycle-by-cycle ZVS realization relies on the accurate detection of the zero current crossing via proper analog circuits. The most popular and conventional zero current detection (ZCD) circuit includes a current sensing resistor, high-speed amplifier, comparator, and isolator. However, the ZCD circuit is sensitive to high frequency di/dt or dv/dt noise, and the control network is prone to anomalous switching actions when an erroneous ZCD signal is generated due to a disturbance from the switching noise. To mitigate the noise issue, significant engineering efforts are often required on the PCB layout and other implementations. Ref. [14] has proposed several control techniques, but they are complicated for a practical implementation. In [15], a controllable blanking time is created by internal logic circuits in a FPGA after each switching action. This method can effectively reject the switching noise but is hard to implement with a DSP unless additional logic circuits are added externally. In addition, nonlinear ZCD time delay exists due to nonideal passive components and the signal propagation via active chips. Such time error is more influential in high-frequency applications, and deviates the converter switching frequency and inductor current from the normal operation, further impacting the current total harmonics distortion (THD) and power loss. To address the problem of ZCD time delay, a current compensation method by dynamically adjusting the comparator reference voltage is proposed in [15]. Though the approach is reasonable, it requires online/offline calculation of the dynamic reference voltage in the controller and a digital-to-analog converter (DAC) circuit to generate the adaptive reference voltage for the comparator.

To overcome both the issues of switching noise and current sensing delay in the GaN-based high-frequency CRM totem-pole PFC converter, a detailed analysis and no-cost approach (no additional hardware) is proposed in this paper. First, mechanisms of the ZCD time error and impacts on converter performance are analyzed in Section II. To avoid additional circuits, qualification time is added within the DSP to provide noise immunity when passing the ZCD signal. In order to reduce the influence of the ZCD time delay, a current sensing delay (CSD) embedded converter model is proposed in Section III. To help analyze the effect of the current sensing delay and verify the proposed method, loss modeling of the CRM totem-pole PFC converter is illustrated in Section IV. A 1.5 kW PFC prototype and experimental verification are presented in Section V, and Section VI states the conclusions.

II. Current Sensing Delay and Impacts

A. Zero Current Detection (ZCD) Circuit

Fig. 3 presents the designed ZCD circuit based on a current sensing resistor R_{shunt}. The current sensing resistor is connected in series with the input power line of the CRM totem-pole PFC converter. To minimize the additional conduction loss, a small sensing resistor (10 mΩ) is selected. A bias voltage is added on one side of the resistor so that the sensed signal is always positive. High-bandwidth amplifier is then required to enlarge the signal. The following circuit includes a high-speed comparator and digital isolator.

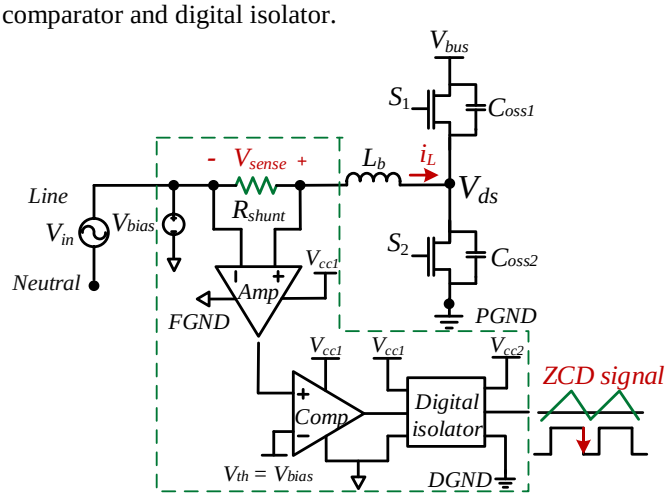


Fig. 3. ZCD circuit based on current sensing resistor.

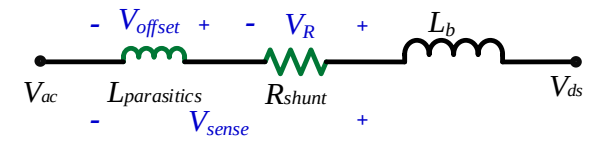
B. Mechanisms of the ZCD Signal Time Error

In practice, ZCD signal time error introduced by signal propagation and noise immunity challenges the ZVS control of the CRM PFC. The controller either acting earlier or later than the real zero current crossing moment causes current distortion and further impacts the converter loss. Mechanisms of the ZCD time error can be divided into four different types:

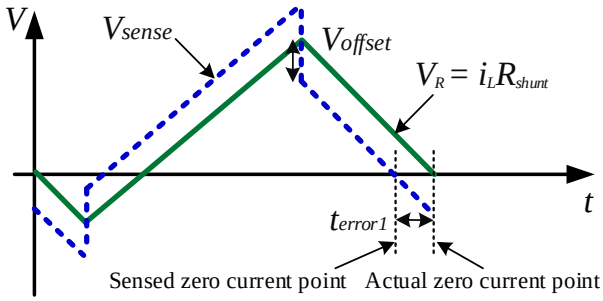
t_{error1} - Leading time error arises from the parasitics in the sensing resistor, as shown in Fig. 4. For the fast-switching CRM operation, minimal series inductance can induce significant offset in the sensed voltage, making the detected zero current point leading to the actual zero current point. And the offset voltage varies with the instantaneous current slope. In this case, $di/dt=(V_{in}-V_o)/L_b$.

$$V_{sense} = V_R + V_{offset} = i_L R_{shunt} + L_{parasitic}\frac{di}{dt} \quad (1)$$

t_{error2} - Propagation delay time error resulting from hardware components like amplifier, comparator, gate driver, RC filters, etc. This time delay can be small (10 ns - 20 ns) if high-bandwidth chips and R-C filter are employed.



(a) Current sensing resistor with the equivalent series inductance.



(b) Sensed voltage with nonlinear offset.

Fig. 4. Illustration of the leading time error due to the series inductance of the sensing resistor.

t_{error3} - Signal processing delay time error in the DSP. Based on the measurment, t_{error3} is around 90 ns - 100 ns, which is consistent with the result in [12].

t_{error4} - Qualification delay time error required for negating the switching noise in the DSP. For the fast-switching CRM PFC, the ZCD circuit is sensitive to high di/dt or dv/dt noise. As shown in Fig. 5, high di/dt noise occurs when the active switch is hard turned off at the peak inductor current. Without good isolation and PCB layout, the switching noise can be coupled into the ZCD circuit and erroenous ZCD signal is generated right after the turn-off transition. This erroenous ZCD signal resets the timer again, and forces the inductor current to keep increasing. Hence, overcurent happens and devices are damaged. To avoid the false switching action, instead of using an additional logic circuit to create blanking time, ZCD signal is qualified in the GPIO port when passed to the DSP. As a result, delay time error t_{error4} is generated.

Therefore, the overall ZCD time error is the sum of the four time errors. Only t_{error1} is the leading time error and the rest are delay time errors. Typically, t_{error3} and t_{error4} are much larger than t_{error1} and t_{error2} if the current sensing resistor with small series inductance is selected. So the final ZCD time error is prone to be delay time. Since the total ZCD time delay is nonlinear and highly depends on the specific circuit, it is hard to predict it accurately. Also, the ZCD signal used in the ZVS control is the positive-to-negative zero current point, which is followed by a very short deadtime. So simple compensation by modifying the time intervals is not feasible. Hence, compensating the current sensing delay becomes a challenge.

C. Impact of the Current Sensing Delay

The ZCD time delay affects the converter switching frequency, inductor current, input current THD, and power loss.

As shown in Fig. 6, the ZCD time delay results in a longer SR switch conduction time, and the inductor valley current is lower. Correspondingly, the PI controller will increase the conduction time T_{on_c} of the active switch to maintain the same output power. It is noted that, according to the model-based variable on-time control shown in [12] [13], the conduction

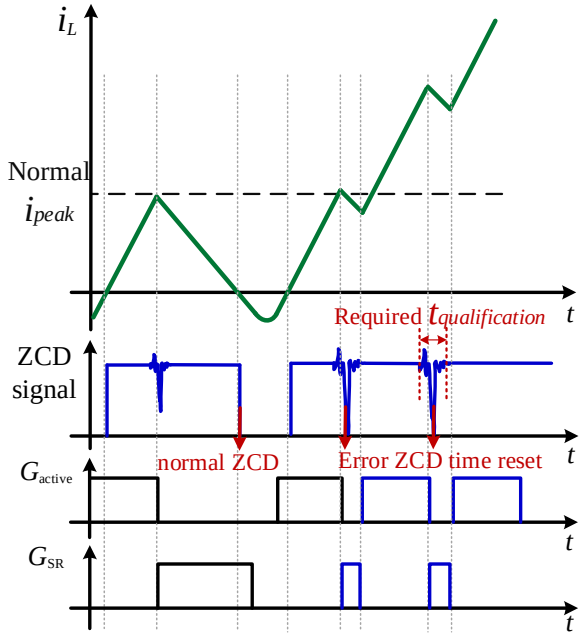


Fig. 5. Anomalous ZCD signal and switching actions due to a disturbance by high di/dt noise.

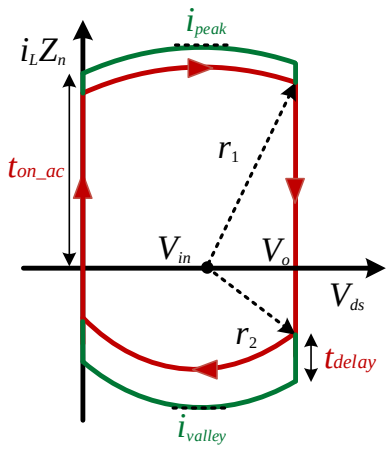
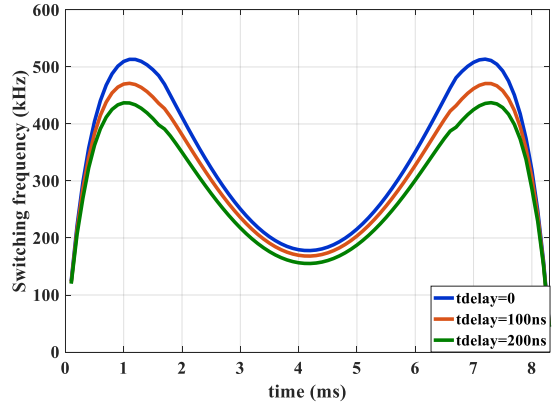


Fig. 6. State trajectory of the CRM PFC with the effect of current sensing delay ($Z_n = (L_b/(2C_{oss}))^{½}$ is the impedance of the resonant tank. Red line - ideal trajectory; green line - trajectory with t_{delay}).

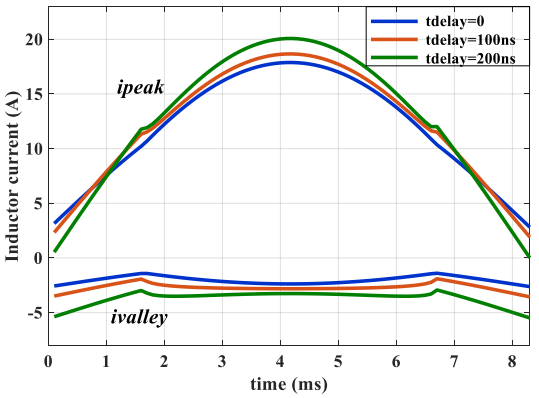
time of the active switch t_{on_ac} is composed of two parts, $t_{on\_ac} = T_{on\_c} + T_{on\_v}$, where T_{on_c} is the constant part generated from the low-bandwidth PI controller, and T_{on_v} is the variable part based on the real-time calculation. When $V_{in} > 0.5V_o$, the peak current will be higher with the increased T_{on_c} since $T_{on\_v} = 0$ and $t_{on\_ac} = T_{on\_c}$. However, when $V_{in} \leq 0.5V_o$, $T_{on\_v} \neq 0$ and $t_{on\_ac} = T_{on\_c} + T_{on\_v}$. Although T_{on_c} is increased, T_{on_v} is still calculated based on the ideal case, which is not enough to keep the same peak current. Meanwhile, due to the lower valley current, the required resonant time is smaller than the normal operation, further distorting the inductor current.

Fig. 7 shows the PFC switching frequency, inductor peak and valley currents, and the input current with various ZCD delay times under the positive half line cycle. Since the ZCD time delay disturbs the normal switching actions, switching speed becomes slower, and inductor current ripple is enlarged.

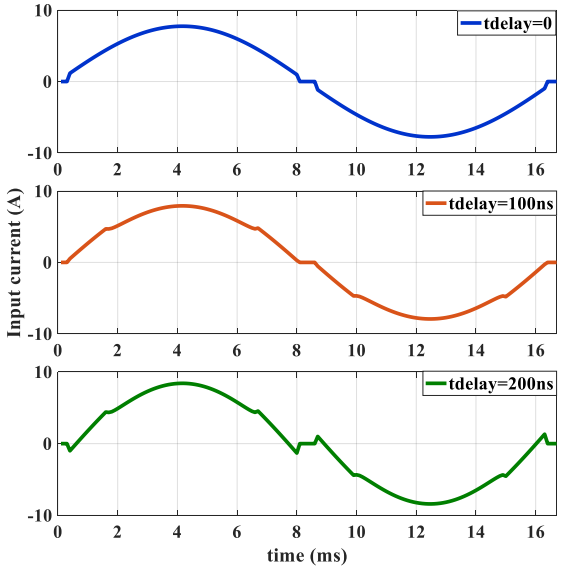
The valley current keeps decreasing with increased delay time, but the peak current only stays higher with ZCD delay time when $V_{in} > 0.5V_o$, and starts to drop when $V_{in} \leq 0.5V_o$. This results in distorted average current and worse current THD. Also, converter loss is influenced with the increased current ripple and switching period. Detailed discussion on the converter loss is given in Section IV.



(a) Switching frequency of the PFC with various ZCD delay times.



(b) Inductor currents of the PFC with various ZCD delay times.



(c) Input current of the PFC with various ZCD delay times.

Fig. 7. Switching frequency, inductor current, and input current of the totem-pole CRM PFC with different ZCD delay times when V_{in} = 277 V_{ac}, V_o = 480 V_{dc}, P_o = 1.5 kW, k_{min} = 1.1, L_b = 20 µH.

III. PFC Model with Current Sensing Delay and Compensation

To reduce the impact of the current sensing delay, two methods are adopted in the control implementation.

A. Partial Delay Cancellation

Noticing that t_{error1} is leading time error and contradictory to other time errors, it can be purposely enlarged to cancel out partial delay time. So instead of using one 10 mΩ sensing resistor, two 5 mΩ sensing resistors are connected in series to enlarge the parasitic inductance. As shown in Fig. 8, the ZCD signal time error from the hardware circuit to the DSP (t_{error1} + t_{error2}) is monitored within the whole line cycle, and the total ZCD time error is obtained by adding the constant time delay within the DSP (t_{error3} + t_{error4}). Based on the PFC prototype, at full load, the hardware time error (t_{error1} + t_{error2}) is nonlinear leading time, and the software time error (t_{error3} + t_{error4}) is constant 140 ns. Hence, the overall time delay is nonlinear over the line cycle, decreasing from 125 ns at low input voltage level to 55 ns at high input voltage level. The final time delay is curve fitted as shown in the dashed red line.

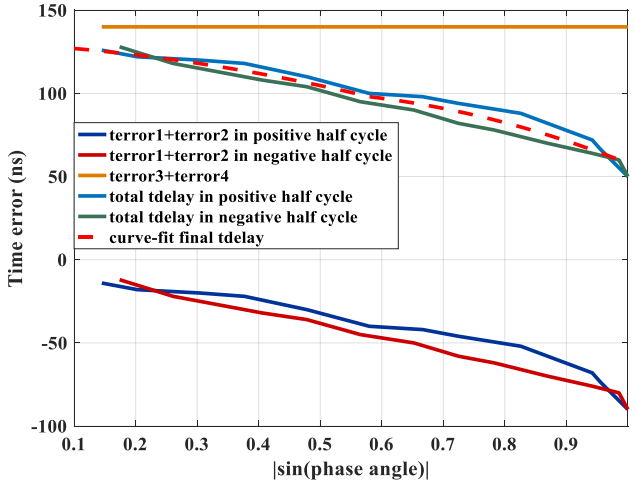


Fig. 8. Monitored and curve-fit total ZCD time error vs. |sinθ| at full load.

B. Current Sensing Delay (CSD) Embeded Converter Model

To further compensate the ZCD time delay, the analytical converter model shown in [13] of the CRM PFC is modified by considering the curve - fit ZCD time delay. Since the time delay enlarges the required conduction time of the SR switch for ZVS achievement, the original SR extended conduction time is reduced by the delay time so that the overall SR conduction time is maintained the same. As shown in (2), k is the ZVS margin constraint, C_{oss} is the equivalent output capacitance of GaN device [13].

$$t_{sr\_ex} = t_{sr\_ex\_original} - t_{delay} = \frac{\sqrt{(k^2-1)V_{in}^2 - V_o^2 + 2V_oV_{in}} \times \sqrt{2L_bC_{oss}}}{(V_o - V_{in})} - t_{delay} \quad (2)$$

Such compensation can only be achieved when $t_{sr\_ex\_orignal} \geq t_{delay}$. When $t_{sr\_ex\_orignal} < t_{delay}$, the extended SR conduction time is zero or not enough to encompass the delay time, and the compensation cannot be fully implemented. Based on the same principle of the model derivation in [13], the ZVS margin constraint is therefore modified to

$$k = \begin{cases} \frac{V_o - V_{in}}{V_{in}} \sqrt{\omega_r^2 t_{delay}^2 + 1}\,, & \text{when } V_{in} < \frac{\sqrt{\omega_r^2 t_{delay}^2 + 1}}{k_{min} + \sqrt{\omega_r^2 t_{delay}^2 + 1}} V_o \\ k_{min} \geq 1 \qquad\qquad , & \text{when } V_{in} \geq \frac{\sqrt{\omega_r^2 t_{delay}^2 + 1}}{k_{min} + \sqrt{\omega_r^2 t_{delay}^2 + 1}} V_o \end{cases} \quad (3)$$

Expressions for i_{peak}, i_{valley}, t_{on_ac}, t_{r1}, t_{on_sr}, t_{r2}, and t_{zvs} do not change. In this way, the desired average input current is maintained, avoiding input current distortion.

Fig. 9 shows the full-load inductor currents (i_{peak}, i_{avg}, i_{valley}) of the CRM PFC within the positive half line cycle with and without the delay compensation. The ZCD time delay at both cases are the same as the one shown in Fig. 8. The dashed red lines represent the ideal currents without any ZCD time delay. For the case (Fig. 9 (a)) with ZCD time delay and no compensation, inductor currents are distorted with larger current ripple, resulting in more conduction loss. If the modified converter model is employed to compensate the current sensing delay, as shown in Fig. 9 (b), the average inductor current is kept the same as the ideal case and inductor current ripple is not enlarged. The only discrepancy is the slightly increased peak and valley current during the natural - ZVS region, where the ZCD signal time delay cannot be fully compensated since there is insufficient extended conduction time and the SR switch only turns off when ZCD signal occurs. However, the impact of such discrepancy is not severe since both the voltage and current at this region are low.

IV. Loss Modeling

The dominant loss mechanisms of the CRM totem-pole PFC converter include the device conduction loss, turn-off switching loss, inductor core loss, and winding loss.

A. Device Conduction Loss

As shown in Fig. 2, if approximating the inductor current as a triangular waveform with the maximum value at i_{peak} and the minimum value at i_{valley}, the inductor RMS current is

$$i_{Lrms} \approx \sqrt{\frac{1}{3}\left({i_{peak}}^2 + {i_{valley}}^2 + i_{peak} i_{valley}\right)} \quad (4)$$

Since the two devices in one phase leg conduct in turns, the total conduction loss in one phase leg is equivalent to one switch conducting all the time if neglecting the small deadtimes. Hence, the equivalent RMS currents of the GaN device and the Si device are $i_{rms\_GaN} \approx i_{rms\_Si} \approx i_{Lrms}$. Then the total GaN device conduction loss over the AC line cycle is

$$P_{cond\_GaN} = f_{line} \int_0^{T_{line}} i_{rms\_GaN}^2 R_{on\_GaN} dt \quad (5)$$

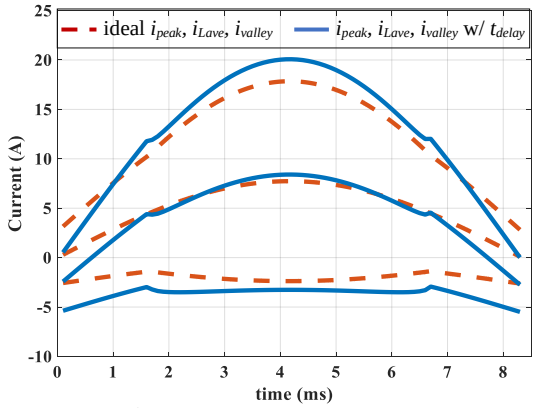
And the Si device conduction loss over the AC line cycle is

$$P_{cond\_Si} = f_{line} \int_0^{T_{line}} i_{rms\_Si}^2 R_{on\_Si} dt \quad (6)$$

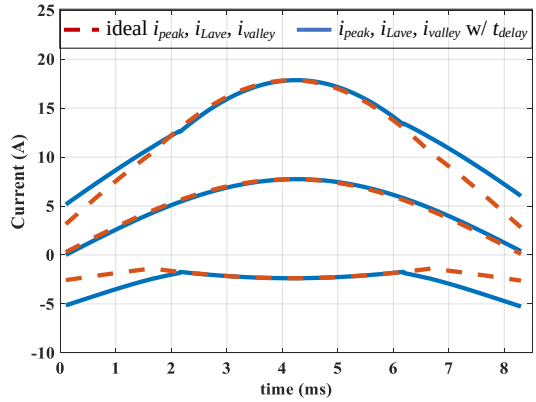
where R_{on_GaN} and R_{on_Si} are the on resistances of the GaN device and Si MOSFET respectively.

B. Device Turn-Off Loss

Since soft-switching turn on of the GaN devices is ensured, the dominant switching loss is the GaN device turn-off loss. Switching loss of Si MOSFETs is very small and neglected



(a) Comparison of inductor currents between ideal case and the case with current sensing delay and no compensation.



(b) Comparison of inductor currents between ideal case and the case with delay compensation by adopting the modified converter model.

Fig. 9. Inductor currents (i_{peak}, i_{avg}, i_{valley}) of the CRM PFC at full load within the positive half line cycle when V_{in} = 277 V_{ac}, V_o = 480 V_{dc}, P_o = 1.5 kW, k_{min} = 1.1, L_b = 20 µH.

because they switch at line frequency. The GaN device turn-off energy is measured by double pulse test (DPT) with soft turn-on switching at different conducting currents. Thus, the total GaN device turn-off loss over the AC line cycle is

$$P_{off\_GaN} = f_{line} \int_0^{T_{line}} f_{sw}(E_{off\_ac} + E_{off\_sr}) dt \quad (7)$$

where $E_{off\_ac} = E_{off}(|i_{peak}|)$ and $E_{off\_sr} = E_{off}(|i_{sr\_off}|)$ are measured turn-off energies for active and SR switches respectively.

C. Inductor Core Loss

Traditional Steinmetz Equation (SE) is not accurate for core loss calculation of the CRM PFC with large current ripple. Instead, Generalized Steinmetz Equation (GSE), proposed in [16], is adopted to estimate the core loss. The core loss density in each switching cycle is

$$p_v = f_{sw} \int_0^{t_{sw}} k_1 \left|\frac{dB}{dt}\right|^{\alpha} |B|^{\beta-\alpha} dt \quad (8)$$

And the total core loss over the AC line cycle is

$$P_{core} = V_{core} \cdot f_{line} \int_0^{T_{line}} p_v dt \quad (9)$$

where B is the instantaneous flux density derived by inductor current, V_{core} is the core volume, α, β, k are Steinmetz coefficients of the specific core material, and $k_1 = k/((2\pi)^{\alpha-1} \int_0^{2\pi} |cos\theta|^{\alpha} |sin\theta|^{\beta-\alpha} d\theta)$, θ = 0~2π.

D. Inductor Winding Loss

The winding loss includes the low-frequency DC copper loss and the high-frequency eddy current related losses. The DC winding loss is calculated based on the copper resistance.

$$P_{winding\_dc} = f_{line} \int_0^{T_{line}} i_{Lrms}^2 R_{winding\_dc} dt \qquad (10)$$

For the high-frequency CRM PFC, litz wire is typically used to reduce the eddy current related loss. However, the commercial finite element analysis (FEA) tools cannot be used directly to simulate the AC winding loss due to the large number of the litz wire strands. Instead, the square-field-derivative (SFD) method combining the FEA simulation and analytical calculation is adopted [17]. The AC winding loss over the line cycle is

$$P_{winding\_ac} = f_{line} \int_0^{T_{line}} p_{winding\_ac} dt$$
$$= f_{line} \int_0^{T_{line}} [f_{sw} \int_0^{t_{sw}} \gamma \langle B_b{}^2 \rangle \left(\frac{di_L}{dt}\right)^2 dt \,] dt \qquad (11)$$

where B_b is the normalized flux with unit current obtained from the static field; γ is determined by parameters of the specific litz wire, $\gamma = k\pi l_t N n d_c^4/(64\rho_c)$ [17].

Other losses including the capacitor loss and conduction losses on the sensing resistor and PCB traces are also calculated in the loss model.

Based on the loss model, loss breakdown of a 1.5 kW CRM PFC at full load is estimated considering different cases, as shown in Fig. 10. In the ideal case without ZCD time delay, the PFC power loss at full load is 15.4 W. With the ZCD time delay presented in Fig. 8, all types of losses increase, and the full-load power loss is 18.5 W. By adopting the proposed compensation approach, the full-load power loss is reduced to 16.2 W, which is only 0.8 W higher than the ideal case. Therefore, the proposed CSD embedded converter model can effectively reduce the extra converter loss induced by the current sensing delay.

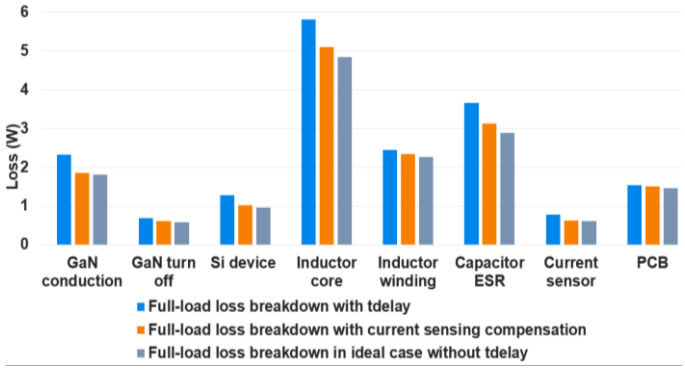


Fig. 10. Loss breakdown of the CRM totem-pole PFC based on the loss model when V_{in} = 277 V_{ac}, V_o = 480 V_{dc}, P_o = 1.5 kW, k_{min} = 1.1, L_b = 20 µH.

V. Experimental Verification

To verify the analysis and proposed method, a 1.5 kW single-phase GaN-based CRM totem-pole PFC prototype is built and tested, as shown in Fig. 11. 650 V GaN device GS66508T and Si MOSFETs IPW65R019C7 are used in the prototype. The boost inductor is designed at 20 µH, implemented with powder toroidal core Mix-2 T106 and 350/42 litz wire. The specified voltage rating is V_{in} = 277 Vac at 60 Hz and V_o = 480 Vdc. ZVS margin k_{min} = 1.1 is adopted.

Fig. 12 presents the experimental results at full load of the 1.5 kW single-phase GaN-based CRM PFC prototype. The ZCD time delay is shown in Fig. 8, and the proposed compensation method is employed to reduce its impact. ZVS is achieved within the whole line cycle, and both input current and output voltage are well regulated. The tested full-load PFC efficiency is 98.9%, and the input power factor is above 0.99.

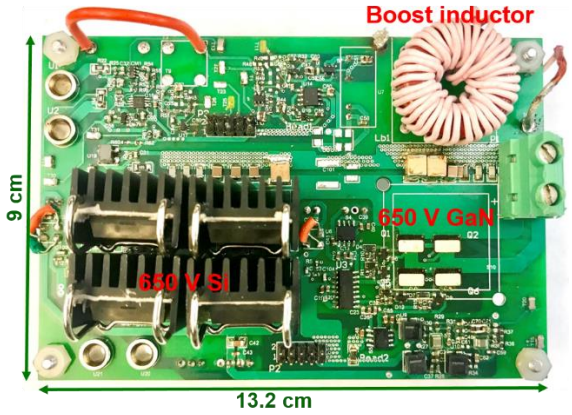
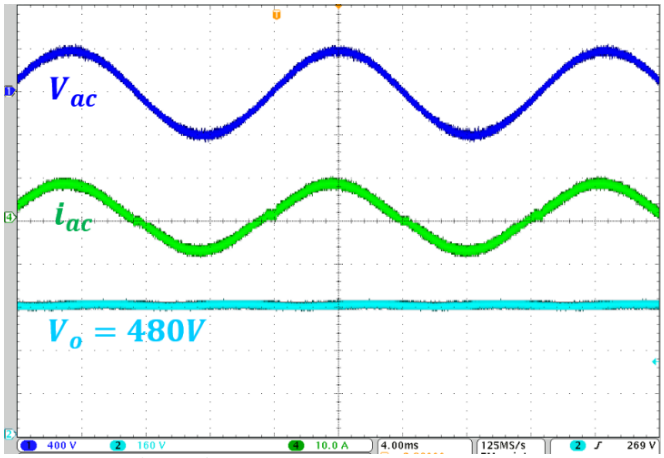
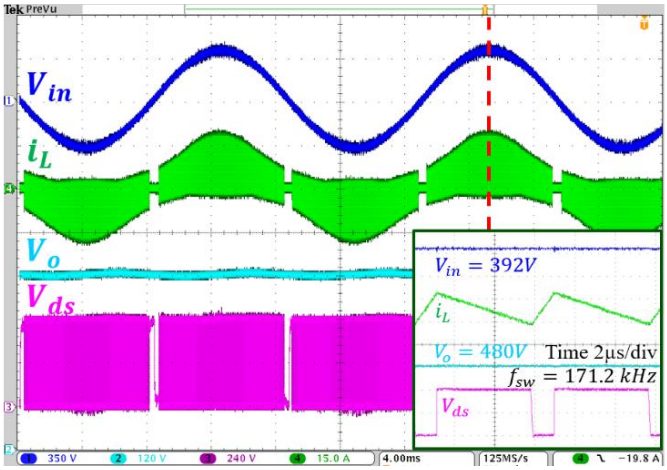


Fig. 11. 1.5 kW single-phase GaN-based CRM totem-pole PFC prototype.



(a) Waveforms of the input voltage, input current, and output voltage.



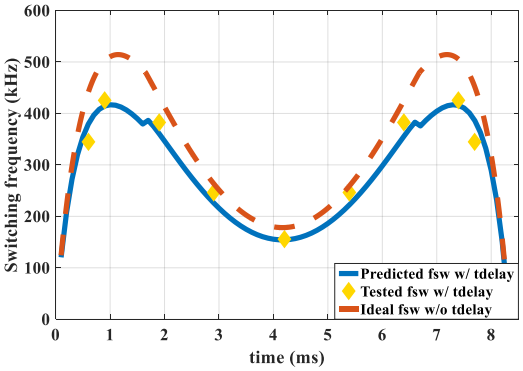
(b) Waveforms of the input voltage, inductor current, device voltage, and output voltage.

Fig. 12. Experimental waveforms of the 1.5 kW single-phase GaN-based CRM PFC at full load with the proposed delay compensation by adopting the modified converter model.

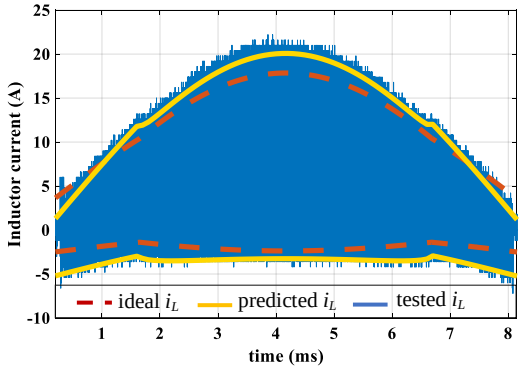
To further verify the current sensing delay impact, the proposed compensation approach, and the converter modeling, experimental results are compared with the predicted converter performances, including switching frequency, inductor current, and input current. Fig. 13 shows the comparison results of the tested and estimated PFC at full load with the current sensing delay. Compared with the ideal case without current sensing delay, converter switching frequency decreases, and the inductor current has larger current ripple. Also, the input current is distorted with worse THD. As a result, the measured full-load efficiency is 98.78% with 18.44 W loss, which is 3 W higher than the ideal case.

Fig. 14 illustrates the comparison results of the tested and estimated PFC at full load with the proposed delay compensation by adopting the modified converter model. As can be seen, the PFC input current overlaps with the ideal waveform without extra distortion, and the inductor current ripple is not enlarged. Although the peak switching frequency is still lower than the ideal case, the average switching frequency is enhanced compared to the case without compensation. Also, the tested full-load efficiency increases to 98.9% with 16.4 W loss.

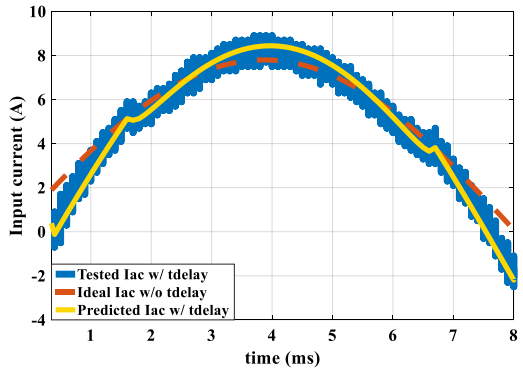
In addition, the predicted converter performances match with the tested results very well, validating the accuracy of the converter modeling. The PFC prototype is also tested at various load conditions ranging from 0.25 load to full load, and Fig. 15 presents the tested and estimated efficiency and current THD with and without ZCD delay compensation. With the proposed compensation method for current sensing delay, both the PFC efficiency and input current THD are improved. The peak efficiency increases to almost 99%, and the current THD is below 5% in all testing points.



(a) Tested and predicted switching frequency at full load.

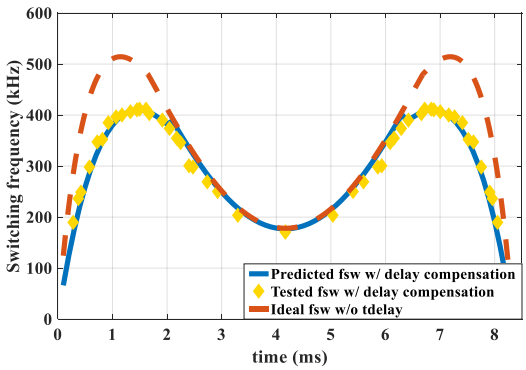


(b) Tested and predicted inductor current at full load.

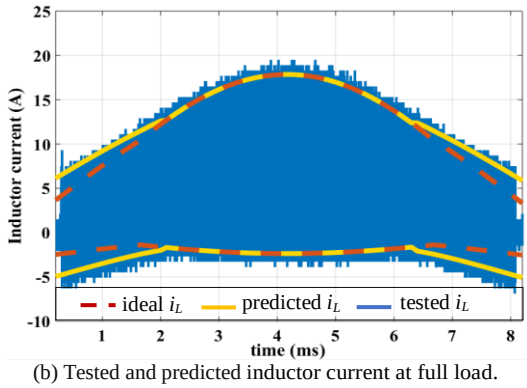


(c) Tested and predicted input current at full load.

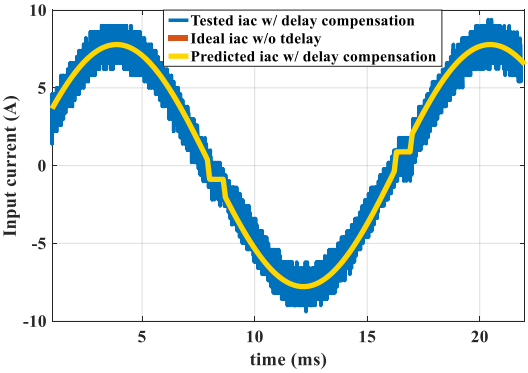
Fig. 13. Comparison of the tested and predicted switching frequency, inductor current, and input current of the CRM PFC prototype at full load with the current sensing delay and no compensation.



(a) Tested and predicted switching frequency at full load.

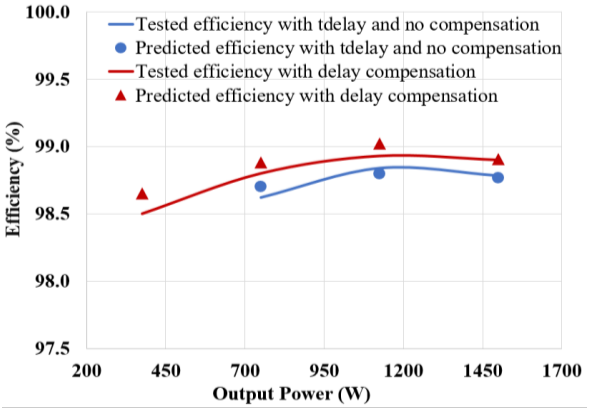


(b) Tested and predicted inductor current at full load.

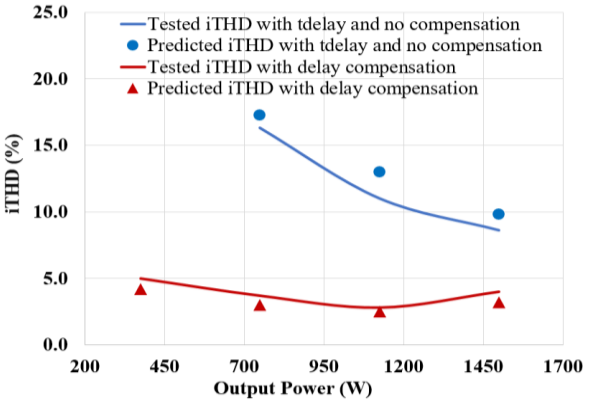


(c) Tested and predicted input current at full load.

Fig. 14. Comparison of the tested and predicted switching frequency, inductor current, and input current of the CRM PFC prototype at full load with delay compensation via the modified converter model.



(a) Tested and predicted efficiency at different loads.



(b) Tested and predicted input current THD at different loads.

Fig. 15. Tested and predicted efficiency and input current THD of the CRM PFC prototype at different loads (blue – with t_{delay} and no compensation; red – with the proposed delay compensation).

VI. Conclusions

A detailed analysis and no-cost method are proposed in this paper to address the issues of switching noise disturbance and current sensing delay in the high-frequency GaN-based CRM totem-pole PFC converter. To reject the high di/dt noise, qualification time is added in the DSP when passing the ZCD signal. The overall current sensing delay arises from different ZCD time errors and causes slower switching frequency, larger inductor current, worse input current THD, and higher converter loss. A CSD embedded converter model is proposed to compensate the ZCD time delay, and loss modeling of the CRM totem-pole PFC is illustrated. The proposed theory has been successfully demonstrated with a 1.5 kW PFC prototype. Experimental results vadiate the effect of the current sensing delay and the accuracy of the modeling. With the proposed compensation method, average switching frequency is enhanced, and inductor current ripple is reduced. Also, converter efficiency and input current THD are both improved.

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