Medium Voltage (13.8 kV) Transformer-less Grid-Connected DC/AC Converter Design and Demonstration Using 10 kV SiC MOSFETs

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***Abstract*—Medium voltage (MV) power converters using high voltage (HV) Silicon Carbide (SiC) power semiconductors result in great benefits in weight, size, efficiency and control bandwidth. However, challenges still exist on the components design considering HV insulation and noise immunity requirements in the MV SiC based power converter. A 5-level MMC based transformer-less grid-connected dc/ac converter is developed for 13.8 kV medium voltage grid using 10 kV SiC MOSFETs. The key components, including gate driver with high dv/dt immunity and fast reliable protection, isolated power supply with low parasitic capacitance, voltage/current sensors with high noise immunity, and passives following related insulation standard are provided. A 25 kV dc-link phase-leg is demonstrated, and the experimental results are presented.**

Keywords—medium voltage converter, 10 kV SiC MOSFET, grid application, high dv/dt

I. Introduction

In recent years, high voltage (HV) SiC devices (>3.3 kV) have been rapidly developed. Wolfspeed/Cree has released the third-generation 10 kV/20 A SiC MOSFET. With optimized doping in the drift and JFET regions, the specific on-resistance achieved 100 mΩ•cm^2 [1]. The reliability of the body diode was also enhanced, resulting in the exclusion of the external anti-parallel diode.

The HV SiC power semiconductors have dramatic improvements on breakdown voltage, specific on-resistance, switching speed and operating temperature. These advantages result in benefits for SiC based converters in the following aspects including 1) Direct device substitution, leading to efficiency improvement and corresponding reduced cooling; 2) Topology simplification, especially saving the bulky and lossy low frequency transformers; 3) New/enhanced functionality/ applications thanks to the higher control bandwidth and faster dynamic response. There are already some efforts in MV converter development using HV SiC devices. SiC devices have been applied in MV motor drives for high speed motors [2]. There is also research on the HV SiC based converter for grid applications [3],[4]. A SiC-based solid-state transformer has been developed in order to achieve significant weight reduction [5],[6]. A 250 kW/12.4 kV PV inverter using 10 kV SiC MOSFET H-bridge module was proposed in [7]. An impedance measurement unit is built for 4.16 kV AC system ranging from 0.1 Hz to 1 kHz [8].

In this research, a grid-connected dc/ac converter for medium voltage (MV, e.g. 13.8 kV) microgrid is designed and demonstrated, using Wolfspeed/Cree third-generation 10 kV/20 A SiC MOSFETs without external anti-parallel diodes, as shown in Fig. 1. The paper is organized as follows: 10 kV SiC characteristics related to the converter design is introduced in section II, and the converter specification and detailed converter design including all key components in the converter (e.g. gate driver, isolated power supply, passives, etc.) is presented in section III. The phase-leg prototype with 25 kV dc-link is demonstrated with testing results in section IV.

This work is supported by the Power America Program.

Fig. 1. 10 kV SiC MOSFET.

II. 10 kV SiC MOSFET Characteristics

As a novel power semiconductor, there is no commercial datasheet for the third-generation 10 kV SiC MOSFET. Therefore, it is essential to characterize it by device users. This paper only focuses on the device output characteristics which impact the converter design.

A. Static Characteristics

The static characteristics, including output characteristics of the MOSFET (forward) and diode (reverse) and the parasitic capacitance, need to be tested. The output characteristics of the MOSFET and diode are necessary for power loss estimation and cooling system design, while the parasitic capacitance can be used for the gate driver design.

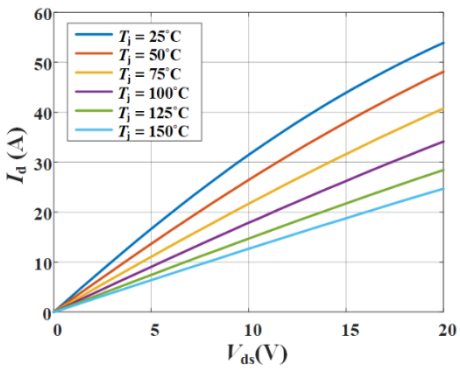


Fig. 2. Output characteristics of MOSFET.

Considering a high gate-source v_{gs} causes the breakdown or degradation of the MOSFET's gate and a low v_{gs} results in a higher on-state resistance, a trade-off value, which is 15 V,

is commonly selected for the 10 kV SiC MOSFET. Fig. 2 shows the output characteristics of the MOSFET when v_{gs} = 15 V under various junction temperatures. The on-state resistance of the MOSFET can be represented as:

$$R_B(T_j) = R_{B,25}\left(\frac{T_j + 273}{298}\right)^{\alpha_T} \quad (1)$$

where $R_{B,25}$ is the base resistance at 25 ˚C and $\alpha_{T,MOS}$ is the temperature coefficient of R_B. $R_{B,25}$ is 307 mΩ and the extracted temperature coefficient α_T is 2.5.

Previous 10 kV SiC MOSFETs required an external diode integrated in the module as the anti-parallel diode because of the low reliability of the body diode. In this case, the diode consists of the external diode and body diode in parallel and the diode characteristics were published in [9]. With the improvement of the body diode, the external diode can be removed. The diode characteristics under various junction temperatures are shown in Fig. 3. The body diode resistance and the MOSFET's ON resistance are nearly the same considering the resistance of the drift region dominates in both resistances. Therefore, the resistance of the diode can also be described by (1).

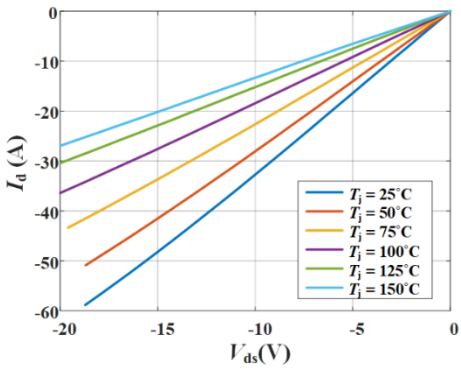


Fig. 3. Output characteristics of 10 kV SiC MOSFET's body diode.

The external diode also highly impacts the parasitic capacitance, especially drain-source capacitance C_{ds}. C_{ds} is significantly reduced by removing the external diode. The parasitic capacitance without the external diode is shown in Fig. 4.

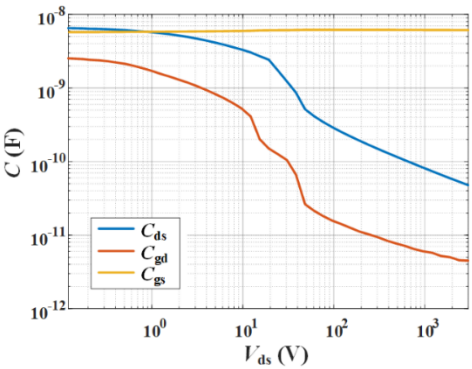


Fig. 4. Parasitic capacitance of 10 kV SiC MOSFET.

The gate-source capacitance C_{gs} can be seen as constant and equals to 6 nF. The gate-drain capacitance C_{gd} and drain-source capacitance C_{ds} are related to the drain-source voltage and can be represented as:

$$C_{gd} = \frac{C_{gdi}}{\sqrt[3]{v_{ds}}},\ C_{ds} = \frac{C_{dsi}}{\sqrt{v_{ds}}} \quad (2)$$

where C_{gdi} and C_{dsi} are the capacitance when v_{ds} = 1 V. C_{gdi} and C_{dsi} are 64.5 pF and 2.55 nF.

B. Switching Characteristics

The focus of switching characteristics includes *dv/dt* and switching losses. The switching losses are important for the cooling system design while *dv/dt* is necessary for the noise immunity and insulation design. The negative gate bias is selected as -5 V to safely hold v_{gs} below the threshold voltage in the off-state, and also not exceeds negative breakdown voltage. The turn-off and turn-on gate resistances are 3 Ω and 15 Ω respectively, achieving a same level of *dv/dt* both during turn-off and turn-on transients. The switching characteristics are tested in the double pulse test (DPT) platform, as shown in Fig. 5. A typical switching waveform of 10 kV SiC MOSFET is given in Fig. 6. The switching losses and *dv/dt* at various load currents and junction temperatures and under rated dc voltage (i.e. 6.25 kV) are shown in Fig. 7 and Fig. 8.

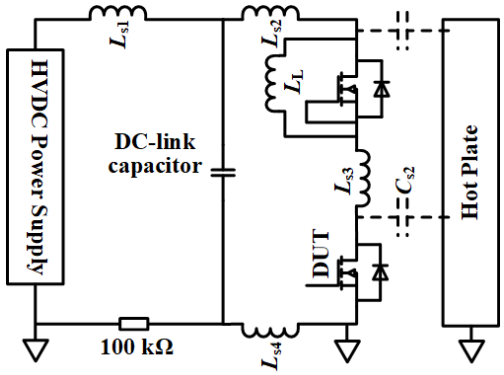


Fig. 5. Double pulse test platform of 10 kV SiC MOSFET.

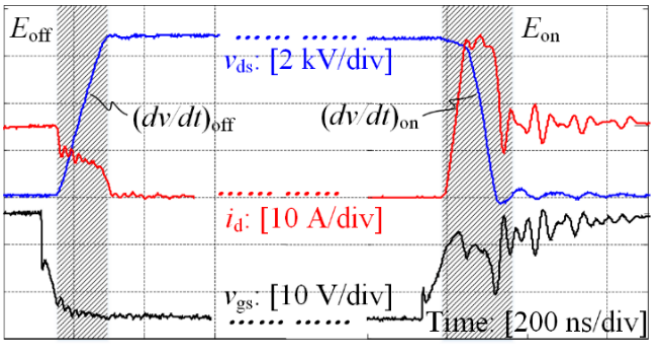


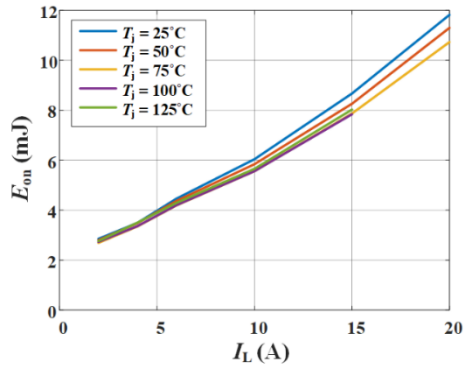
Fig. 6. Switching waveforms of 10 kV SiC MOSFET.

The switching losses, including turn-on loss E_{on} and turn-off loss E_{off}, are nearly the same at various junction temperatures, but increase with increasing load currents I_L. E_{on} and E_{off} can be represented by:

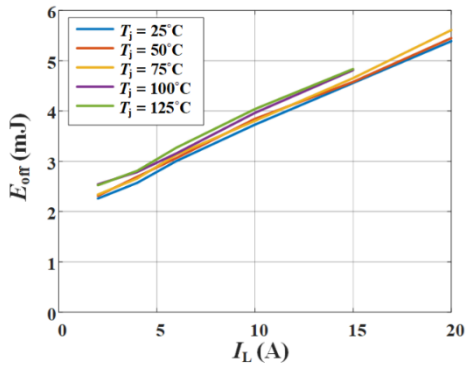
$$E_{on} = a_{Eon2} I_L^2 + a_{Eon1} I_L + a_{Eon0} \quad (3)$$

$$E_{off} = a_{Eoff1} I_L + a_{Eoff0} \quad (4)$$

where a_{Eon2}, a_{Eon1} and a_{Eon0} are fitting coefficients to describe the turn-on loss at various load currents, while a_{Eoff1} and a_{Eoff0} are used for turn-off loss. Their values are given in Table I.

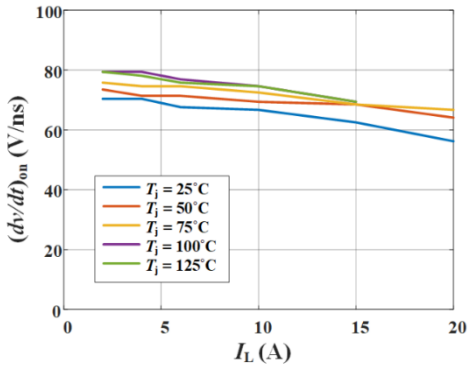


(a) turn-on loss

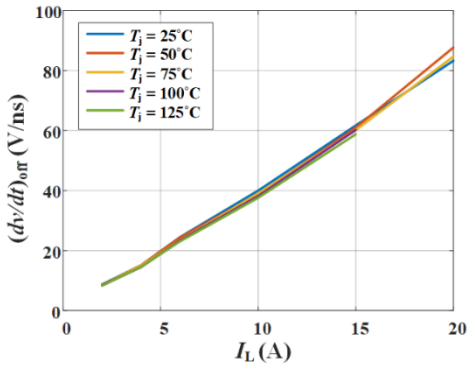


(b) turn-off loss

Fig. 7. Switching losses for a 10 kV SiC MOSFET at various junction temperatures, load currents and 6.25 kV rated dc voltage.



(a) *dv/dt* during turn-on transient



(b) *dv/dt* during turn-off transient

Fig. 8. *dv/dt* for a 10 kV SiC MOSFET at various junction temperatures, load currents and 6.25 kV rated dc voltage.

The *dv/dt* during the turn-on transient $(dv/dt)_{on}$ increases with elevating junction temperature and decreases with increasing load current. The *dv/dt* during the turn-off transient $(dv/dt)_{off}$ is nearly independent of the junction temperature and significantly increases with increasing load current. The *dv/dt* can be described by:

$$\left(dv/dt\right)_{on} = \left(a_{von1} I_L + a_{von0}\right)\left[1 + a_{vonT}\left(T_j - 298\text{K}\right)\right] \quad (5)$$

$$\left(dv/dt\right)_{off} = a_{voff1} I_L + a_{voff0} \quad (6)$$

where a_{von1}, a_{von0}, a_{voff1} and a_{voff0} are fitting parameters for *dv/dt* during switching transients, and a_{vonT} is the temperature coefficient of *dv/dt* during the turn-on transient. The parameter values for *dv/dt* are also given in Table I according to test results.

TABLE I. SWITCHING CHARACTERISTIC PARAMETERS

	Switching Loss		*dv/dt*	
	Parameter	**Value**	**Parameter**	**Value**
Turn-on	a_{Eon2}	0.0094 mJ/A^2	a_{vonT}	0.09 /K
	a_{Eon1}	0.289 mJ/A	a_{von1}	-0.77 V/ns/A
	a_{Eon0}	2.25 mJ	a_{von0}	73 V/ns
Turn-off	a_{Eoff1}	0.196 mJ/A	a_{voff1}	4.17 V/ns/A
	a_{Eoff0}	1.85 mJ	a_{voff0}	0

C. Short Circuit Characteristics

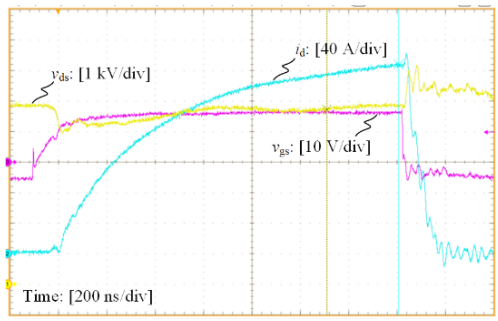


Fig. 9. Short circuit waveforms at 6.25 kV dc voltage.

The short-circuit characteristics are vital for determining the short circuit protection in the gate driver design. The short circuit protection response time should be shorter than the short circuit withstand time. The short circuit withstand time can be estimated according to the power loss during the short circuit and the thermal model considering the die structure. The short circuit waveforms at 6.25 kV dc voltage are shown in Fig. 9. The saturation current is 250 A and the power loss is 1.7 J with a short circuit time of 1.4 µs. The saturation current and power loss are nearly constant at various junction temperatures, and just slightly increases with elevated junction temperatures with a coefficients of 0.2 A/K and 1.2 mJ/K. Therefore, the power loss at higher junction temperature (i.e. 125 ˚C) and longer short circuit time can be obtained according to the test results at lower junction temperature and shorter short circuit time, and can be described by:

$$E_{SC} = a_{SC1}\left(t_{SC} - t_0\right) + a_{SC0} \quad (7)$$

where t_{SC} is the short circuit duration time, and t_0 is the time duration when the MOSFET current reaches the saturation value and equals 1.4 µs. a_{SC0} is the power loss during t_0 and equals 1.7 J. a_{SC0} is determined by saturation current and dc link voltage and equals to 1.56 J/µs. The short circuit withstand time can be estimated using a die model based on the power loss in (7) [10], and is longer than 2 µs.

III. Converter Design

A. Specifications of Converter

The specifications of the grid-connected dc/ac converter are listed in Table II. Considering the key technical challenge is the application of 10 kV SiC MOSFET, the focus of this paper is the HV SiC based converter design.

TABLE II. Specifications of DC/AC Converter

Parameter	Value
Power rating	100 kVA
Nominal voltage rating	13.8 kV (-12% ~ +10%)
Power factor	Four-quadrant
TDD	< 5%
Ambient temperature	-25ºC ~ 55ºC
Control frequency	10 kHz

The third harmonic injection cannot be applied in the transformer-less grid-connected converter. Therefore, the dc-link voltage needs to be 25 kV in 13.8 kV ac grid considering 10% overvoltage.

B. Topology Selection

In order to achieve 25 kV dc-link as well as 13.8 kV ac output, a 5-level power converter is required using 10 kV SiC MOSFETs (i.e. operating at 6.25 kVdc for each device). There are three options, including 5-level neutral point clamped (NPC), flying capacitor converter (FCC), and modular multilevel converter (MMC). NPC and FCC have benefits in weight and volume thanks to less passives. However, it is very difficult to limit the stray inductance of commutation paths in 5-level NPC and FCC. The large stray inductance will cause severe voltage spike and power loss during switching transients, especially for fast switching 10 kV SiC MOSFET. Furthermore, considering the superior voltage/power scalability, redundancy, and operation availability, 5-level MMC using the half-bridge submodule is selected for the 25 kVdc/13.8 kVac converter, as shown in Fig. 10.

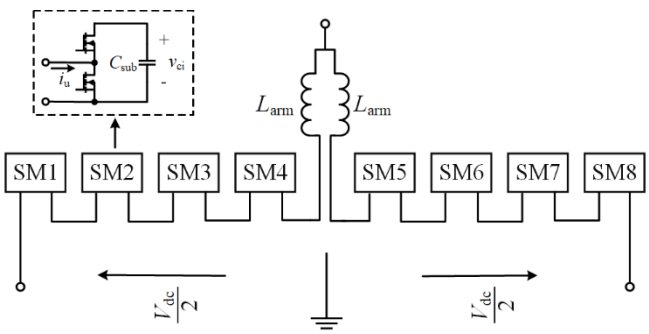


Fig. 10. 5-level MMC with half-bridge submodule.

C. Gate Driver Design

The gate driver should be designed considering basic functions, protection, and noise immunity.

The basic functions consist of gate positive and negative bias, gate resistances, and signal isolation. The gate positive and negative gate bias are selected as +15 V and -5 V, as introduced in Section II. The turn-on and turn-off gate resistances are 15 Ω and 3 Ω, respectively. The gate signal is transmitted and isolated by the optic fiber.

The protections consist of short circuit protection, under voltage lock-out, and fiber optic based communication check. The undervoltage lock-out and communication check have been widely applied for HV Si IGBT and can be leveraged for 10 kV SiC MOSFETs. The high *dv/dt* (100 V/ns) can induce a significant interference for the short circuit protection. The short circuit withstand time of 10 kV SiC MOSFET is also much shorter than conventional HV Si IGBT, requiring a faster short circuit protection. A FPGA-based short circuit protection for 10 kV SiC MOSFET has been proposed to achieve < 2 µs response time and meanwhile avoid interference [10]. The protection can also be implemented with analog circuit [11].

The interference caused by high *dv/dt* impacts the gate driver performance in many aspects. In a half-bridge configuration, with increasing *dv/dt* during lower device's turn-on transient, v_{gs} of upper switch may be charged higher than the gate threshold voltage through C_{gd}. Similarly, during the turn-off transient, a negative spurious gate voltage would be induced, leading to degradation of the upper switch if its magnitude exceeds the maximum allowable negative biased gate voltage acceptable to the semiconductor device itself. The maximum v_{gs} spike can be obtained by assuming that all current flowing though C_{gd} charges C_{gs}:

$$\Delta v_{gs} = \frac{\int_0^{v_{dc}} C_{gd} dv}{C_{gs}} \tag{8}$$

where C_{gd} and C_{gs} are given in (2). The calculated maximum v_{gs} spike is 5.5 V. Therefore, the cross-talk suppression is not necessary in the gate driver circuit. The high *dv/dt* will also induce a large common mode current (hundreds of mA) flows through the grounding and power supply system of the gate driver. It is recommended to separate the analog GND and digital GND in the gate driver board. The gate driver will also be interfered by radiated noise. In order to avoid the radiated noise interference, a filter is necessary for critical signals in the gate driver board. The gate driver of a half bridge is shown in Fig. 11.

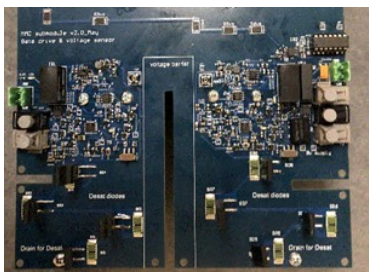


Fig. 11. Gate driver board of a half-bridge.

D. Gate Driver Power Supply

Two of major challenges in the gate driver power supply design are low parasitic capacitance and high voltage insulation capability.

The high *dv/dt* between the MOSFET's source and ground induces a large displacement current through the parasitic capacitance of the gate driver power supply. The current will

cause interference both in the gate driver board and in 120 V utility power. With optimized winding design for the isolated transformer, the capacitance can be reduced to < 3 pF [12], resulting in a displacement current of 0.3 A. It is not easy to measure the electro-magnetic interference (EMI) level using a spectrum analyzer due to the high ambient noise. However, the EMI level can be modeled and estimated using the parasitic capacitance of the gate driver power supply and *dv/dt* given in (5) and (6). A common mode EMI filter is necessary on the 120 V utility power.

The high *dv/dt* increases the amount of partial discharge (PD) in cavities in the solid insulation, causing a serious degradation of insulation materials. There is no industry standard regarding the insulation design for HV SiC based converters. Here, the conventional IEC standard for 13.8 kV grid is used for insulation design [13]. Compared to insulation paper and Kapton tape, the silicon gel with vacuum potting process is the more reliable and effective solution to achieve high voltage insulation, especially under high *dv/dt*. The gate driver power supply is shown in Fig. 12.

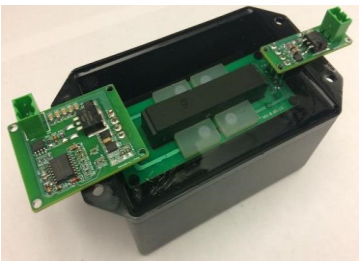


Fig. 12. Gate driver power supply.

E. Thermal Management Design

Due to a higher requirement on reliability of grid-connected converters and over current under abnormal cases (e.g. ground faults), it is preferred to overdesign the cooling system in grid applications. The maximum junction temperature in normal operation is selected as 80 ˚C. The power loss of 10 kV SiC MOSFET can be estimated according to (1), (3) and (4) with T_j = 80 ˚C. The power loss of one single device with 10 kHz control frequency (i.e. 2.5 kHz switching frequency in 5-level MMC) is 12 W. The maximum allowable temperature rise from the junction to the ambient is 25 ˚C considering the maximum ambient temperature of 55 ˚C. Therefore, the junction-to-ambient thermal resistance should be lower than 2.08 K/W. The junction-to-heatsink thermal resistance of 10 kV SiC MOSFET is 0.4 K/W. Therefore, the heatsink-to-ambient thermal resistance should be lower than 1.68 K/W. Forced air cooling is used and the fan can be selected based on thermal resistance-airflow-pressure curves. Because there is only a single die in the 10 kV SiC MOSFET module as shown in Fig. 1, the cooling system is not a limitation in the converter design. However, the cooling design becomes complicated if multiple dies are packaged in the module.

F. Voltage/Current Sensor

Due to the compact design of the SiC based converter, sensors are very close to the noise source and can be easily disturbed. Therefore, the submodule dc voltage sensor and arm current sensor will be required to have high noise immunity. The Σ-Δ analog-to-digital converter (ADC) feedback method is considered to meet the high noise immunity requirement. However, a sample delay, which is half control cycle, should be considered in the control design. Fiber optics, instead of cable, is used as the communication between the voltage/ current sensors and converter controller. The parasitic capacitors between the sensors and noise sources should be minimized as well.

G. Passive Components

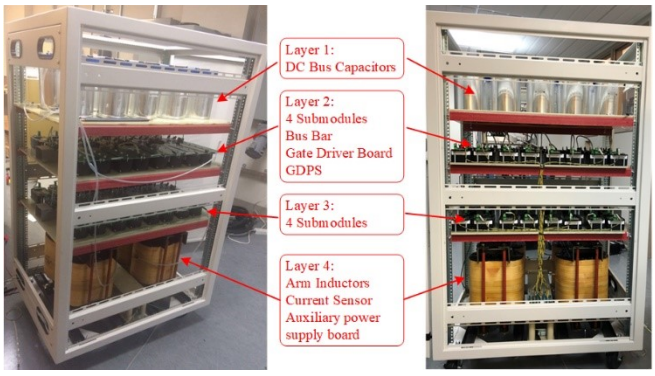
The selection method of the submodule capacitance and arm inductance have been provided in [14],[15]. The dc-link capacitance is selected as 8.75 μF and the peak-peak voltage variation in the submodule capacitor is smaller than 15%. The arm inductance is selected as 90 mH and the arm current ripple is smaller than 10%.

The arm inductor will experience high *dv/dt*, resulting in an insulation challenge for arm inductor design. The HV insulation design of the arm inductor also follows IEC standard for 13.8 kV grid requirement [11] with consideration of transient overvoltage including lightning and switching overvoltage. Vacuum pressure impregnation (VPI) is applied for insulation enhancement.

IV. Prototype and Experimental Validation

A. Prototype Demonstration

A 5-level MMC based dc/ac phase-leg for 13.8 kV asynchronous microgrid PCS using 10 kV SiC MOSFET is built as shown in Fig. 13. The estimated efficiency with 10 kHz control frequency is 99.3%. The specific power and power density of the developed DC/AC converter are 0.14 kW/kg and 80 kW/m^3, respectively. The arm inductor is a major contributor to weight and size. Without the inductor, the specific power and power density could reach 1.17 kW/kg and 240 kW/m^3, respectively. Therefore, an improved inductor design is necessary in order to further reduce the weight and size. Furthermore, a large percentage of the power converter volume is the high voltage insulation material which does not scale proportional with increasing power. Therefore, the specific power and power density of the converter will improve for higher power ratings (e.g. 1 MW).



(a) right side view (b) left side view

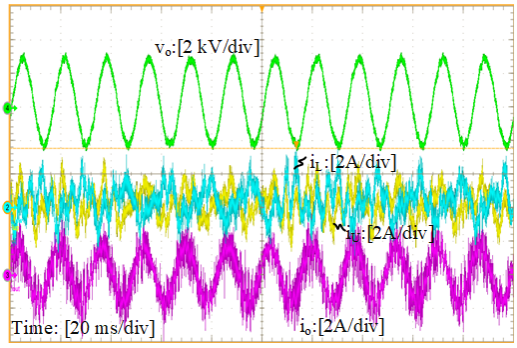
Fig. 13. Grid-connected dc/ac converter prototype.

B. Experimental Validation

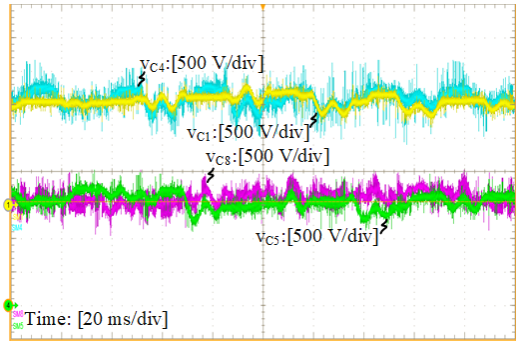
Fig. 14 shows the phase-leg test at 6 kV dc-link including a) ac output, and b) submodule dc voltage. The differential voltage probe is used to measure the submodule voltage, but it is not viable at higher voltage rating (> 6 kV dc-link). Dc voltages of all submodules are within a range of 15% variation. The functions of the submodule dc voltage sensor and voltage balancing control are validated.

Fig. 15 shows the phase-leg test waveforms including a) PWM output voltage at 12 kV dc-link and b) ac output voltage

at 25 kV dc-link, demonstrating the normal operation for developed 10 kV SiC MOSFET based dc/ac converter. The high voltage probe will suffer from PD issue to measure the PWM output voltage at a dc-link voltage higher than 12 kV. Therefore, at 25 kV dc-link (i.e. nominal dc-link), only the ac output voltage is tested.

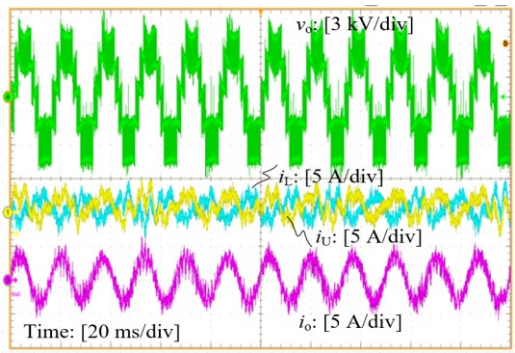


(a) ac output

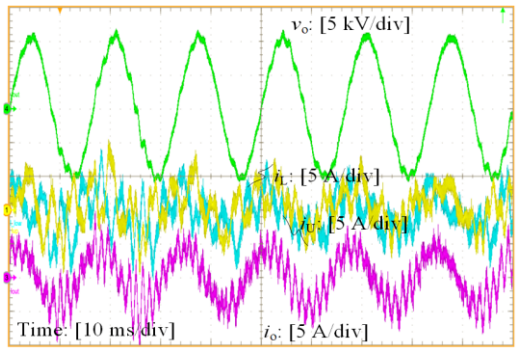


(b) submodule dc voltage

Fig. 14. Phase-leg test at 6 kV dc-link.



(a) PWM output at 12 kV dc-link



(b) ac output at 25 kV dc-link

Fig. 15. Phase-leg experimental waveforms at 12 kV and 25 kV dc-link.

V. Conclusion

A 100 kW/13.8 kVac grid-connected dc/ac converter using 10 kV SiC MOSFET design is detailed in this paper, with all key component designs provided. 25 kV dc-link is necessary and 5-level MMC is selected. The gate driver with high *dv/dt* immunity and fast protection and isolated power supply with low parasitic capacitance are developed. The voltage/current sensors with high noise immunity are implemented. The insulation design follows the 13.8 kV grid requirement in IEC standard. A 25 kV dc-link phase-leg prototype is demonstrated with testing results.

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References

[1] J. Palmour, L. Cheng, V. Pala, E. Brunt, D. Lichtenwalner, G. Wang, J. Richmond, M. O'Loughlin, S. Ryu, S. Allen, A. Burk, C. Scozzie, "Silicon carbide power MOSFETs: breakthrough performance from 900 V up to 15 kV," in *IEEE Internaional Symposium on Power Semiconductor Devices and ICs* (*ISPSD*), 2014, pp. 79-82.

[2] H. Li, K. Potty, Z. Ke, J. Pan, Y. Chen, F. Zhang, M. Sabbagh, W. Perdikakis, G. Li, X. Ye, R. Na, J. Zhang, L. Xu, J. Wang, "Hardware design of a 1.7 kV SiC MOSFET based MMC for medium voltage motor drives," in *IEEE Applied Power Electronics Conference and Exposition* (*APEC*), pp. 1649-1655, 2018.

[3] L. Zheng, X. Han, Z. An, R. Kandula, K. Kandasamy, "Modular universal converter for MVDC applications," in *IEEE Energy Conversion Congress and Exposition* (*ECCE*), pp. 5544-5551, 2018.

[4] S. Madhusoodhanan, K. Mainali, A. Tripathi, A. Kadavelugu, K. Vechalapu, D. Patel, S. Bhattacharya, "Comparative evaluation of 15 kV SiC IGBT and 15 kV SiC MOSFET for 3-phase medium voltage high power grid connected converter applications," in *IEEE Energy Conversion Congress and Exposition* (*ECCE*), pp. 1-8, 2016.

[5] A. Huang, L. Wang, Q. Tian, Q. Zhu, D. Chen, W. Yu, "Medium voltage solid state transformers based on 15 kV SiC MOSFET and JBS diode," in *IEEE Annual Conference of the Industrial Electronics Society* (*IECON*), pp. 6996-7002, 2016.

[6] J. W. Kolar, G. I. Ortiz, "Solid state transformer concepts in traction and smart grid applications," ETH report, 2013.

[7] S. Ji, Z. Zhang, F. Wang, "Overview of high voltage SiC power semiconductor devices: development and application," *CES Transaction on Electrical Machines and Systems*, vol. 1, no. 3, pp. 254-264, Sep. 2017.

[8] I. Cvetkovic, Z. Shen, M. Jaksic, C. Dimarino, F. Chen, D. Boroyevich, R. Burgos, "Modular scalable medium-voltage impedance measurement unit using 10 kV SiC MOSFET PEBBs," in *IEEE Electric Ship Technologies Symposium* (*ESTS*), pp. 326-331, 2015.

[9] S. Ji, S. Zheng, F. Wang, L. Tolbert, "Temperature-dependent characterization, modeling and switching speed limitation analysis of third generation 10 kV SiC MOSFET," *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 4317-4327, May. 2018.

[10] S. Ji, M. Laitinen, X. Huang, J. Sun, W. Giewont, F. Wang, L. Tolbert, "Short circuit characterization and protection of 10 kV SiC MOSFET," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1755-1764, Feb. 2019.

[11] X. Huang, S. Ji, J. Palmer, L. Zhang, L. Tolbert, F. Wang, "Parasitic capacitor's impact on siwtching performance in a 10 kV SiC MOSFET based converter," in *IEEE Workshop on Wide Bandgap Power Devices and Applications* (*WiPDA*), pp. 311-318, 2018.

[12] L. Zhang, S. Ji, S. Gu, X. Huang, J. Palmer, W. Giewont, F. Wang, L. Tolbert, "Design considerations of high-voltage-insulated gate drive power supply for 10 kV SiC MOSFET in medium-voltage application," in *IEEE Applied Power Electronics Conference and Exposition* (*APEC*), pp. 425-430, 2019.

[13] "High-voltage test techniques – general definitions and test requirements," IEC 60060-1.

[14] Z. Xu, H. Xiao, Z. Zhang, "Selection methods of main circuit parameters for modular multilevel converters," *IET Renewable Power Generation*, vol.10, no.6, pp.788-797, Jul. 2016.

[15] Y. Li, E. Jones, F. Wang, "Circulating current suppressing control's impact on arm inductance selection for modular multilevel converter", *IEEE Trans. Power Electron.*, vol. 5, no. 1, pp. 182-188, Mar. 2017.