DC Impedance Model of MMC Considering Capacitor Voltage and Circulating Current Dynamics

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***Abstract*—The modular multilevel converter (MMC) is regarded as a competitive choice for future dc grids at high and medium voltage levels. To study the dc grid stability, a few MMC dc impedance models have been proposed, but their accuracy is limited by the assumption of ideal submodule voltage or neglecting the circulating current control. In this paper, a more accurate MMC dc impedance model is developed considering both the submodule capacitor voltage and circulating current dynamics. Simulation and experiment results indicate that the developed model matches with the actual MMC better than state-of-art models and can predict the dc system stability correctly.**

Keywords—CPL, dc grid, dc impedance, MMC, small-signal stability

I. Introduction

The modular multilevel converter (MMC), which was originally invented for high voltage direct current (HVDC) applications, has also become a promising topology in medium voltage direct current (MVDC) systems due to the benefits of high efficiency, modularity for manufacturing, and low harmonics [1-5]. However, the dc system stability with MMCs has not been thoroughly investigated. An impedance-based stability analysis method, which investigates the relationship of source side converter impedance and load side converter impedance at the point of common connection (PCC) using Nyquist stability criterion, has been widely used for such interconnected-stability studies [6, 7]. To apply the same approach for dc grid stability analysis with MMCs, it is critical to developing an accurate MMC dc impedance model.

Several research efforts have been done to obtain the impedance models of MMC for system analysis. In [8], by using the MMC ac impedance model, the MMC ac bus stability was investigated but not the dc bus. In [9], both ac and dc impedances of MMC were derived, but it only considered the effects of circulating current control. The dc impedance model was simplified as an RLC branch without considering the effects of MMC control blocks. Another dc impedance model of MMC was developed in [10]. This model was developed for single line-to-ground (SLG) fault conditions with/without circulating current control. But the submodule capacitor voltage is assumed to be constant. Reference [11] developed a dc impedance model of MMC and analyzed the stability in MVDC applications, but this model relies on the assumption of large enough submodule capacitors, which ignores the submodule voltage dynamics. In [12], an average model represented by an equivalent two-level VSC (2L-VSC) was proposed. This model considered the effect of submodule capacitor voltage ripple. Therefore, it can reveal some particular dynamic behaviors of MMCs. However, it cannot predict the effect of circulating current dynamics due to the intrinsic limits of the equivalent two-level structure. Although the impedance models of MMC developed so far have addressed different issues, there are still some limitations due to the assumptions in the model-derivation process. Therefore, a refined MMC dc impedance model considering the effects of submodule capacitor voltage dynamics and circulating current suppression control is developed in this paper.

The rest of the paper is organized as follows. Section II describes the operation principle and control function blocks of MMC. Section III explains the proposed MMC dc impedance model. Moreover, the existing dc impedance models in [11] and [12] are further elaborated in section III, as a comparison with the proposed model. Section IV validates the proposed model through circuit-based simulations. In section V, the stability of a dc system consisting of an MMC and a constant power load (CPL) is analyzed using the proposed model and existing models, and the analysis results are compared with circuit-based simulations and experimental results.

II. Operation Principles and Control Strategies of MMC

A. Operation Principles of MMC

Fig. 1 shows the structure of a typical three phase modular multilevel converter, where there are two arms (one upper arm and one lower arm) in each phase. And there are N submodules (SMs) connected in series in each arm, together with an arm inductor L_{arm} and its parasitic resistance R_{arm}. Typically, each submodule can be a half-bridge circuit or a full-bridge circuit as shown in Fig. 2.

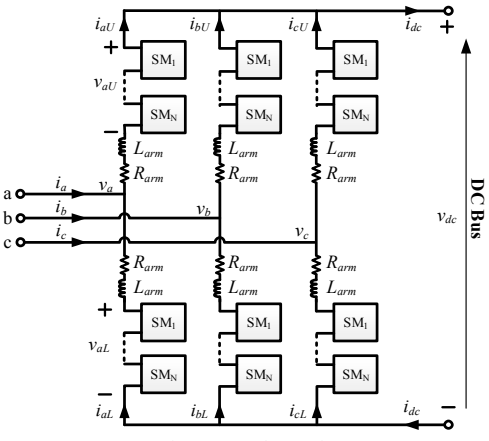
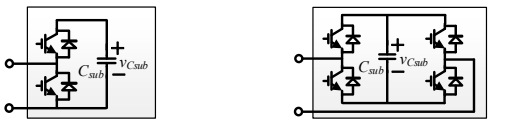


Fig. 1. Topology of MMC.



(a) Half bridge SM (b) Full bridge SM

Fig. 2. Circuits of submodules.

B. Control Strategies of MMC

Normally, there are three control blocks in MMCs. One is the converter function control block; one is the circulating current suppression control block; another is the submodule dc voltage balance control block [13].

The converter function control is a double-loop controller which includes the outer dc voltage and power control loop, and the inner current control loop [14-16]. In this paper, a dc voltage controlled MMC with unity power factor is illustrated as an example and the function control block is shown in Fig. 3. The outer dc voltage controller generates the *d* axis current reference I_{dref}. The *q* axis current reference I_{qref} is set to be 0 because of the assumptions of unity power factor. The inner current loop controls *d*-*q* axis currents using PI controllers and decoupling terms, respectively. Therefore, the *abc*-frame duty cycle d_a, d_b and d_c can be generated.

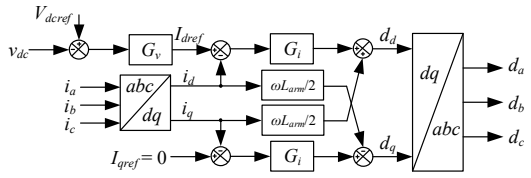


Fig. 3. Converter function control block of MMC.

A circulating current suppression control is implemented in MMC to eliminate the second-order circulating current as shown in Fig. 4 [17, 18]. The circulating current is controlled through a proportional resonance (PR) controller. The circulating current control duty cycle d_{xcir} is subtracted from the function control duty cycle d_x obtained by Fig. 3 to generate the upper arm duty ratio d_{xU} and lower arm duty ratio d_{xL} in phase *x* (*x*=*a*, *b*, *c*).

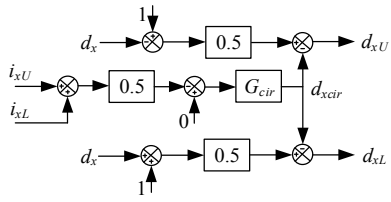


Fig. 4. Circulating current suppression control block of MMC.

Additionally, the submodule capacitor dc voltage is balanced with a sorting method as shown in Fig. 5. By sorting the sensed submodule voltage, each SM module can be assigned with a corresponding duty cycle [4, 19]. In this paper, the submodule capacitor dc voltages are assumed to be well-balanced with this control.

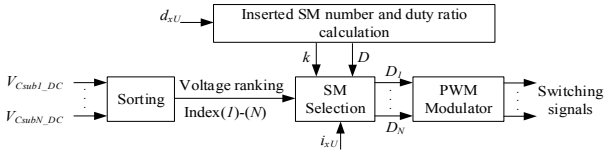


Fig. 5. SM voltage balance control block of MMC.

III. DC Impedance Models of MMC

The mathematical representation of MMC can be obtained as follows. First, the real switching function of each arm is a stepped waveform which indicates when the submodules are connected or bypassed. In this paper, it is regarded as a continuous waveform for simplicity. Therefore, the average switching function is considered, which is defined as $S_{xU(L)}$. Also, the submodule voltages in each arm are assumed to be identical. Hence, the relationships among the arm voltage $v_{xU(L)}$, arm current $i_{xU(L)}$, SM capacitor voltage $v_{CsubU(L)}$, and average switching function $S_{xU(L)}$ can be obtained as (1) and (2). In addition, the line current i_x, phase voltage v_x, dc current i_{dc}, and dc voltage v_{dc} can be obtained as (3)-(6). Note that the currents are defined with the respective flow path as in Fig. 1.

$$\begin{cases} v_{xU} = NS_{xU}v_{CsubU} \\ v_{xL} = NS_{xL}v_{CsubL} \end{cases} \tag{1}$$

$$\begin{cases} S_{xU}i_{xU} = -C_{sub}\dfrac{dv_{CsubU}}{dt} \\ S_{xL}i_{xL} = -C_{sub}\dfrac{dv_{CsubL}}{dt} \end{cases} \tag{2}$$

$$i_x = i_{xU} - i_{xL} \tag{3}$$

$$v_x = \frac{1}{2}\left[L_{arm}\frac{di_x}{dt} + R_{arm}i_x - (v_{xU} - v_{xL})\right] \tag{4}$$

$$i_{dc} = \sum_{x=a,b,c} i_{xU} = \sum_{x=a,b,c} i_{xL} \tag{5}$$

$$v_{dc} = (v_{xU} + v_{xL}) - R_{arm}(i_{xU} + i_{xL}) - L_{arm}\frac{d(i_{xU} + i_{xL})}{dt} \tag{6}$$

Based on (1) - (6), the relationships between v_{dc} and i_{dc} represented by switching functions could be obtained as (7).

$$v_{dc} = \frac{1}{3}\sum_{x=a,b,c} N(S_{xU}v_{CsubU} + S_{xL}v_{CsubL}) - \frac{2}{3}R_{arm}i_{dc} - \frac{2}{3}L_{arm}\frac{di_{dc}}{dt} \tag{7}$$

A. Review of Two Prior-Art DC Impedance Models of MMC

1) Model I

The modeling method in [11] is referred to as model I in this paper. In model I, the submodule capacitors are assumed to be large enough and their voltages are assumed to be identical and constant, which are V_{dcref}/N. Average switching function $S_{xU(L)}$ is equivalent to $d_{xU(L)}$. Therefore, (7) can be reformed as (8).

$$v_{dc} = \frac{1}{3}\sum_{x=a,b,c}(d_{xU} + d_{xL}) \cdot V_{dcref} - \frac{2}{3}R_{arm}i_{dc} - \frac{2}{3}L_{arm}\frac{di_{dc}}{dt} \tag{8}$$

According to the control block in Fig. 4, the sum of d_{xU} and d_{xL} can be represented by (9).

$$d_{xU} + d_{xL} = 1 - 2d_{xcir} \tag{9}$$

Therefore, the dc impedance model is derived as (10) and its corresponding dc terminal equivalent circuit is shown in Fig. 6. This model ignores the submodule capacitor voltage ripple. Therefore, it has some limitations as shown later in section IV and section V.

$$Z_{dc\_model\_I}(s) = \frac{2}{3}(G_{cir}V_{dcref} + R_{arm} + sL_{arm}) \tag{10}$$

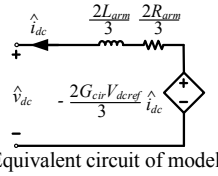


Fig. 6. Equivalent circuit of model I [11].

2) Model II

The modeling method in [12] is referred to as model II in this paper. It considers the capacitor voltage ripple and proposes an equivalent two-level VSC control model as shown in Fig. 7, with equivalent dc impedance and ac impedance as in (11) and in (12), where the voltage across C_{ac} as in (13) contains the capacitors voltage information.

$$Z_{dc\_model\_II}(s) = \frac{2}{3}R_{arm} + \frac{2}{3}sL_{arm} + \frac{N}{6sC_{sub}} \tag{11}$$

$$Z_{ac}(s) = \frac{1}{2}R_{arm} + \frac{1}{2}sL_{arm} + \frac{1}{sC_{ac}} \tag{12}$$

$$C_{ac} = 8C_{sub}/[N\left(1 - \frac{3k^2}{8}\right)]$$
$$\text{where, } k = \frac{V_d}{V_{dc}/2} \tag{13}$$

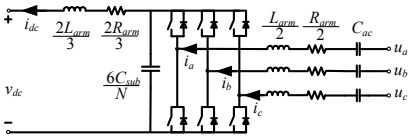


Fig. 7. Equivalent circuit of model II [12].

The dc impedance equation in (11) is derived based on the energy conservation of the sub-module capacitors. However, the dynamics are not revealed. Thereby, to analyze the system stability considering the internal dynamics of MMC, the equivalent circuit in Fig. 7 has to be used. Because there is no complete mathematical expression for the equivalent circuit, this model is difficult to be adopted for stability analysis. In addition, the circulating current control effect cannot be revealed by this model.

B. Proposed DC Impedance Model of MMC

Considering the limitations of the existing models, this paper proposes a dc impedance model considering the MMC internal dynamics: submodule capacitor voltage ripple and circulating current suppression control.

By defining d_{dc} as in (14) and assuming all the submodule capacitor voltages are the same, (7) can be written as (15). Accordingly, the linearized small-signal equivalent circuit of MMC dc terminal can be illustrated as shown in Fig. 8.

$$d_{dc} = \frac{1}{3}\sum_{x=a,b,c}(d_{xU} + d_{xL}) \tag{14}$$

$$v_{dc} = Nd_{dc}v_{Csub} - \frac{2}{3}R_{arm}i_{dc} - \frac{2}{3}L_{arm}\frac{di_{dc}}{dt} \tag{15}$$

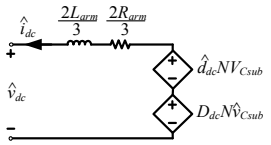


Fig. 8. Small-signal equivalent circuit of MMC dc terminal.

From Fig. 8, it can be noted that if $\hat{d}_{dc}$ and $\hat{v}_{Csub}$ can be represented by $\hat{i}_{dc}$ and $\hat{v}_{dc}$, respectively, the dc impedance model of MMC can then be derived. Therefore, to develop the model, four transfer functions are defined first as in (16).

$$G_{di}(s) = \frac{\hat{d}_{dc}(s)}{\hat{\imath}_{dc}(s)}, \quad G_{dv}(s) = \frac{\hat{d}_{dc}(s)}{\hat{v}_{dc}(s)}$$
$$G_{vi}(s) = \frac{\hat{v}_{Csub}(s)}{\hat{\imath}_{dc}(s)}, \quad G_{vv}(s) = \frac{\hat{v}_{Csub}(s)}{\hat{v}_{dc}(s)} \tag{16}$$

Based on (5) and according to Fig. 4, the transfer functions of $\hat{i}_{dc}$ to $\hat{d}_{dc}$ and $\hat{v}_{dc}$ to $\hat{d}_{dc}$ can be obtained as shown in (17).

$$G_{di}(s) = -\frac{2}{3}G_{cir}(s)$$
$$G_{dv}(s) = 0 \tag{17}$$

In addition, the expression of submodule capacitor voltage v_{Csub} is the foundation to derive the transfer functions $G_{vi}(s)$ and $G_{vv}(s)$. According to (2), the submodule capacitor voltage can be represented by $S_{xU(L)}$ as shown in (18) and $i_{xU(L)}$ as shown in (19), where, $M = 2V_d/V_{dc}$ is the modulation index, $I_s = \frac{I_d}{\sin\beta}$ is the magnitude of the fundamental-frequency component, α, β, φ and γ are phase angles, and v_{cir} and i_{cir} are the second-order circulating current related voltage and current. In this paper, assume a unity power factor application, so $\sin\alpha = 1$ and $\sin\beta = 1$. In addition, circulating current is assumed to be well suppressed by the control in Fig. 4. Thereby, $v_{cir} = 0$ and $i_{cir} = 0$.

$$S_{xU} = \frac{\frac{1}{2}V_{dc} - \frac{1}{2}V_{dc}M\sin(\omega t + \alpha) + v_{Cir}\sin(2\omega t + \varphi)}{V_{dc}}$$
$$S_{xL} = \frac{\frac{1}{2}V_{dc} + \frac{1}{2}V_{dc}M\sin(\omega t + \alpha) + v_{Cir}\sin(2\omega t + \varphi)}{V_{dc}} \tag{18}$$

$$i_{xU} = \frac{1}{3}i_{dc} - \frac{1}{2}I_s\sin(\omega t + \beta) + i_{cir}\sin(2\omega t + \gamma)$$
$$i_{xL} = \frac{1}{3}i_{dc} + \frac{1}{2}I_s\sin(\omega t + \beta) + i_{cir}\sin(2\omega t + \gamma) \tag{19}$$

By substituting (18) and (19) into (2), the upper arm SM capacitor voltage can be expressed as (20). It consists of a quasi-dc component, fundamental frequency component, second-order frequency component, and neglecting the higher-order frequency components [20, 21]. The lower arm SM voltages have the same frequency components, whereas, the fundamental frequency has the opposite sign. In this paper, all the submodule capacitor voltages are assumed to be the same. Therefore, the lower arm submodule voltage v_{CubL} is assumed to be the same as (20).

$$\frac{dv_{Csub}}{dt} = -\frac{1}{6C_{sub}}i_{dc} - \frac{1}{8C_{sub}}MI_s\cos(\alpha - \beta) + \frac{1}{4C_{sub}}I_s\sin(\omega t + \beta) + \frac{1}{6C_{sub}}Mi_{dc}\sin(\omega t + \alpha) + \frac{1}{8C_{sub}}MI_s\cos(2\omega t + \alpha + \beta) \tag{20}$$

By substituting all the values, (20) can then be written as (21).

$$\frac{dv_{Csub}}{dt} \approx -\frac{1}{6C_{sub}}i_{dc} - \frac{MI_d}{8C_{sub}} + \frac{i_d}{4C_{sub}}\cos(\omega t) + \frac{Mi_{dc}}{6C_{sub}}\cos(\omega t) \tag{21}$$

By doing Laplace transformation on the differential equation of v_{Csub} in (21) based on (22) and (23), and neglecting the higher-order differential components, the transfer function $G_{vi}(s)$ can be obtained as in (24).

$$\cos x = \sum_{n=0}^{\infty} \frac{\cos(\frac{n\pi}{2})}{n!} x^n \tag{22}$$

$$\mathcal{L}\{x^n f(x)\} = (-1)^n \frac{d^n}{ds^n} \mathcal{L}\{f(x)\} \tag{23}$$

$$G_{vi}(s) = -\frac{1}{2C_{sub}s} + \frac{M}{6C_{sub}s} \tag{24}$$

Similarly, the transfer function $G_{vv}(s)$ can be obtained as shown in (27) based on (21) - (23), (25) and (26).

$$v_d(s) = \frac{V_{dcref}}{2} G_v(s) G_i(s) v_{dc}(s) \tag{25}$$

$$i_d(s) = G_v(s) \frac{T_i(s)}{1 + T_i(s)} v_{dc}(s) \tag{26}$$

where, $T_i(s) = \frac{G_i(s) V_{dcref}}{sL_{arm} + R_{arm}}$

$$G_{vv}(s) = \frac{\left(\frac{I_d G_v G_i V_{dcref}}{2} + \frac{V_d G_v T_i}{1 + T_i}\right) V_{dcref} - V_d I_d}{4C_{sub} V_{dcref}^2 s} - \frac{G_v T_i}{4C_{sub}(1 + T_i)s} - \frac{\left(\frac{G_v G_i V_{dcref}}{2} - V_d\right) I_{dc}}{3C_{sub} V_{dcref}^2 s} \tag{27}$$

Therefore, the dc impedance model of MMC could be obtained as (28), where $G_{di}(s)$, $G_{vi}(s)$ and $G_{vv}(s)$ can be seen in (17), (24) and (27), respectively.

$$Z_{dc}(s) = \frac{\frac{2}{3}(L_{arm}s + R_{arm}) - G_{di}(s) V_{dcref} - N G_{vi}(s)}{1 - N G_{vv}(s)} \tag{28}$$

IV. Validation of MMC DC Impedance Models

To validate the accuracy of the proposed dc impedance model of MMC, a circuit-based simulation is conducted in MATLAB/Simulink with the parameters and working conditions listed in Table 1. The simulation model is built based on the non-linear switching circuit of MMC. The dc impedance simulation results are obtained by injecting a small current perturbation (frequency range in the simulation: 1 Hz – 10 kHz) at MMC dc side, and doing FFT analysis on the measured dc current and dc voltage at the perturbation frequency.

TABLE 1. Components and Working Conditions of the MMC

Parameters	Value	Parameters	Value
DC bus voltage V_{dcref}	21 kV	Submodule DC voltage V_{Csub}	7 kV
Power rating P	1 MW	Submodule capacitor C_{sub}	70 μF
AC voltage $V_{LL,rms}$	13.8 kV	DC voltage PI controller	K_{pv}=0.01, K_{iv}=4
AC grid frequency f_o	60 Hz	AC current PI controller	K_{pi}=0.0029, K_{ii}=0.01
Arm inductor L_{arm} & its ESR R_{arm}	17 mH 1 mΩ	Circulating current PR controller	K_{pr}=0.3, K_{sr}=30
Submodule number per arm N	3	Switching frequency f_{sw}	5 kHz

The comparisons among the dc impedance models and simulation results are shown in Fig. 9. The blue-star curve is the circuit-based simulation result. It can be seen that model I (black curve) cannot predict the low-frequency (around 1-50 Hz) characteristics which is mainly caused by the neglect of capacitor voltage dynamics. Model II (green curve) cannot reveal the middle-frequency (around 12-1200 Hz) behavior which is related to the circulating current suppression control. The proposed model (red curve), considering both capacitor voltage dynamics and circulating current control effects, can match with the simulation results. Though due to the simplifications and linearization process of the submodule capacitor voltage, such as assuming v_{cir} = 0 and i_{cir} = 0 and ignoring high-order components, there is still a small dc offset of the proposed model compared with the circuit based simulation. This small dc offset will not affect the prediction of the dc system stability as shown in section V.

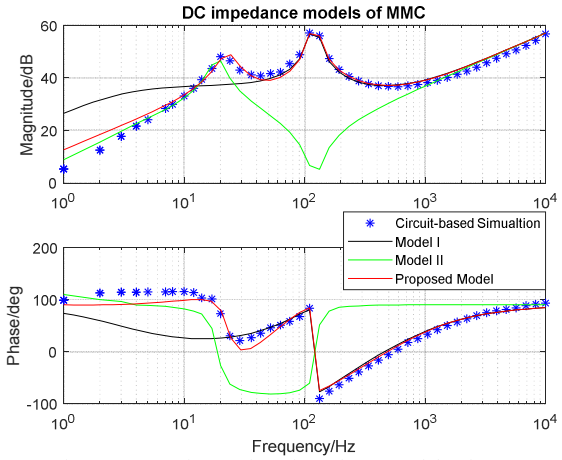


Fig. 9. Comparisons of DC impedance models of MMC.

V. Stability Analysis of a DC System with MMC

With the proposed dc impedance model, if connecting a standalone-stable MMC on a dc bus, the overall system stability can be predicted by analyzing the relationships of the impedances between the interconnected converters. By checking the RHP poles P_R and counterclockwise encirclements of (-1+j0) N_c on the Nyquist locus of the minor loop gain T_{minor}, which can be defined as $T_{minor} = Z_{MMC}/Z_L$ or $T_{minor} = Z_L/Z_{MMC}$, the system stability can be determined. If T_{minor} satisfies with $Z_R = P_R - N_c = 0$, the system would be stable; otherwise, it would be unstable.

A dc system consisting of the MMC feeding a constant power load (CPL) through the dc link as shown in Fig. 10 is studied in this paper, where the well-controlled MMC (in the simulation) or a two-level VSC (in the experiment) is regarded as a constant power load.

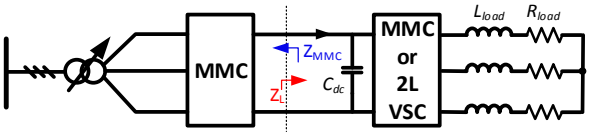


Fig. 10. Configuration of a system with an MMC feeding a CPL.

A. Simulation Results

Three cases with different control parameters have been studied to validate the effectiveness of the proposed MMC dc impedance model for system stability analysis. Note that the MMC and the load converter have been designed to be stable in the standalone operation, so if there were unstable phenomena, they should be caused by the interactions

between MMC and the load converter. In addition, the minor loop gain T_{minor} is defined as $T_{minor} = Z_L/Z_{MMC}$ in the analysis for these three simulations.

Simulation I: the same parameters as listed in Table 1.

In simulation I, the circuit uses the same parameters as listed in Table 1. Fig. 11(a) shows the Nyquist stability analysis diagram using model I and the proposed model. It can be observed that both model I and the proposed model predict that the RHP zero of T_{minor} Z_R is 0, which means that the system would be stable. Fig. 11(b) shows the bus voltage predicted by model II. As mentioned in section III, model II does not have a mathematical expression of closed loop dc impedance, the stability analysis using model II is conducted by time domain simulation in MATLAB/Simulink with the equivalent circuit in Fig. 7. Fig. 11 (c) shows the circuit-based simulation results of dc bus voltage, it can be seen that the system is stable. Therefore, the stability analysis results using the proposed model and existing models all correspond with the simulation results. Note that the part of the Nyquist contours not shown in the *GH*-plane in Fig. 11(a), Fig. 12(a) and Fig. 13(a) all go through the right half plane which will not affect the (-1+*j*0) encirclement counting for stability analysis.

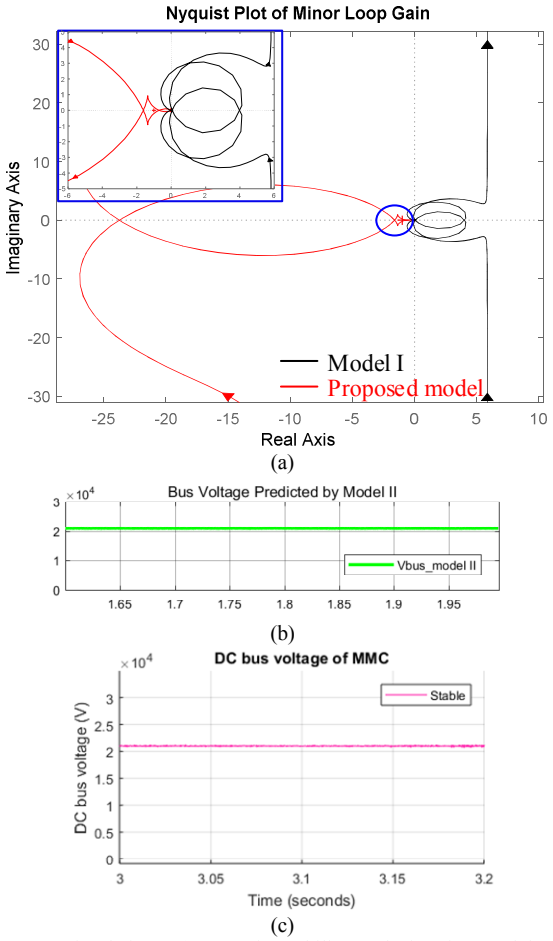


Fig. 11. Simulation I: (a) Nyquist stability analysis using model I and the proposed model, (b) stability analysis using model II, and (c) simulated dc bus voltage.

Simulation II: change of ac current PI controller.

In simulation II, the ac current controller G_i is changed to be k_{pi}=0.00029 and k_{ii}=0.001. Note that the standalone operation of MMC (MMC with a current load, instead of CPL) is kept to be stable. Fig. 12 (a) shows the system stability analysis results using the proposed model and model I. It can be seen that the proposed model predicts that the system would be unstable, since the RHP zero $Z_R = P_R - N_c = 0 + 4 = 4$. But model I predicts it to be stable since there are no encirclements of the critical point (-1+*j*0). Model II predicts the system to be unstable as shown in Fig. 12(b). The simulation of dc bus voltage as shown in Fig. 12(c) indicates that the system is unstable. Therefore, the proposed model and model II can predict the system stability correctly in this case, while model I is ineffective in this case because it neglects submodule capacitor voltage dynamics in its modeling process.

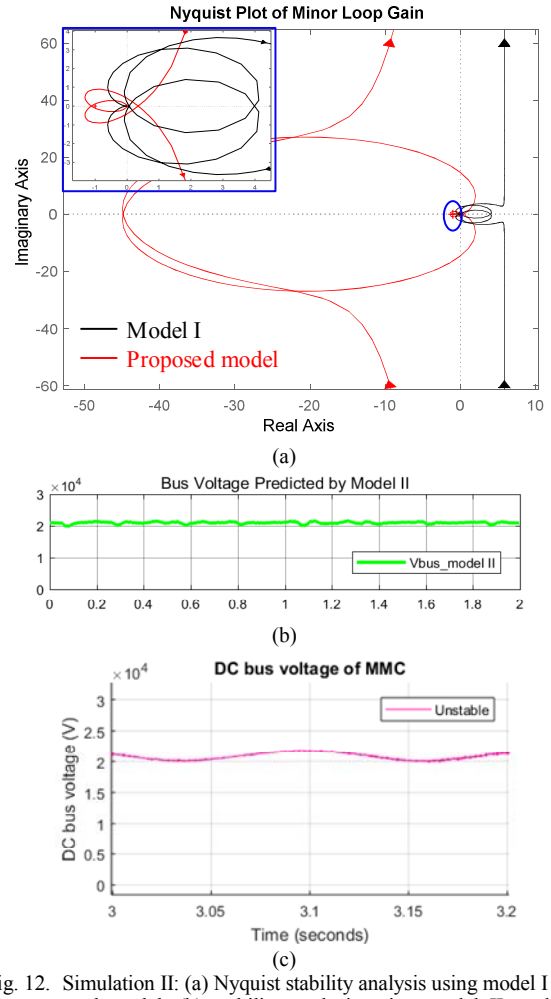


Fig. 12. Simulation II: (a) Nyquist stability analysis using model I and the proposed model, (b) stability analysis using model II, and (c) simulated dc bus voltage.

Simulation III: change of circulating current PR controller

In simulation III, the circulating current parameters are changed to be k_{pr}=0.5 and k_{sr}=1. From the analysis results, it can be observed that the proposed model shows that the system would be unstable ($Z_R = P_R - N_c = 0 + 2 = 2$). This prediction as shown in Fig. 13(a) agrees with the simulated unstable dc bus voltage as shown in Fig. 13(c). However, both model I and model II predict the system would be stable which are opposite of the dc bus voltage simulation results. Model I is inaccurate because of the lack of information of submodule capacitors' voltage dynamics. Model II cannot model the effects of the circulating current

suppressing control, therefore, it cannot reveal the second-order frequency component in dc bus voltage.

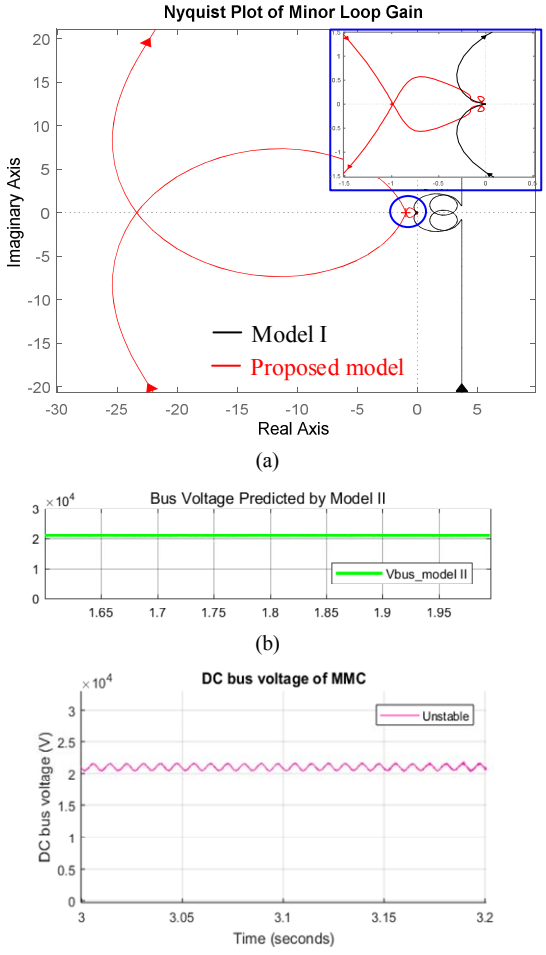


Fig. 13. Simulation III: (a) Nyquist stability analysis using model I and the proposed model, (b) stability analysis using model II, and (c) simulated dc bus voltage.

B. *Experimental Results*

The experiments are carried out with a flexible modular multilevel converter test-bed as introduced in [13] and a two-level VSC working as CPL. The MMC has 10 SMs on each arm and the working conditions and control parameters are listed in Table 2.

TABLE 2. PARAMETERS OF MMC IN EXPERIMENTS

Parameters	Value	Parameters	Value
DC bus voltage V_{dcref}	200 V	Power rating P	1.7 kW
AC voltage $V_{LL,rms}$	110 V	Submodule capacitor C_{sub}	2.2 mF
AC grid frequency f_o	60 Hz	Arm inductor L_{arm}	3 mH
Submodule number N	10	AC current PI controller	K_{pi}=0.05, K_{ii}=1.885
DC voltage PI controller	K_{pv}=0.4, K_{iv}=12	Circulating current PR controller	K_{pr}=0.4, K_{sr}=20

Similar as in section *A*, the stability analysis of the dc system is conducted using the proposed model and existing models first. And then the dc bus voltage is measured on the MMC-2LVSC testbed to validate the analysis results.

Test I: the same parameters as listed in Table 2

The MMC hardware uses the same parameters as listed in Table 2. Fig. 14 (a) shows the Nyquist stability analysis diagram. It can be observed that model I ($Z_R = P_R - N_c = 0 - 1 = -1$) predicts the system to be unstable, and the proposed model reveals that the RHP zero of T_{minor} Z_R is 0 ($Z_R = P_R - N_c = 0 - 0 = 0$), which means that the system is predicted to be stable. The simulation using model II as in Fig. 14(b) shows that the system is stable. Fig. 14(c) shows the measurement of a stable dc bus voltage and current. Therefore, in test I, the stability analysis results using the proposed model and model II match with the measurement, while model I cannot predict the system stability correctly.

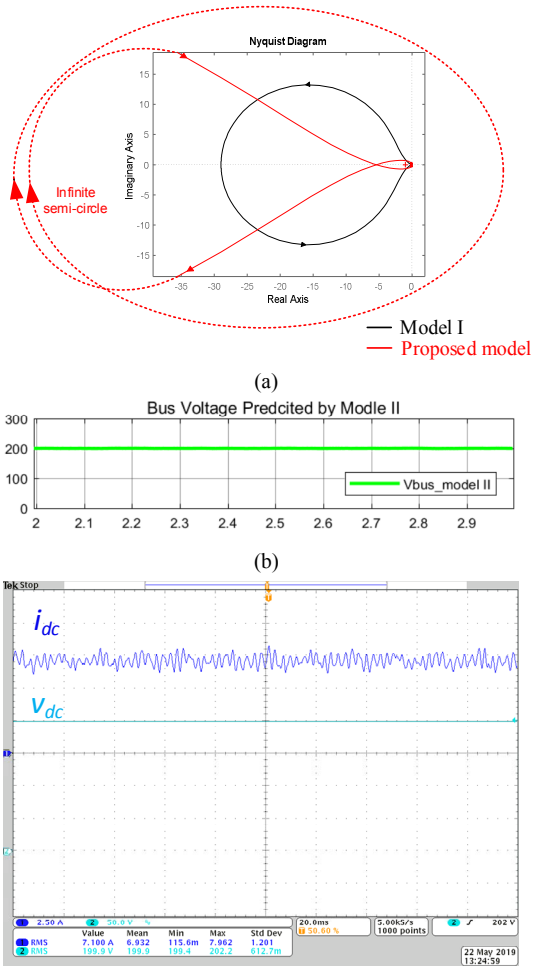
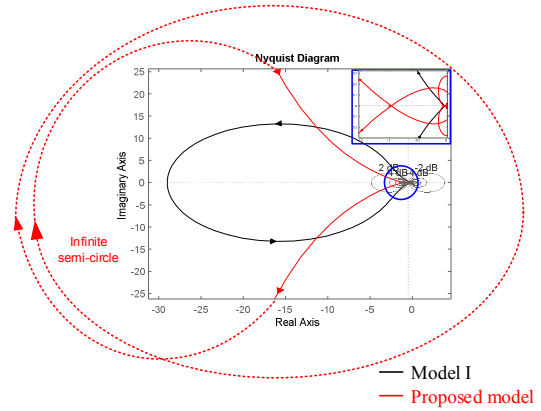


Fig. 14. Test I: (a) Nyquist stability analysis using model I and the proposed model, (b) stability analysis using model II, and (c) measurement of dc bus voltage.

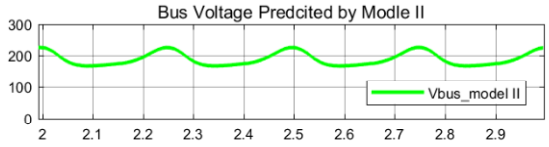
Test II: change of ac current PI controller

In test II, the ac current controller G_i is changed to be k_{pi}=0.005 and k_{ii}=0.1885. Still, the standalone operation of MMC is kept to be stable. Fig. 15 (a) shows the system stability analysis results using the proposed model and model I. It can be seen that the proposed model predicts that the system would be unstable, since the RHP zero Z_R is 2 ($Z_R = P_R - N_c = 0 + 2 = 2$). Model I predicts it to be unstable too because the RHP zero Z_R is -1 ($Z_R = P_R - N_c = 0 - 1 = -1$). The simulation of dc bus voltage using model II as shown in Fig. 15 (b) also indicates that the system is unstable. And the measurement results in Fig. 15(c) also shows that the system is unstable. Therefore, it

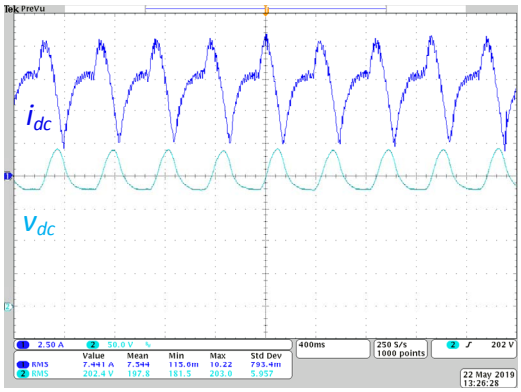
can be concluded that all the models can predict the system stability correctly in this case.



(a)



(b)



(c)

Fig. 15. Test II: (a) Nyquist stability analysis using model I and the proposed model, (b) stability analysis using model II, and (c) measurement of dc bus voltage.

In both test I and test II, model II can predict the system stability correctly. This is because the control parameters of the circulating current loop can only be changed within a small range due to the effects of control delays in the MMC testbed. Therefore, the ineffectiveness of model II cannot be revealed by the tests. However, the limitations of model II which is caused by neglecting the effects of circulating current control cannot be overlooked. In the future, by compensating the control delays in the testbed, the effects of the circulating current controller would be further investigated.

VI. Conclusions

A dc impedance model is proposed and used to conduct the stability analysis of a dc system. Compared with the prior-art MMC models, the proposed dc impedance model can match with the simulated results well and can predict the dc system stability correctly, due to the consideration of both the cell capacitor voltage ripple and circulating current dynamics. Simulation and experimental results have proven the effectiveness of the proposed MMC impedance model for dc system analysis.

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