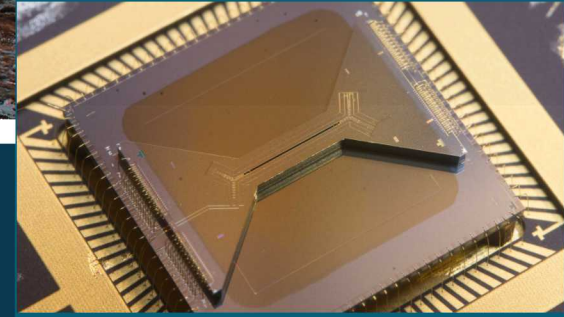
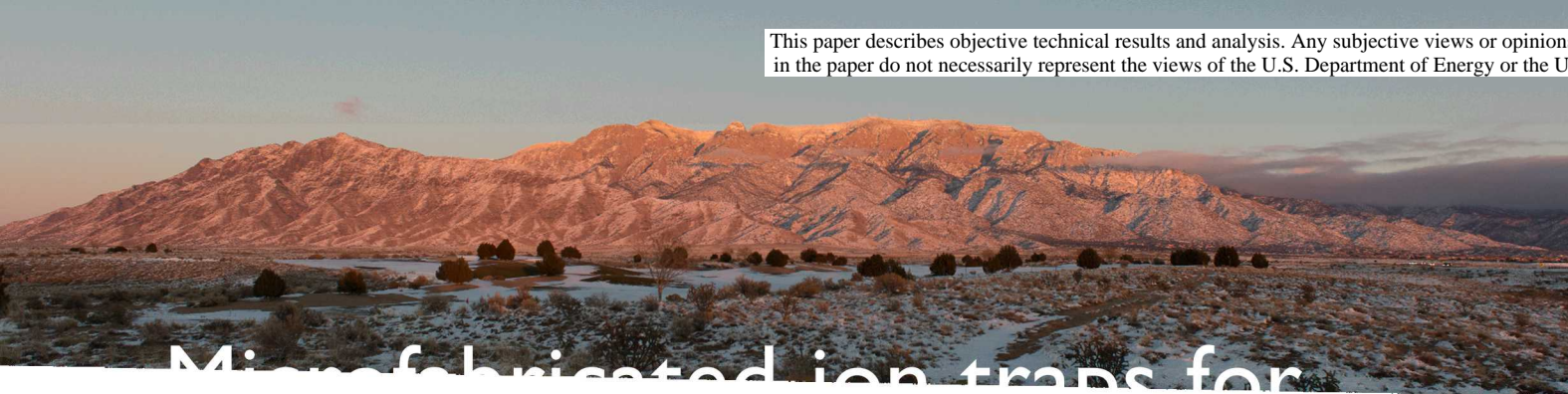
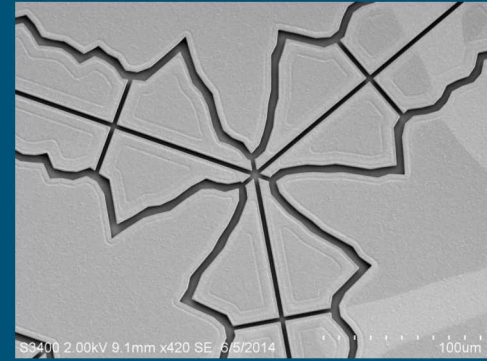
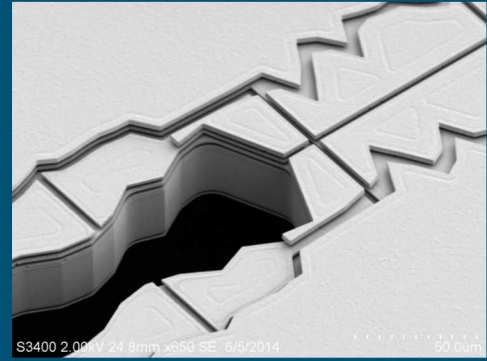
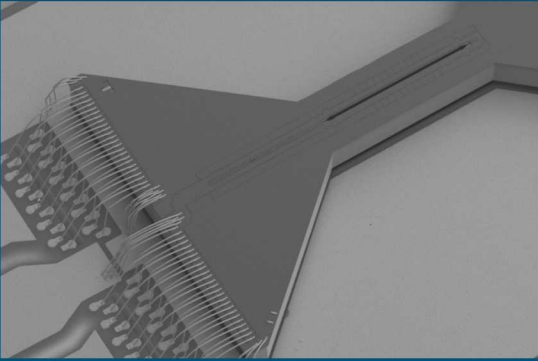


This paper describes objective technical results and analysis. Any subjective views or opinions that might be expressed in the paper do not necessarily represent the views of the U.S. Department of Energy or the United States Government.

SAND2020-0373C



# Microfabricated ion traps for LogiQal Qubits

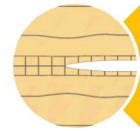


*PRESENTED BY*  
Peter Maunz, Susan Clark, Craig Hogle, Raymond Haltli, Daniel Lobser, Jessica Pehr,  
Melissa Revelle, Brandon Ruzic, Christopher Yale, and Matthew G. Blain

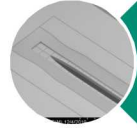


**IARPA**  
BE THE FUTURE

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Phoenix trap design



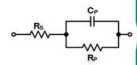
Phoenix trap fabrication and testing



Prompt-onset fields and ion heating



Phoenix package



Rf-dissipation



Peregrine trap



Quantum Scientific Open User Testbed (QSCOUT)

## Phoenix objectives

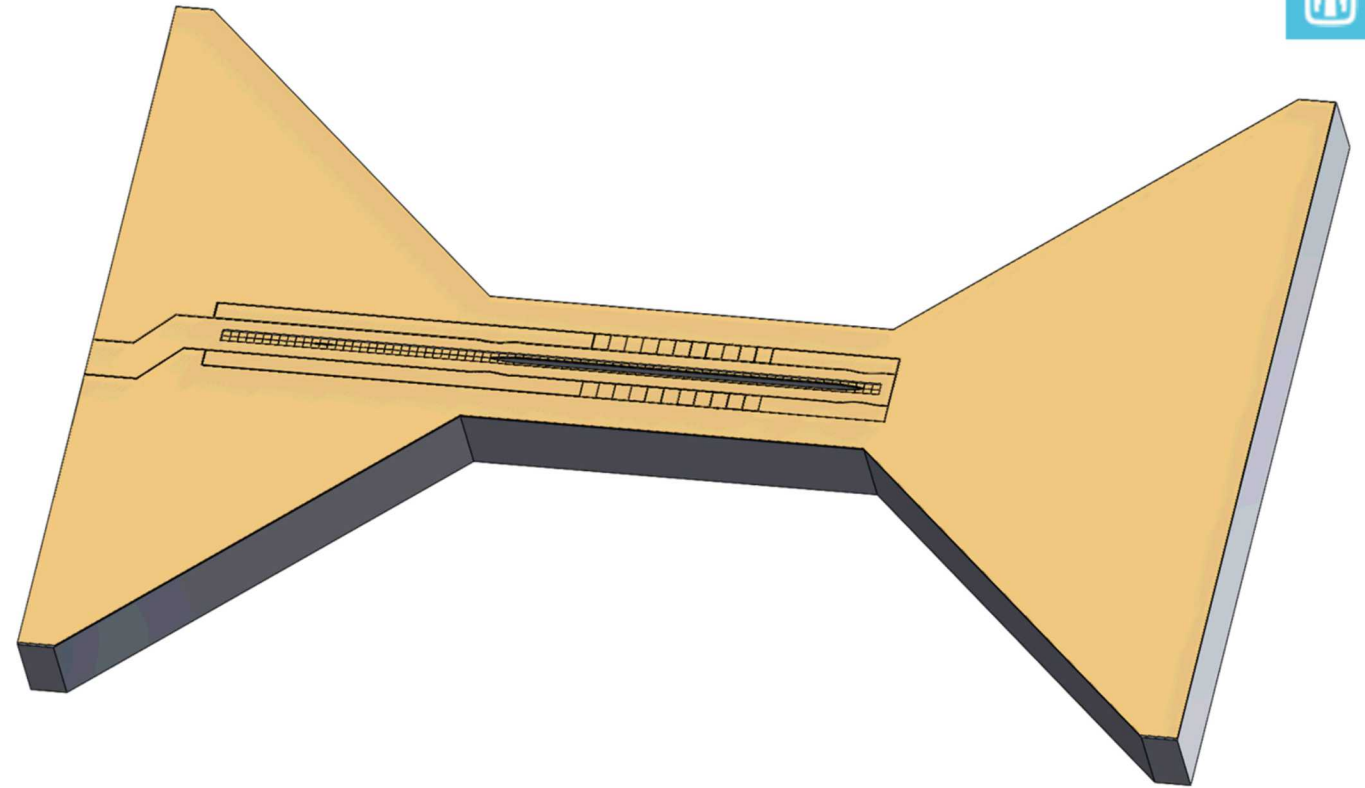
- High optical access platform
- Through-substrate slot for optical access
- Linear trap

### Improvements:

- Reduction of rf dissipation in device
- Additional electrode segmentation to control long ion chains
- Enable shuttling while maintaining trap characteristics
- Improve slot sidewall to enable continuous metal film

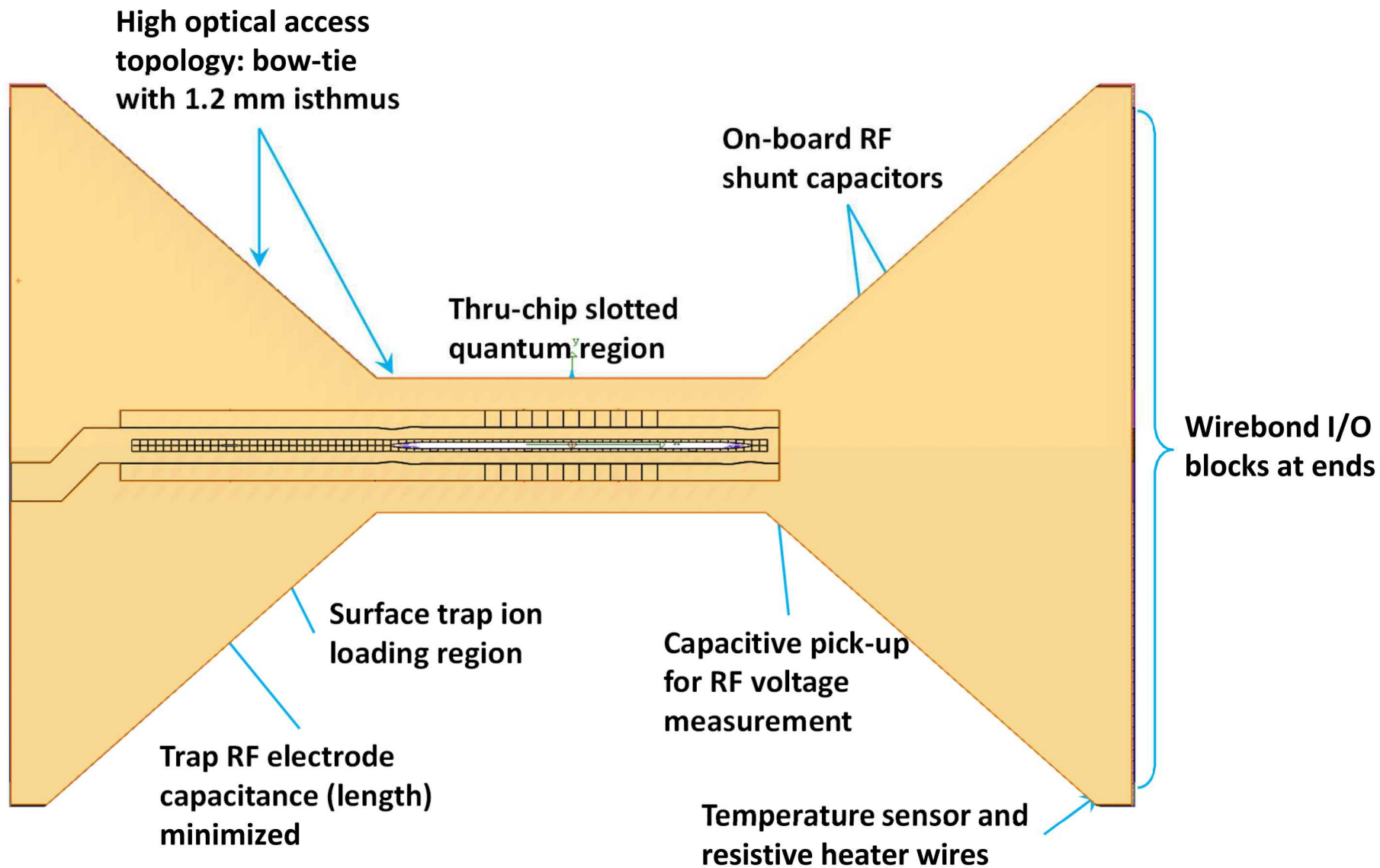
### Features:

- Integrated trench capacitors on device
- Packaging with solder die attach on custom SiN ceramic package (eliminates organics)



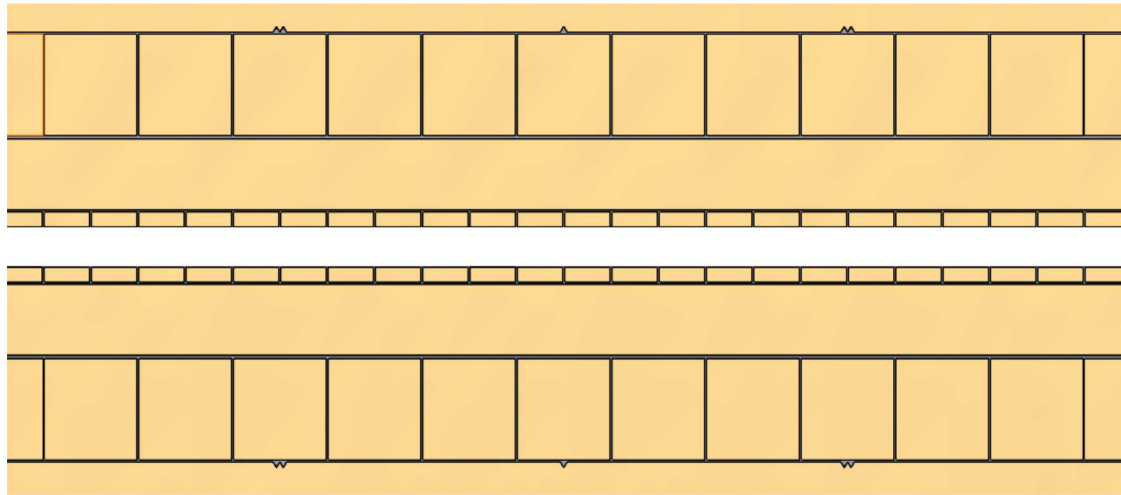
# Phoenix trap fabrication

## Design and features



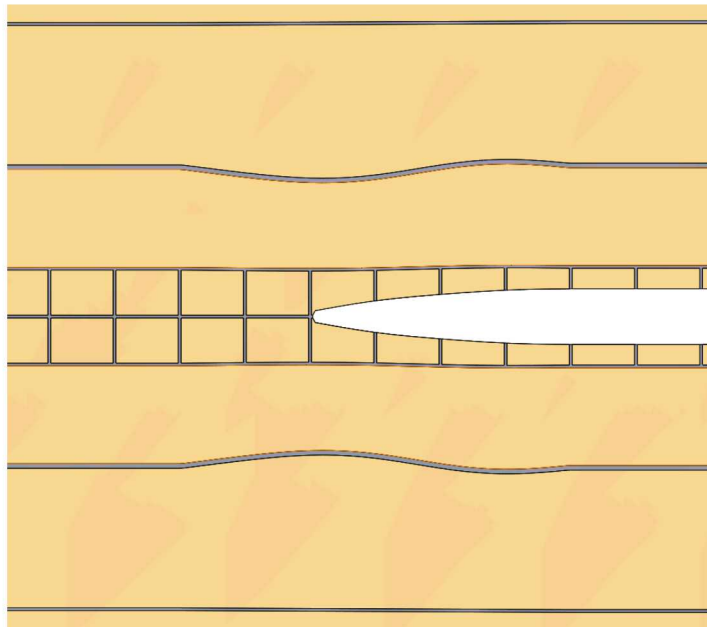
# Phoenix trap fabrication

## Trap regions



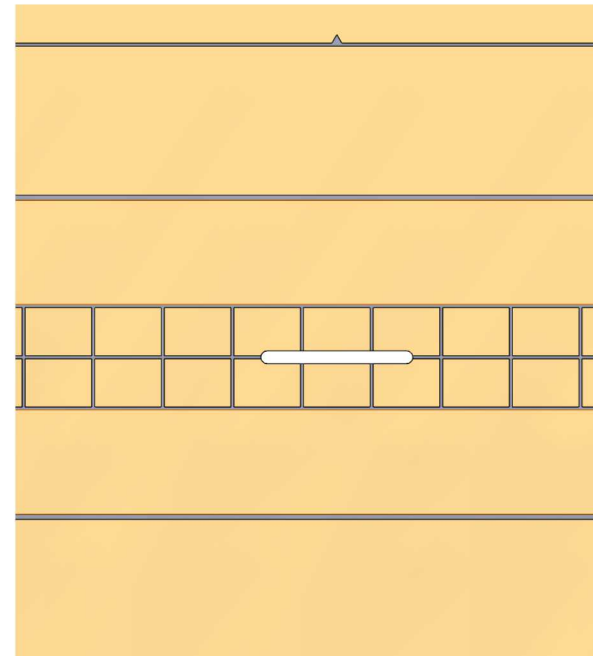
### Quantum region

- Segmentation of 22 inner electrode pairs and 11 outer pairs for better control of ion chains and spatial re-ordering of ions
- $22 \times 70 \mu\text{m} = 1540 \mu\text{m}$  long
- Ion height  $70 \mu\text{m}$



### Transition

- 9 degrees of freedom
- Low spatial frequencies

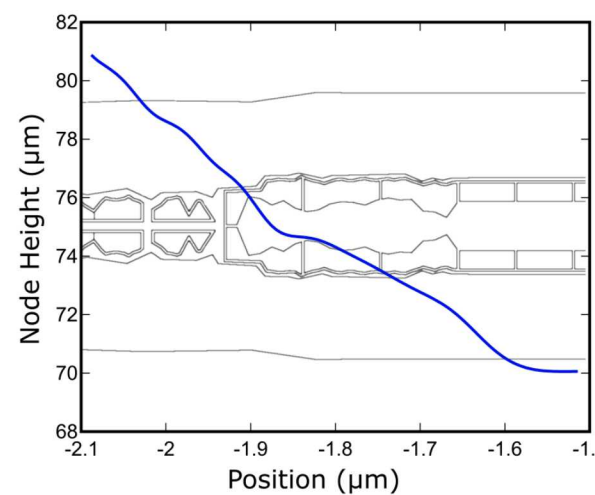
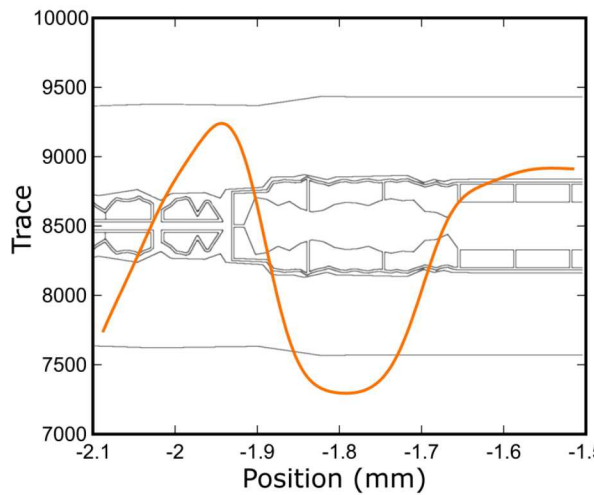
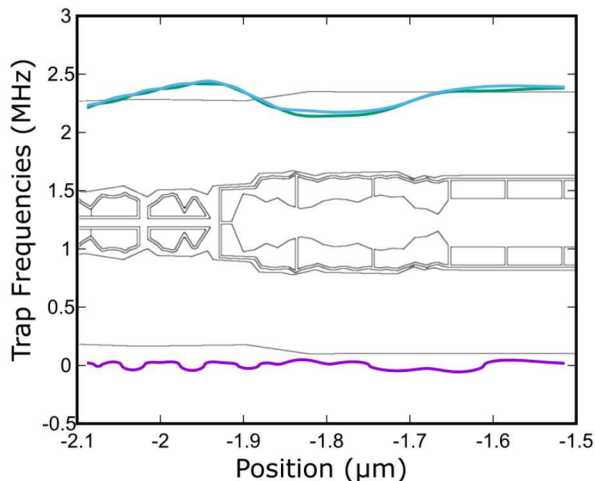
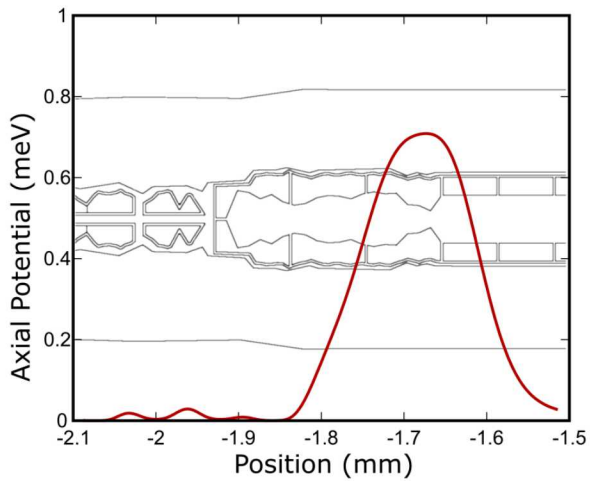


### Loading region

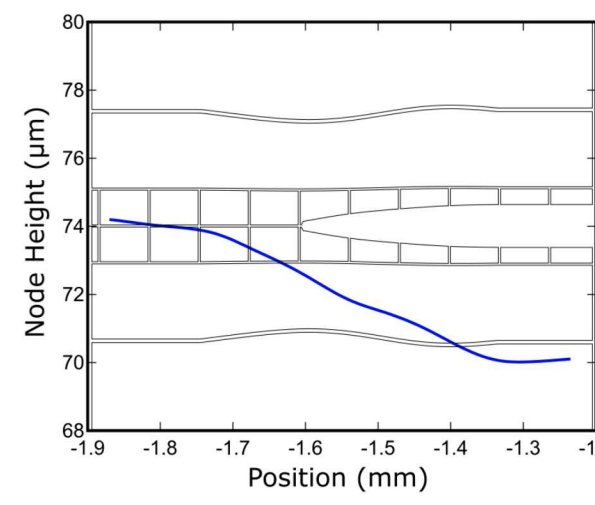
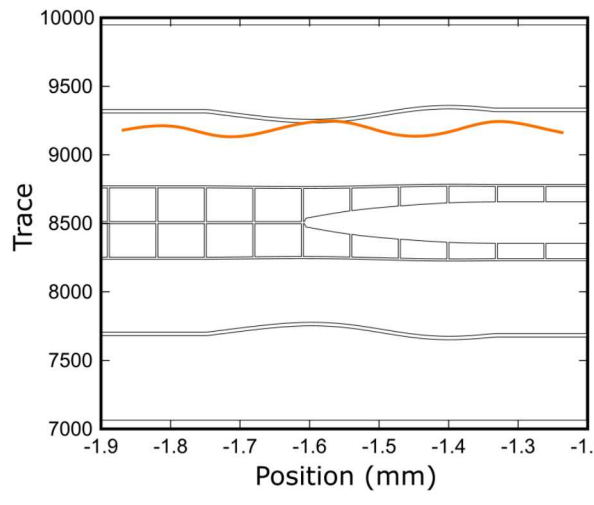
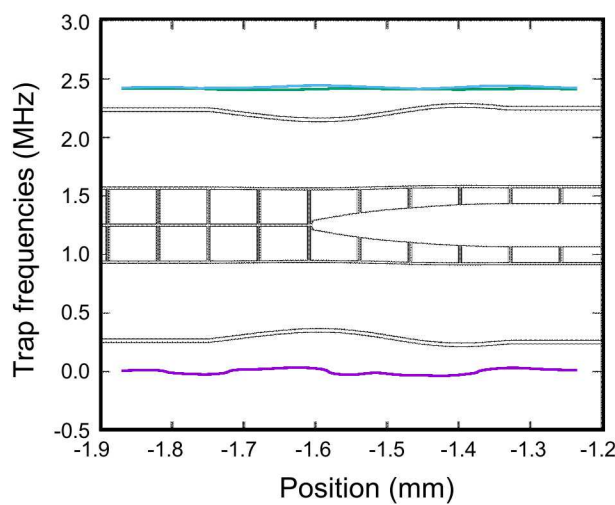
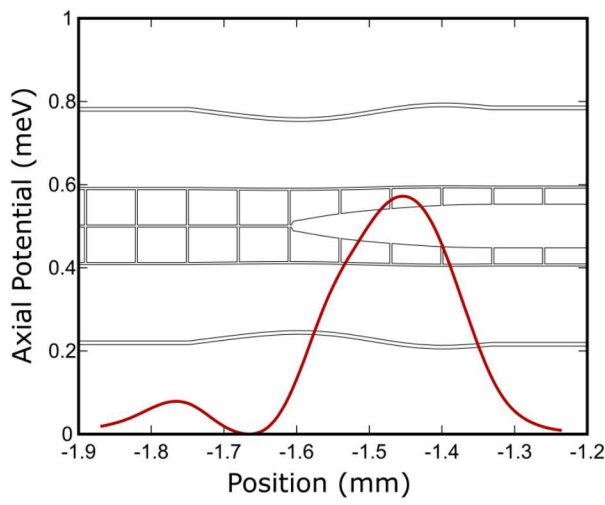
- 5 electrode pairs
- Loading slot  $150 \mu\text{m} \times 13 \mu\text{m}$

# 6 Design Improvements

## HOA - 2



## Phoenix trap



## Phoenix design

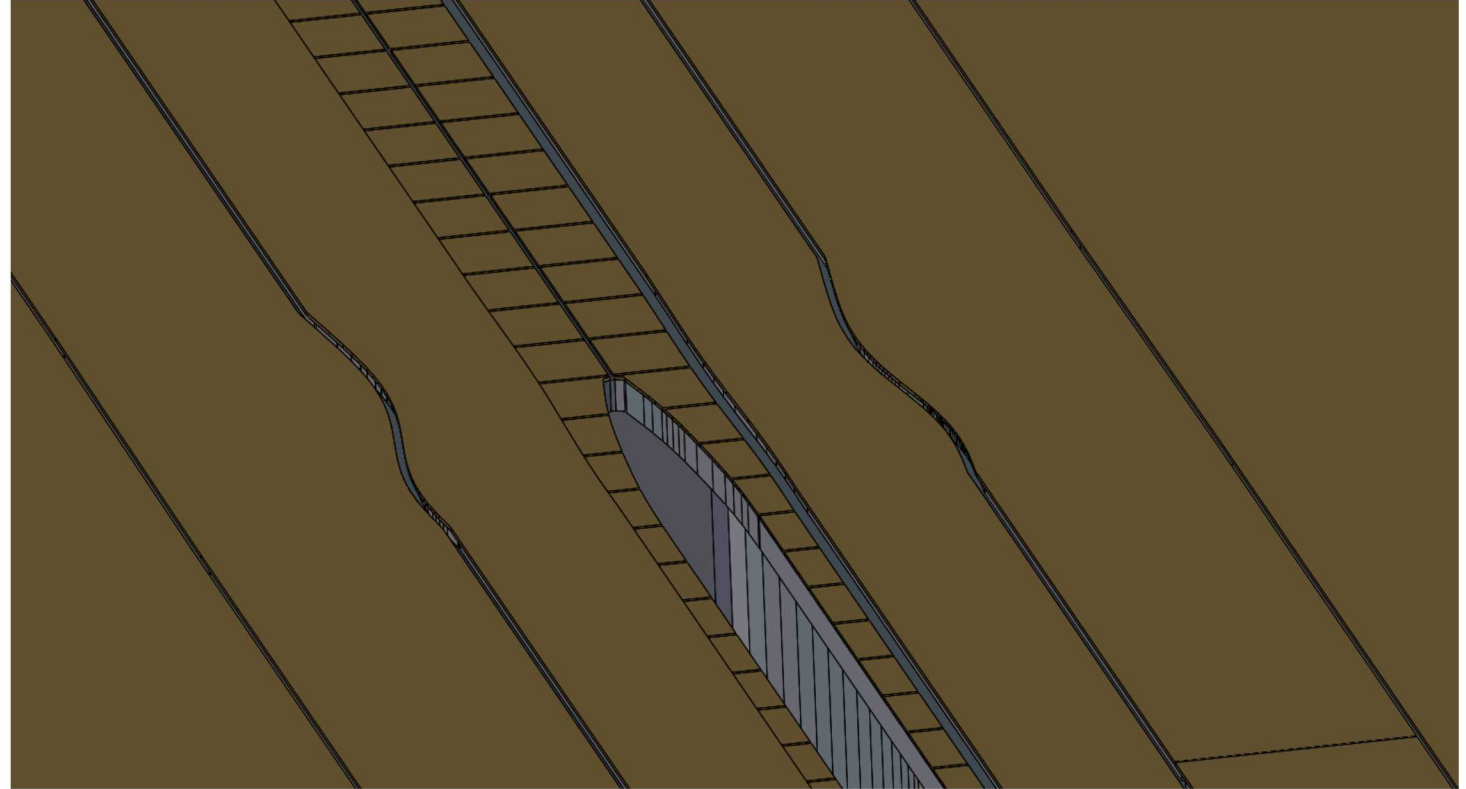
Objective was to refabricate Phoenix with low risk improvements to trap design

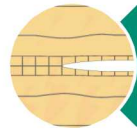
Phoenix changes:

- Use latest processes and design rules
- Modify design to reduce fabrication risk
- and resilient to fabrication errors

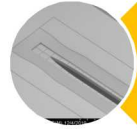
Trap changes:

- All inner control electrodes on lower metal layer
  - Smaller modulations on transition
  - Smaller potential barrier
  - Smaller variations on trace of curvature tensor

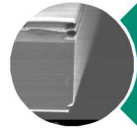




Phoenix trap design



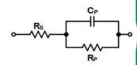
Phoenix trap fabrication and testing



Prompt-onset fields and ion heating



Phoenix package



Rf-dissipation



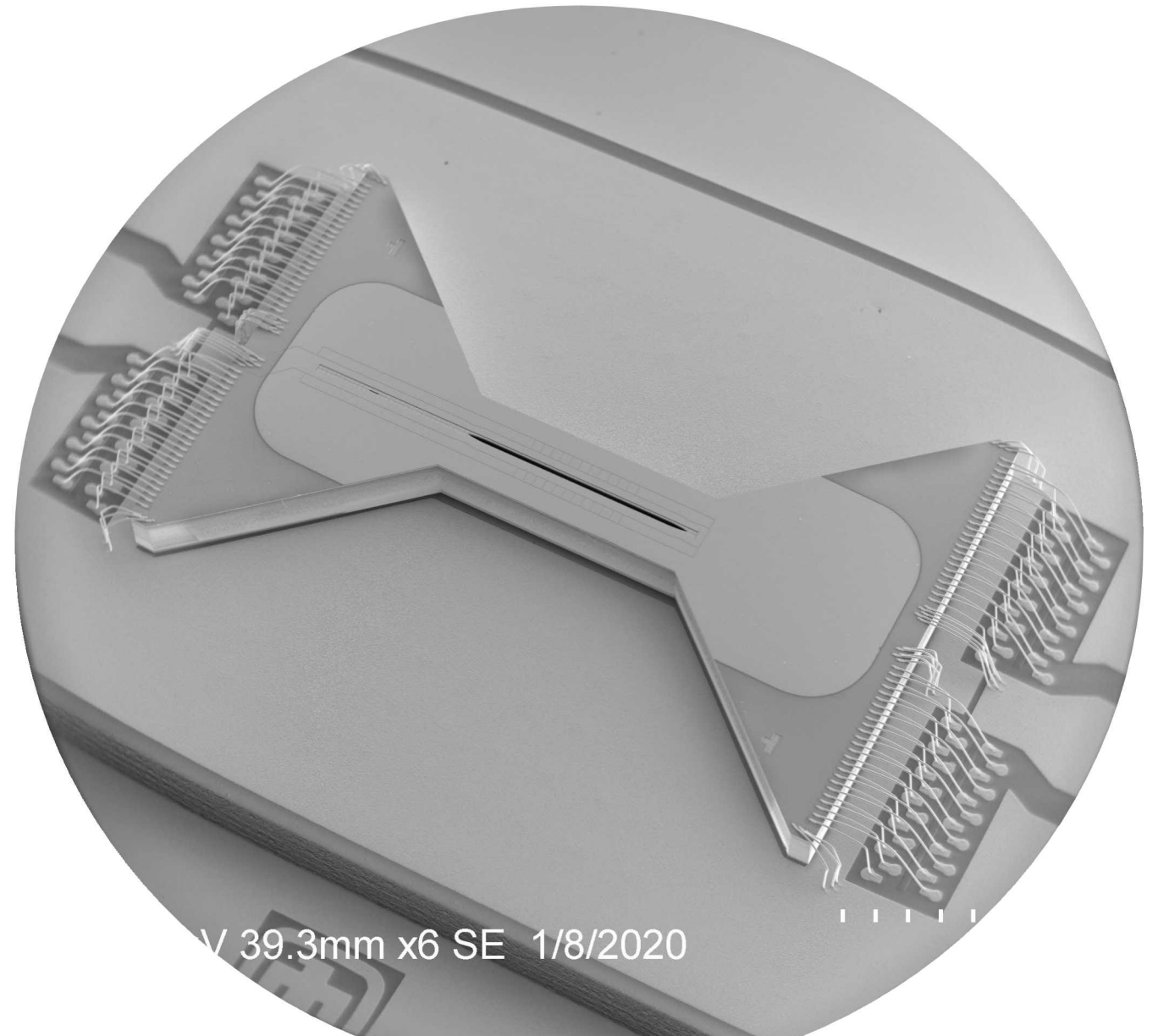
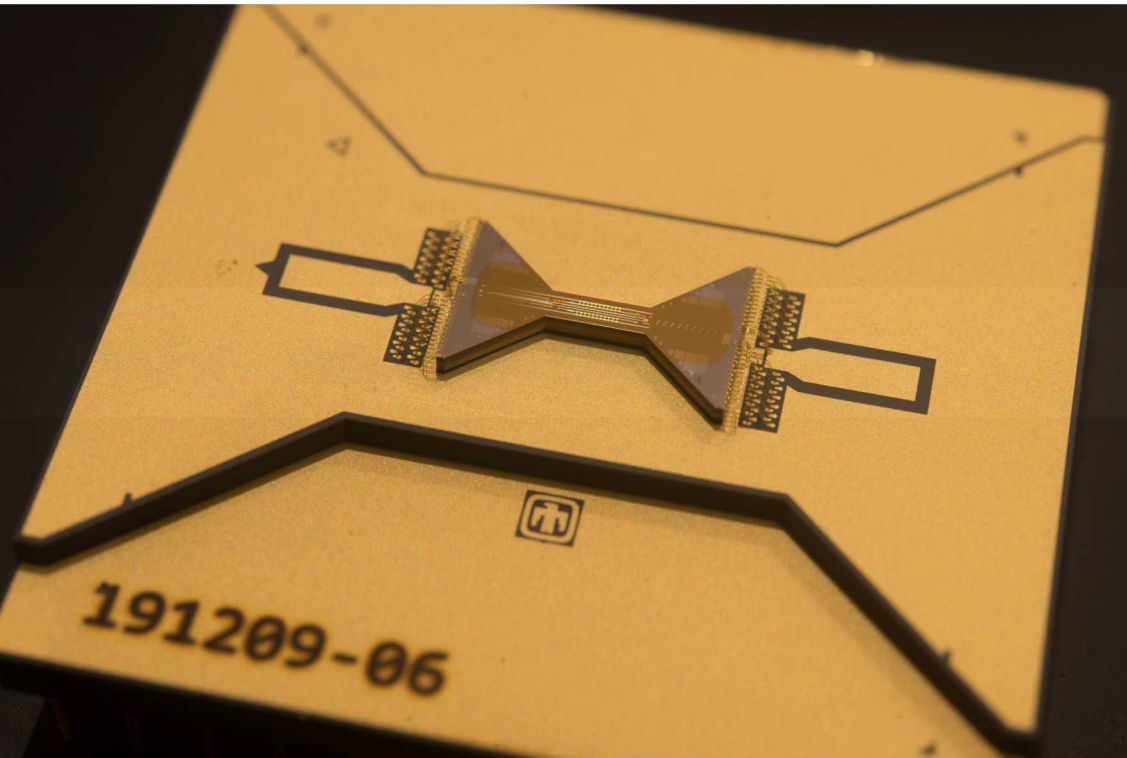
Peregrine trap



Quantum Scientific Open User Testbed (QSCOUT)

## 9 Phoenix trap fabrication

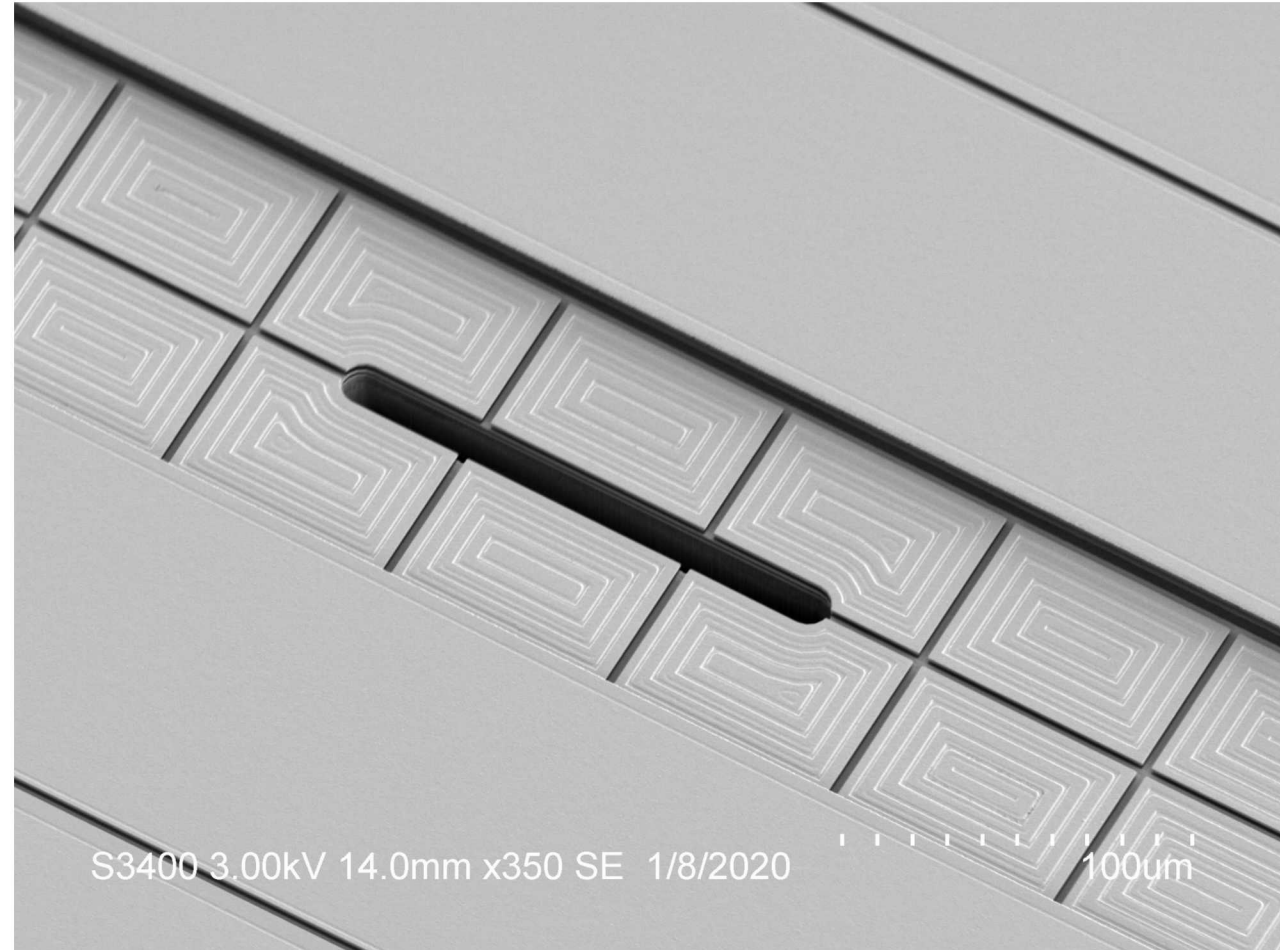
- Rendered with 6 metal layers
- Integrated trench capacitors
- RF electrode in M6
- Inner control electrodes in M3
- 450 steps



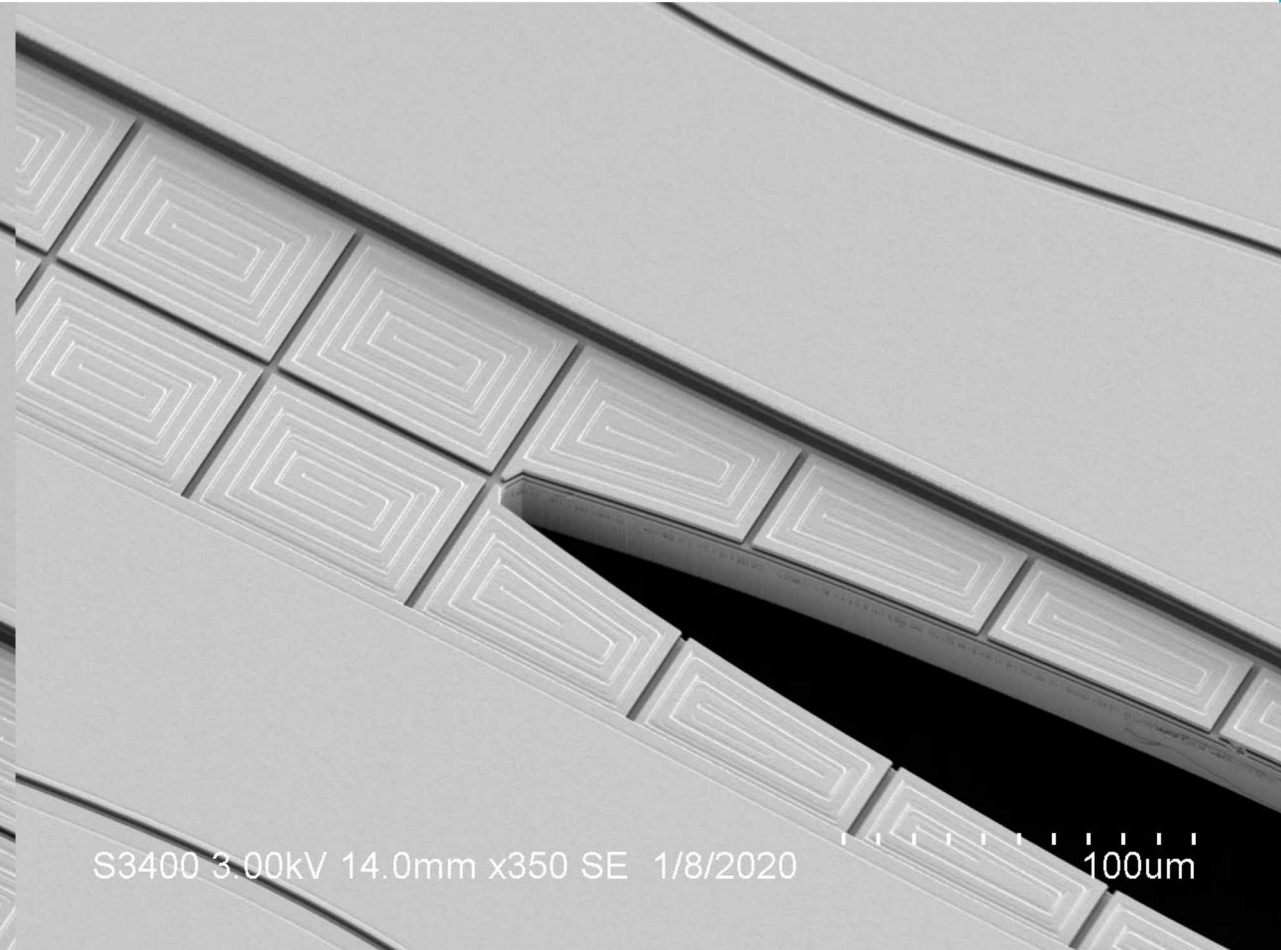
# Phoenix trap

All inner control electrodes are on a lower metal layer

Loading slot

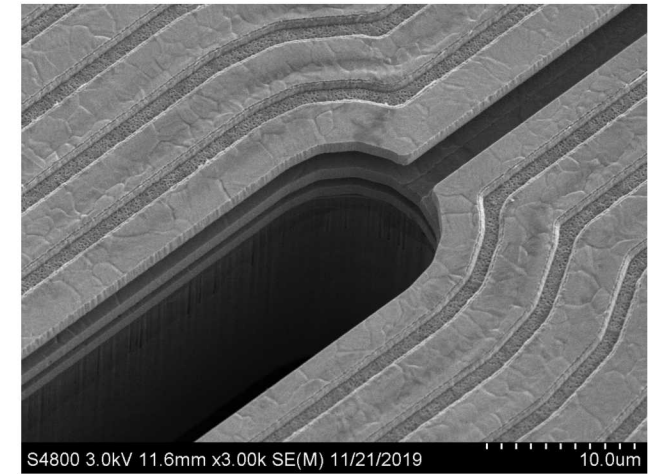


Transition between above-surface and slotted parts of trap

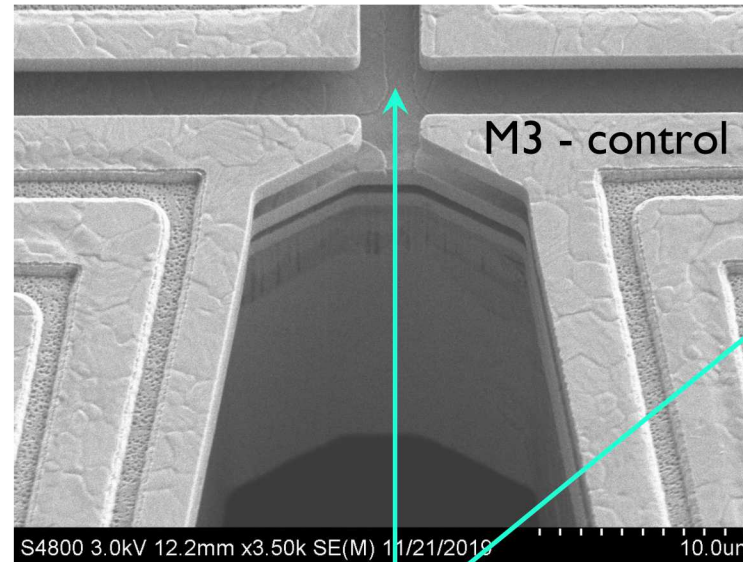
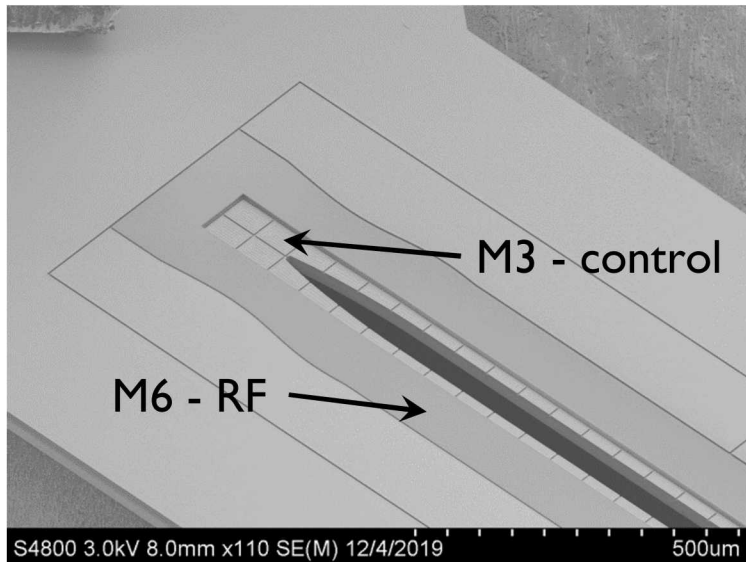


# 11 Device engineering the Phoenix trap

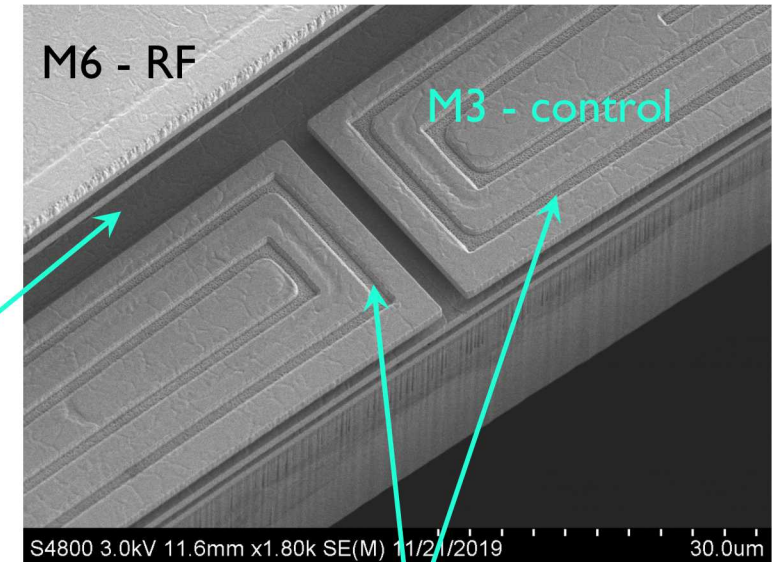
- Rendering of the 6-metal level Phoenix surface ion trap
  - RF electrode in M6
  - Control electrodes in M3
  - Device singulation was very well behaved



Loading hole



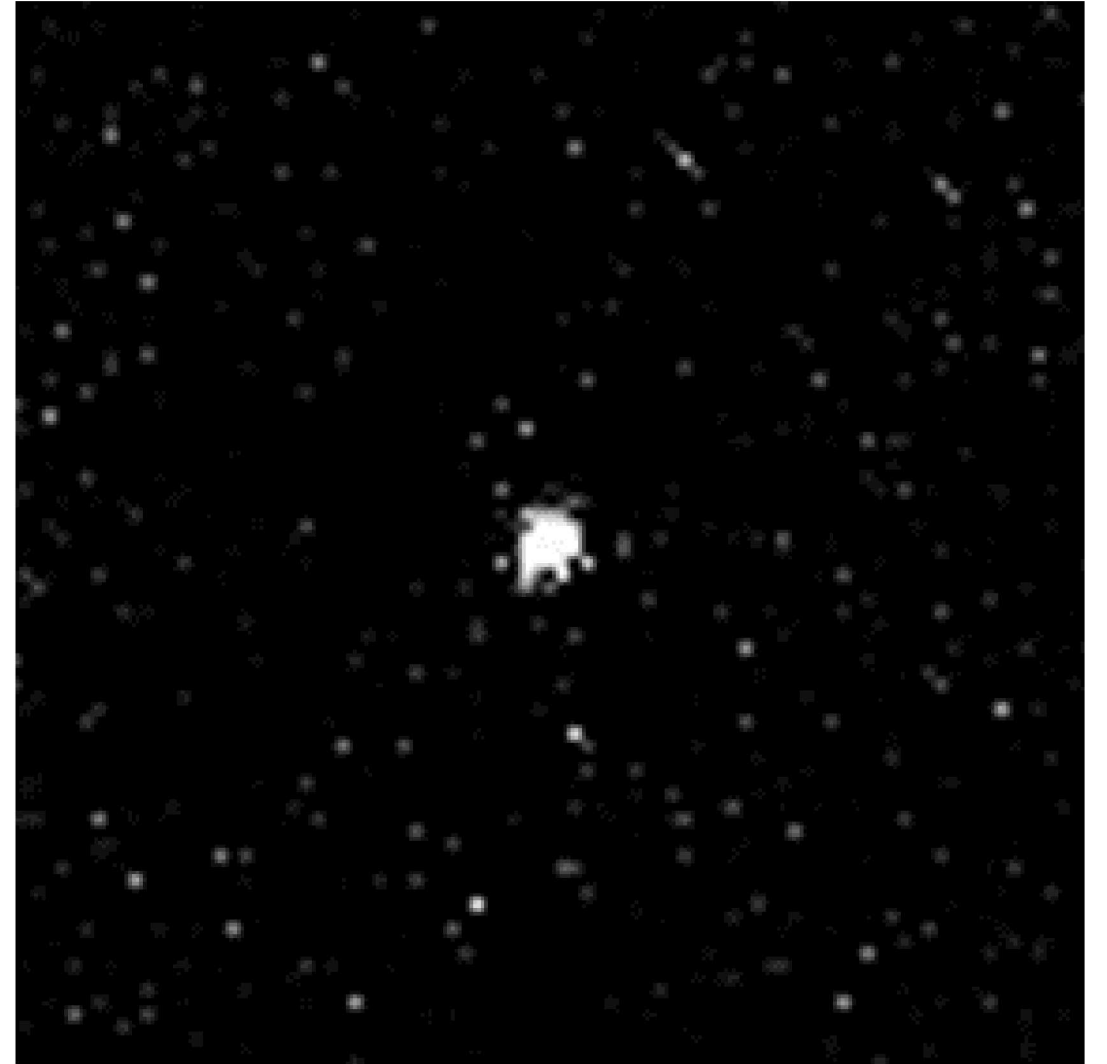
Clean removal of dielectric between electrodes

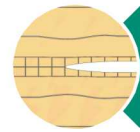


Imprint etch into control electrodes cosmetic; due to oxide over-etch  
Will be fixed in next wafer and in delivered traps

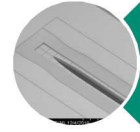
## Phoenix testing

- Trap mounted in chamber 1/3/2020
- Finished bake 1/8/2020
- Trapped first ions 1/10/2020
  
- First results are very encouraging
  - Trap without problems
  - Stable and small compensation fields
  - Trap frequencies narrow and as expected
  
- In-depth testing to resume when we return





Phoenix trap design



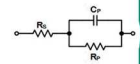
Phoenix trap fabrication and testing



Prompt-onset fields and ion heating



Phoenix package



Rf-dissipation



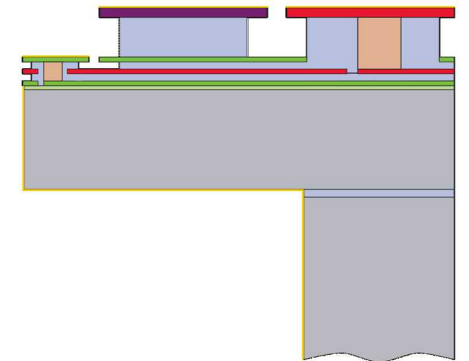
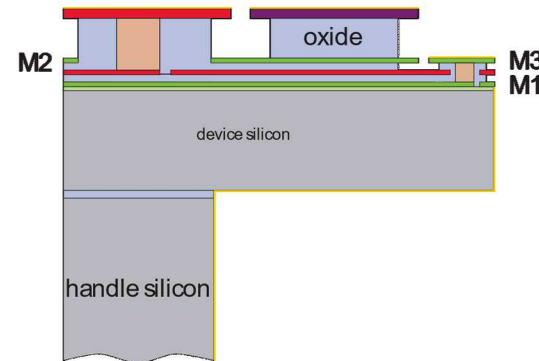
Peregrine trap



Quantum Scientific Open User Testbed (QSCOUT)

## Prompt-onset electric fields

- Exposed Silicon in the slot of the trap
- If light reaches this area, electric fields can change on timescales of oscillation periods
- This can result in prompt response and heating
- Covering the sidewall with continuous metal film should solve this problem
- Evaporating gold on this surface reduced effect by several orders of magnitude



## Ion heating in HOA-2 traps

- HOA-2 room temperature (Sandia)
  - 80q/s @ 2.6MHz, Ytterbium
- HOA-2.1 Cryogenic (Duke)
  - 70q/s @ 2.6MHz, Ytterbium
- HOA-2.1 Cryogenic (Innsbruck/Zürich)
  - 1,000 – 60,000q/s ? @ 2 – 3 MHz ?, Calcium

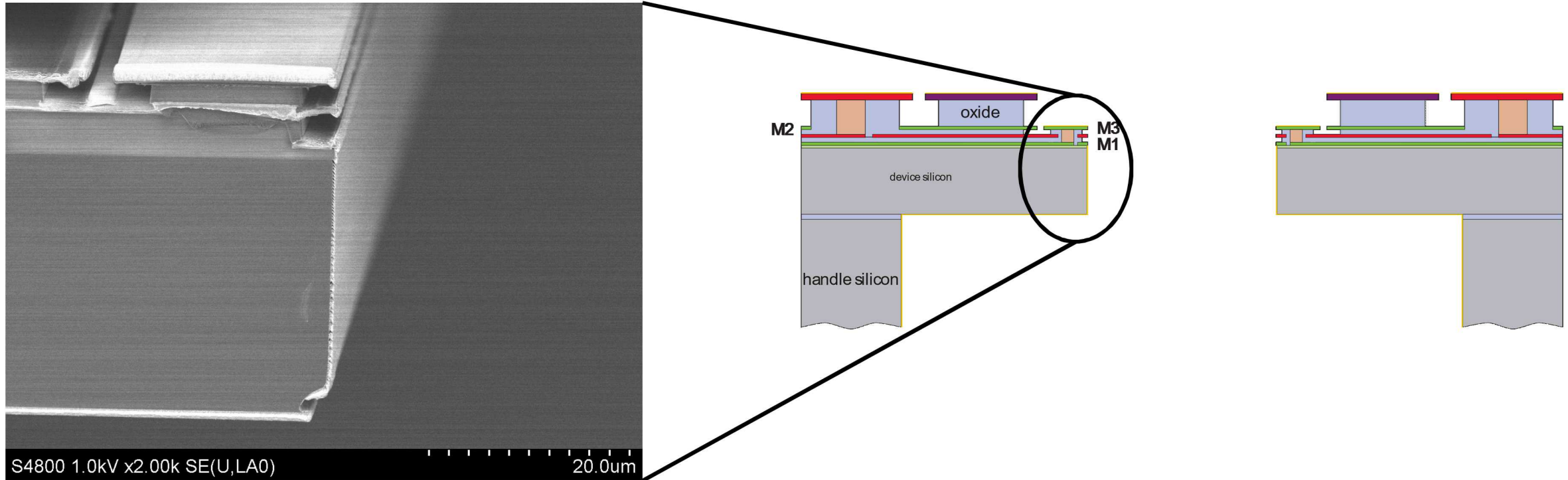
### Conjectures:

- Heating rates in HOA-2.1 trap do *not* drop as trap is cooled to cryogenic temperatures
- Beams through slots might lead to heating due to prompt-onset charging

Heating rates at cryogenic temperature might be due to material properties  
Currently being investigated.

Metallization of slot sidewalls might be crucial for achieving low heating rates

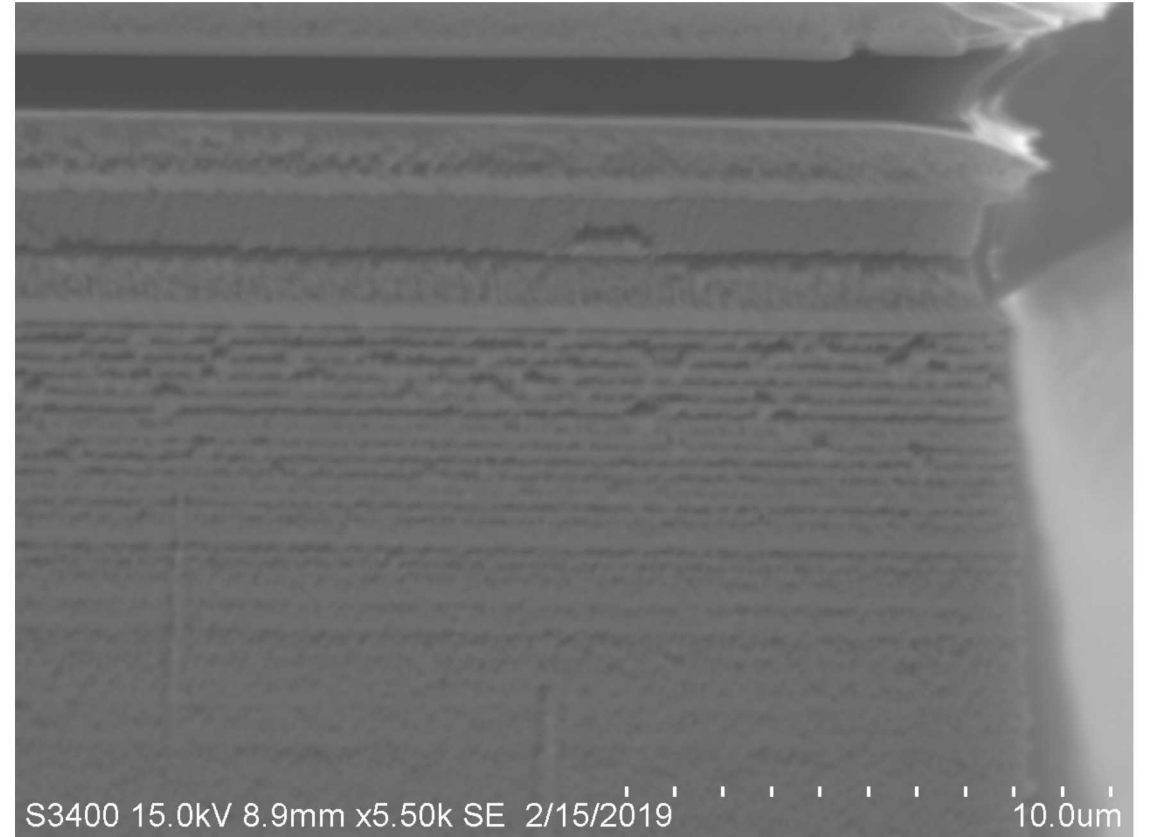
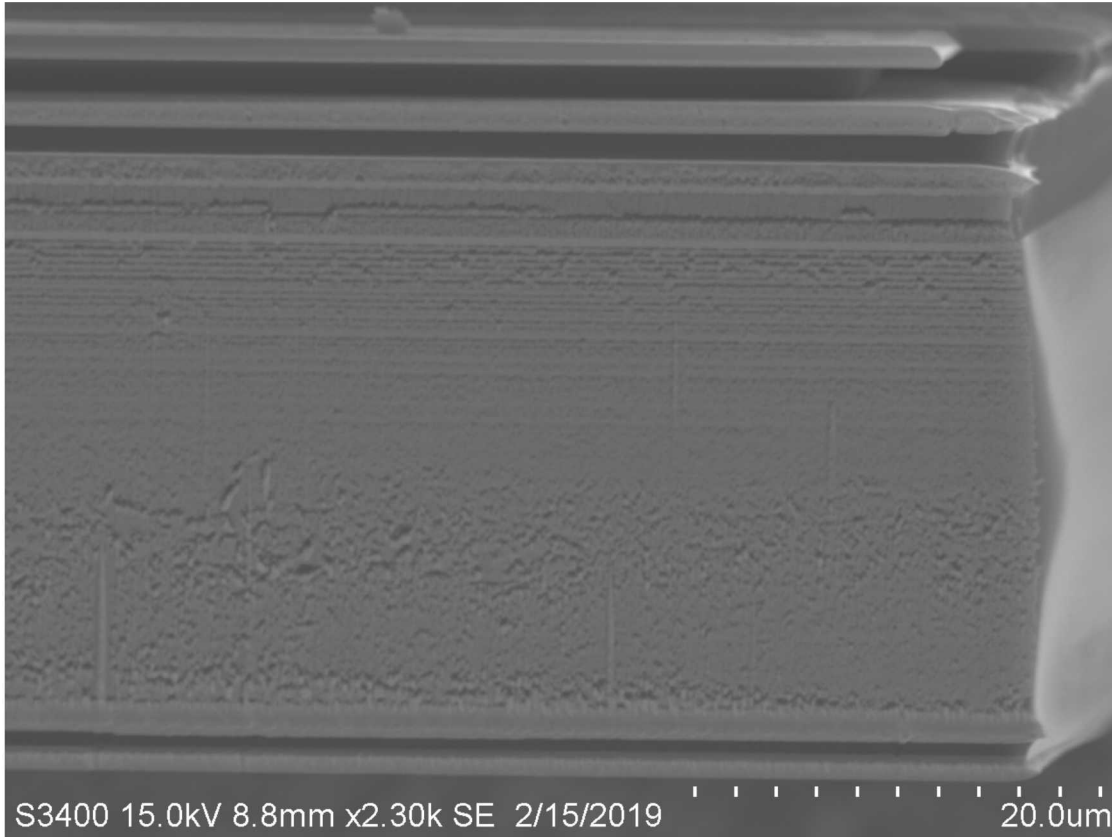
# HOA-2 trap characterization



- Increased evaporated gold layer thickness on backside ten times
- Adjusted evaporation angle to optimize for sidewall coverage
- SEM shows gold layer on sidewall >100nm
- Fast-onset charging is strongly suppressed, still to be improved
- However, Innsbruck team, cryogenic operation, still observe charging

## Second look at sidewall coverage

Deep reactive-ion etching (DRIE) leads to undulated sidewalls

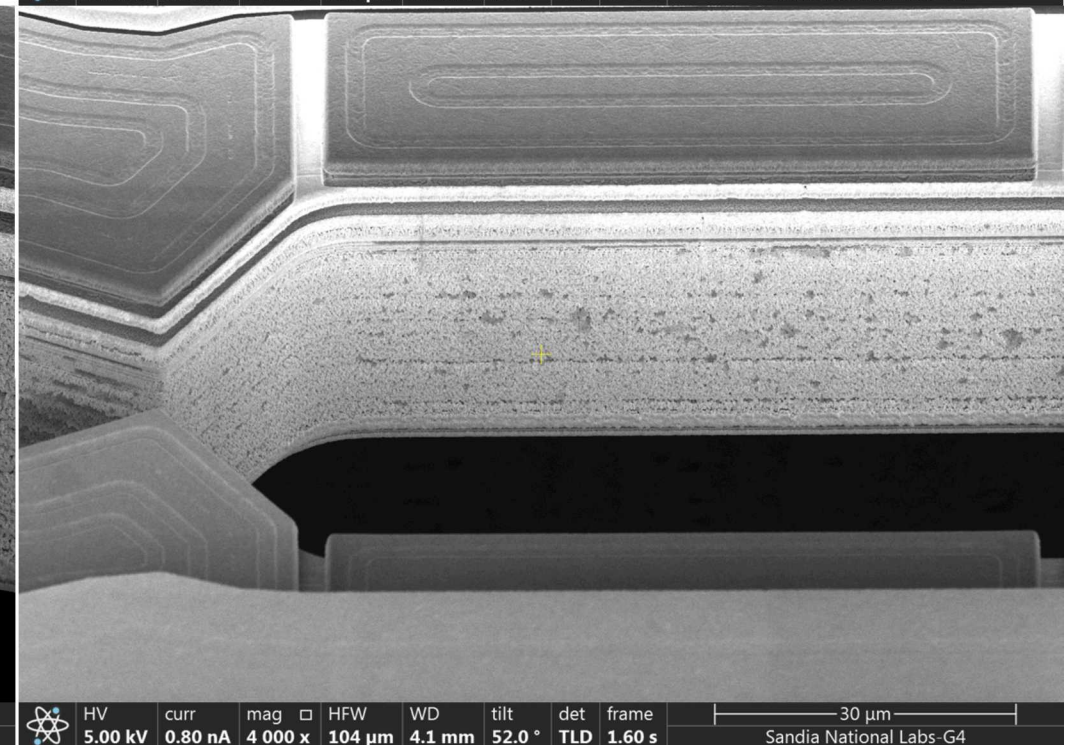
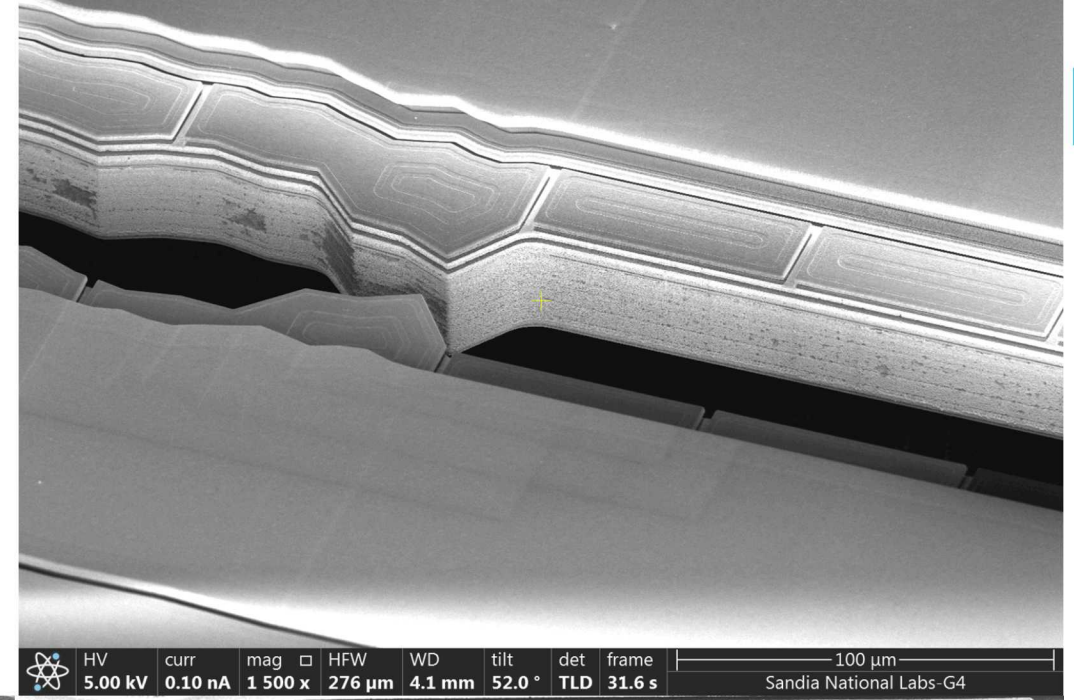
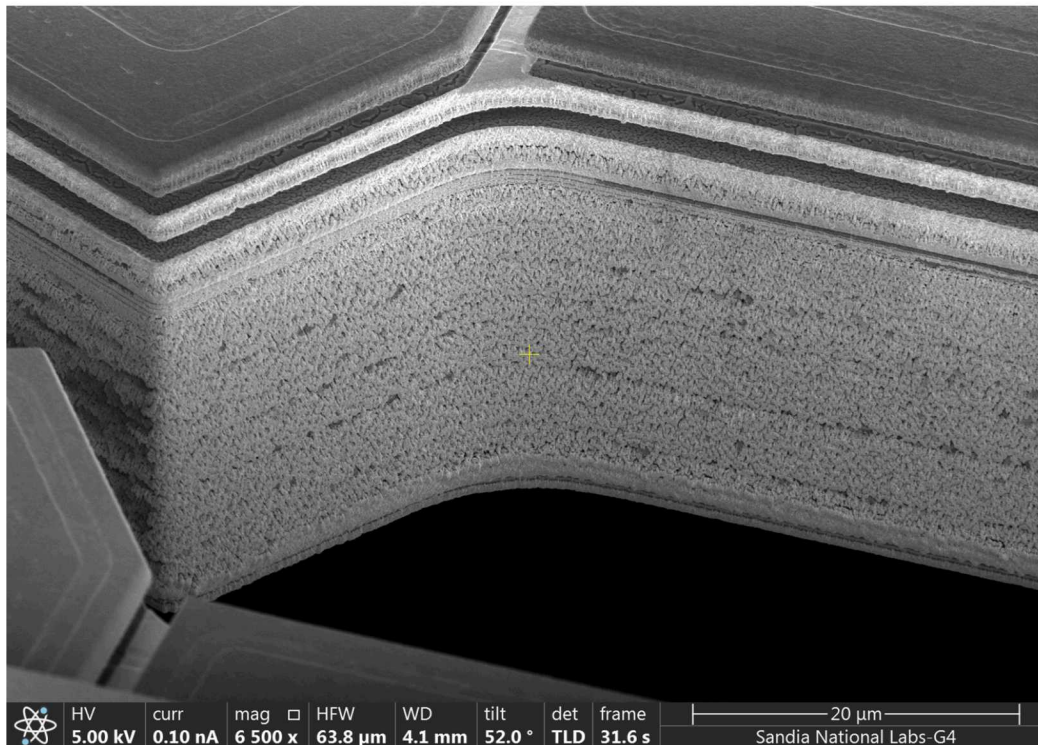


There might be exposed silicon that is susceptible to charging

## HOA-2.1 trap characterization

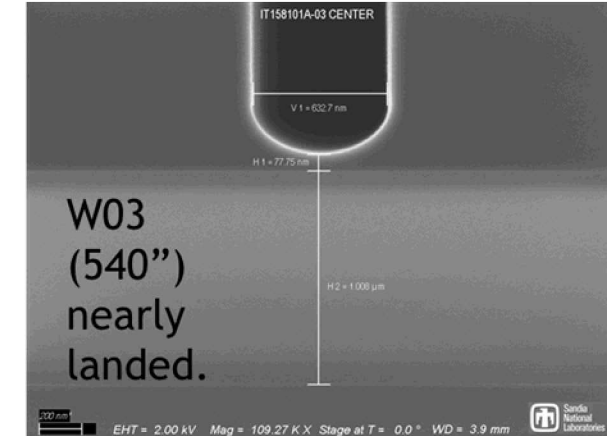
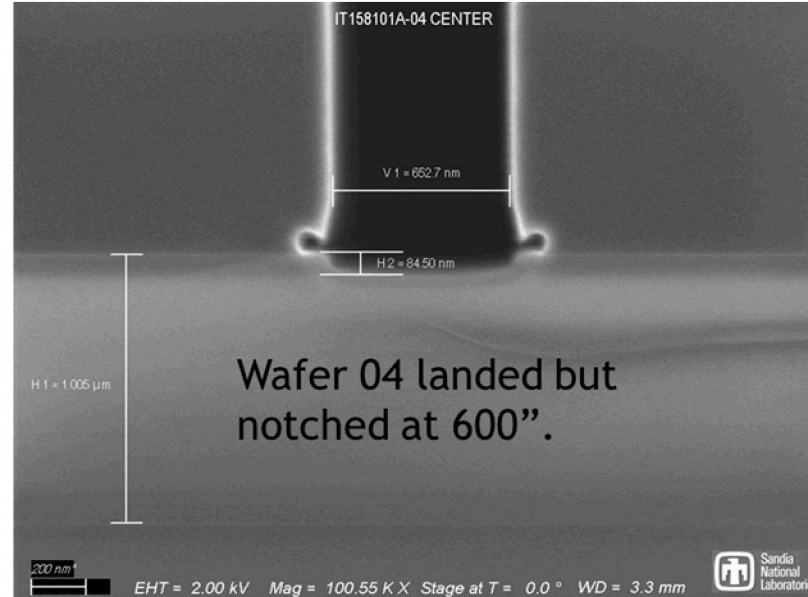
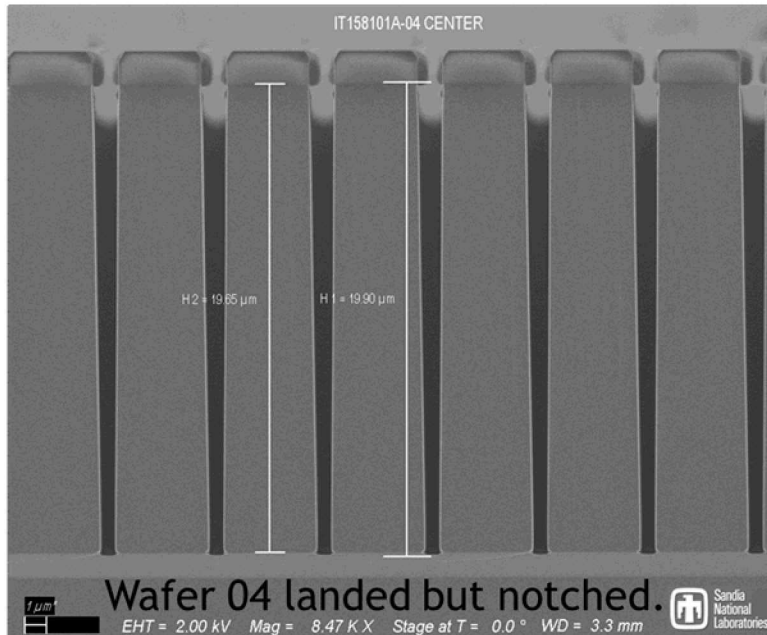
Slot sidewall analysis of Bosch etched slot feature in HOA 2.1 – Innsbruck

- Ti/Pt/Au coverage:  $15^\circ$
- SEM images imply incomplete Au coverage



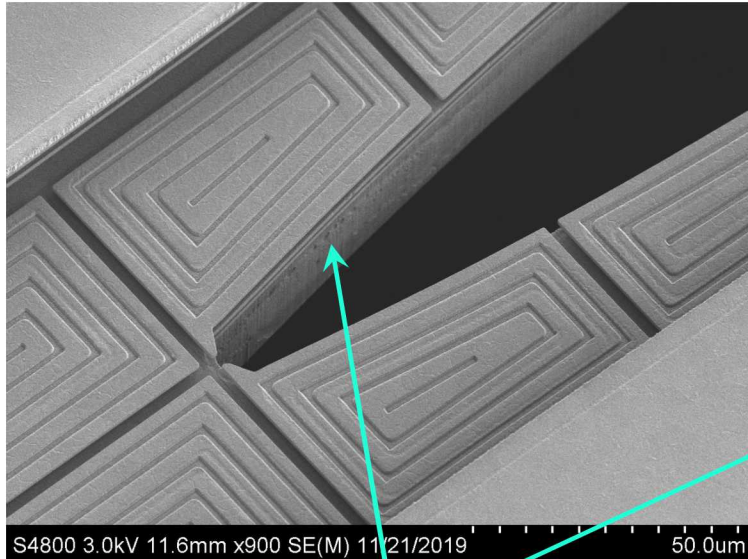
## Re-engineered sidewall on Phoenix traps

- Using etch used for trench capacitors for definition of slot
- Smooth sidewalls
- Slightly angled ( $<1^\circ$ )
- Expect continuous sidewall coverage from evaporation
- Will use short-loop to verify before devices are complete

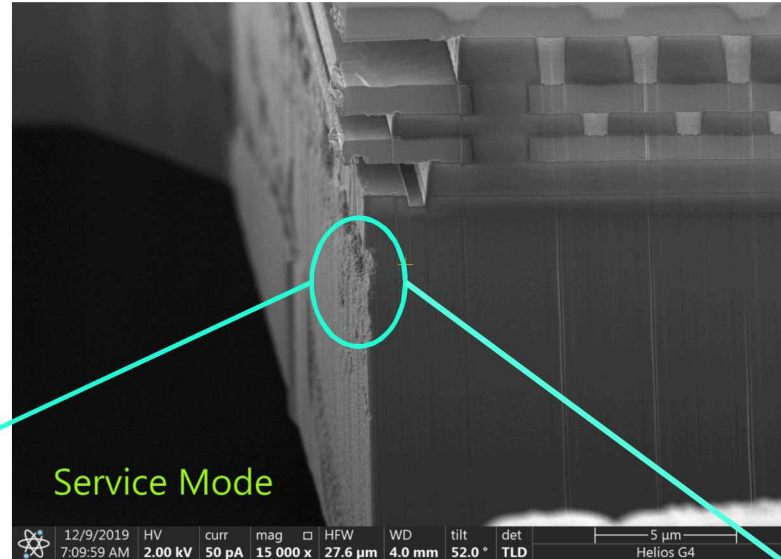


# Re-engineering the slot sidewall for Phoenix traps

- Define slot using the mixed-gas etch employed for trench capacitors
  - Replaces Bosch dep-etch process
  - Mixed-gas etch process gives smoother, but not perfect, sidewalls
  - Slight positive angle ( $<1^\circ$ )
  - Goal: continuous metal sidewall coverage upon metal evaporation

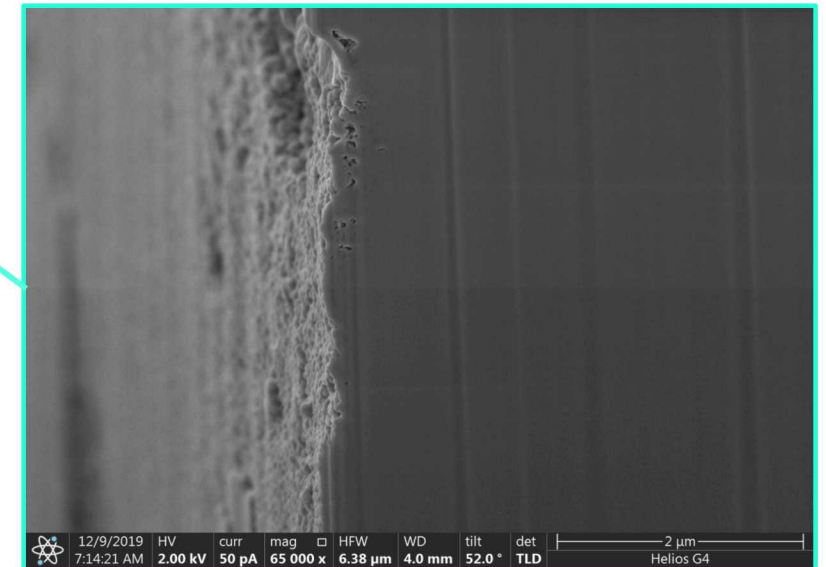
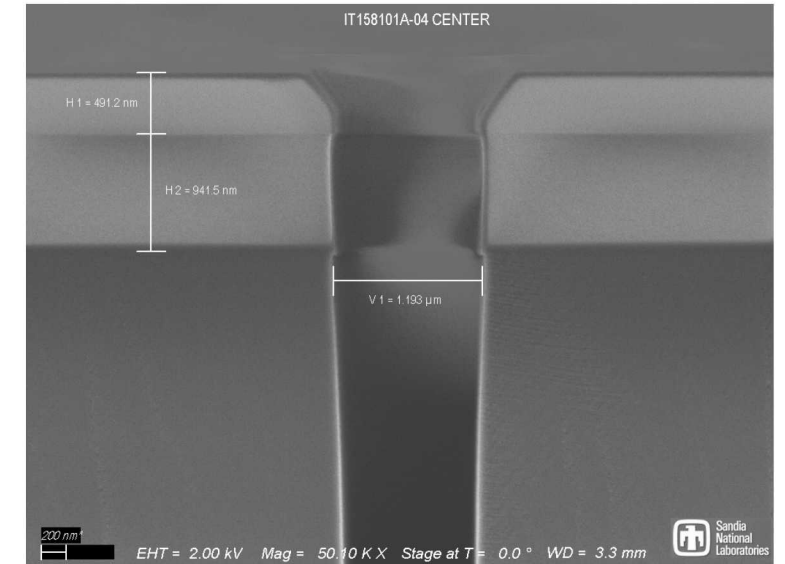


Surface roughness in top-Si sidewall of slot



Surface roughness occurs after definition of the slot

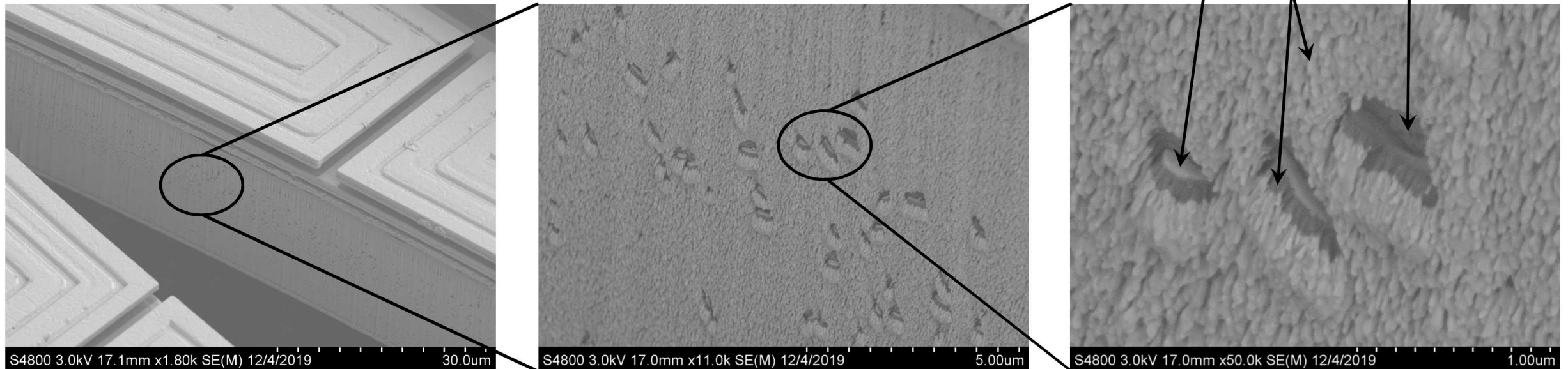
As etched sidewall



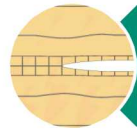
# Re-engineering the slot sidewall for Phoenix traps

## Au coating of electrodes and slot sidewall

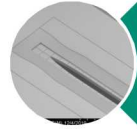
- Device backside/sidewall coating
  - 200/200/500 (nm) Ti/Pt/Au
  - 15° (fixed) angle evaporation
- Frontside electrode coating
  - 20/20/50 (nm) Ti/Pt/Au
  - Normal incidence (0°) evaporation
- Imperfect coverage → Si probably still exposed
- Front and backside variable angle deposition experiments in progress



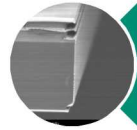
- Suggests Stranski-Krastanow (SK) growth = layer-by-layer + island growth



Phoenix trap design



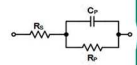
Phoenix trap fabrication and testing



Prompt-onset fields and ion heating



Phoenix package



Rf-dissipation



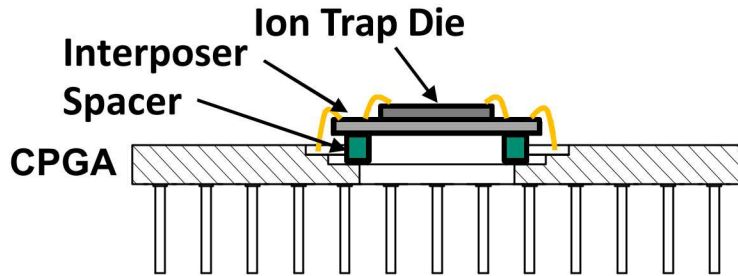
Peregrine trap



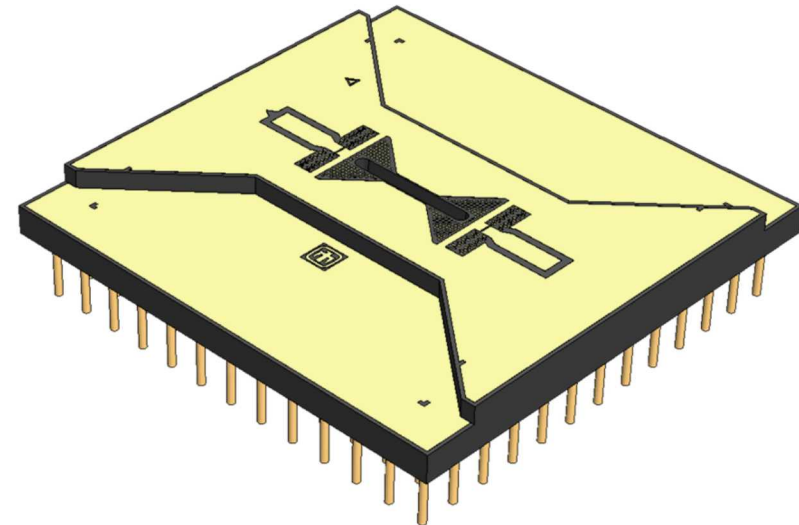
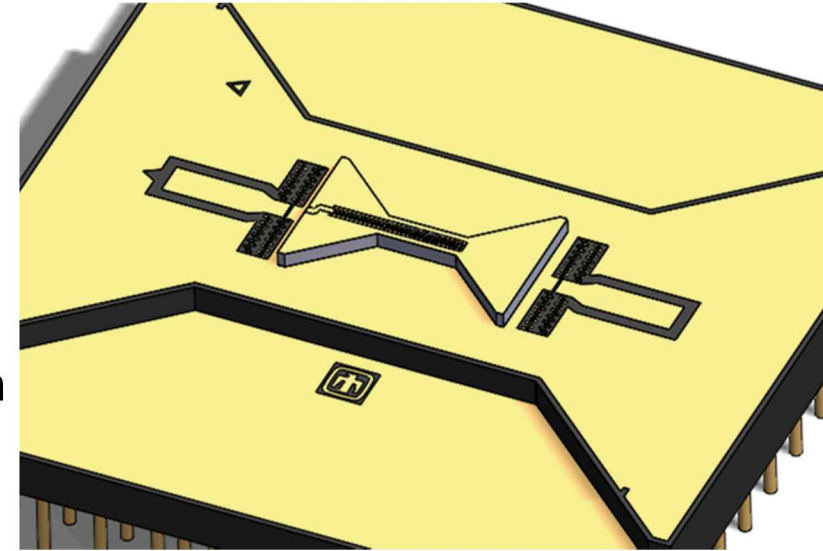
Quantum Scientific Open User Testbed (QSCOUT)

# Custom trap package

## Legacy 4 Level CPGA Packaging Assembly



## Simplified 2 part assembly



### Objectives:

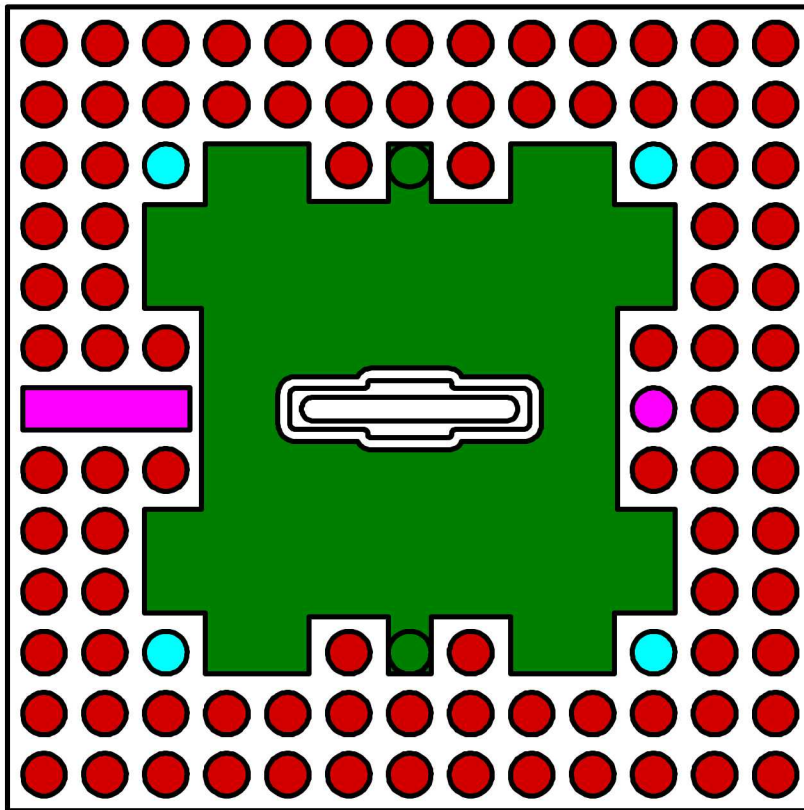
- Improved rf- and ground performance, reduced rf dissipation
- Compatible with bowtie chip without interposer
- Simplified assembly
- Backwards compatibility with MQCO package

### Properties:

- AlN for improved thermal conductivity and reduced thermal expansion vs  $\text{Al}_2\text{O}_3$
- Two rf connections with minimized capacitance (3pF) and resistivity (50mOhm)
- Backwards compatible with prior HOA devices
- Metal coverage of top surface
- All metal is signal or ground (no floating metals)

## Package signals

- Accommodations to be able to route rf on outside of package
- 2 ground pins in PGA
- Up to 18 ground connections in LGA



- 94 DC control signals
- 4 connections for resistive wires
- rf feed
- rf monitor
- ground

## Trap packaging

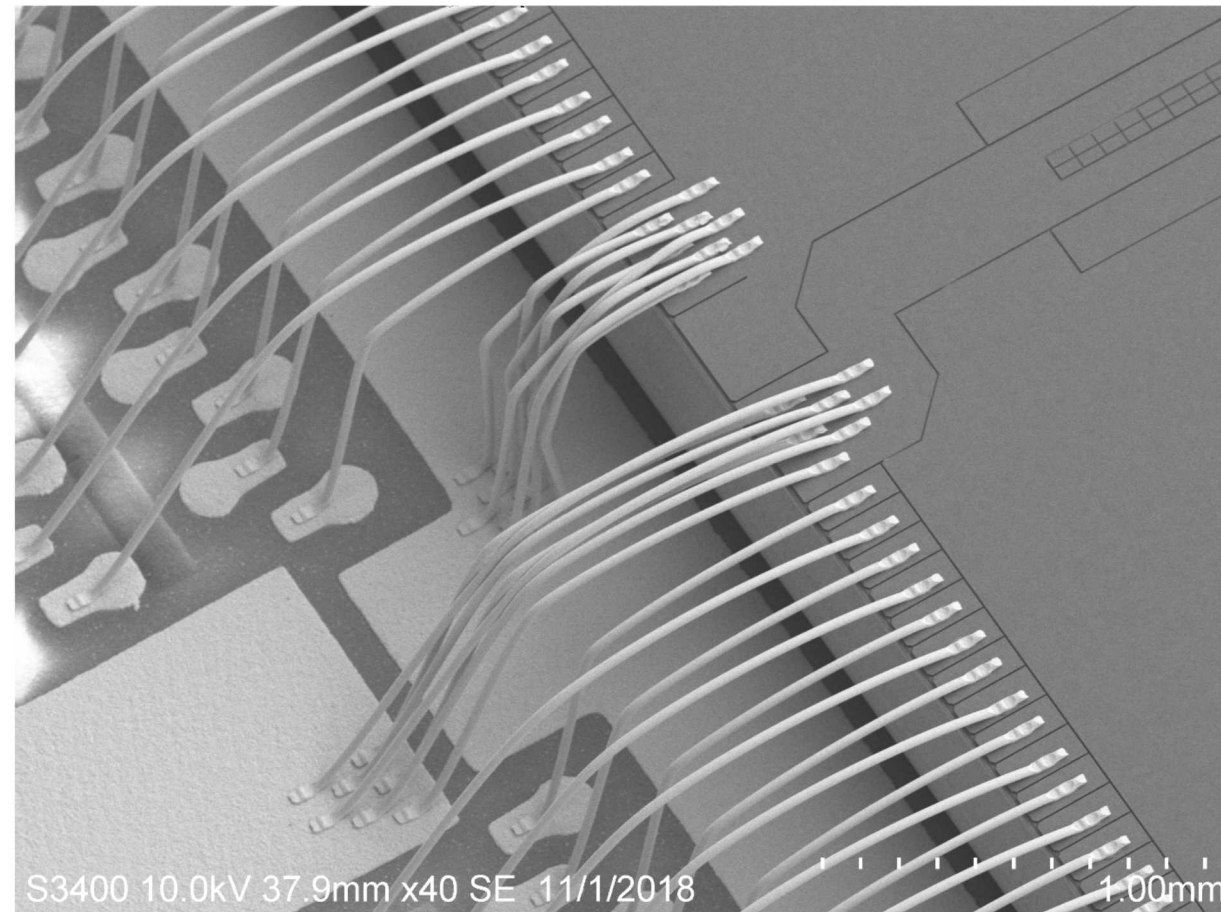
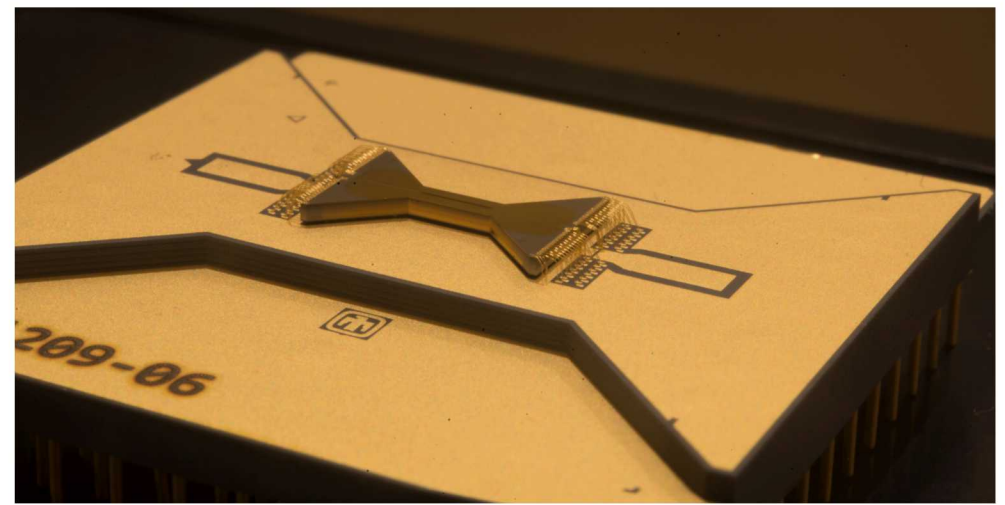
- Packaging enables parametric testing
- Packaging enables transport and mounting of traps in vacuum chambers

### Objectives of new custom package:

- Improved rf- and ground performance
- Compatible with bowtie chip without interposer
- Simplified assembly
- Backwards compatibility with MQCO package
- Organics-free solder die attach process

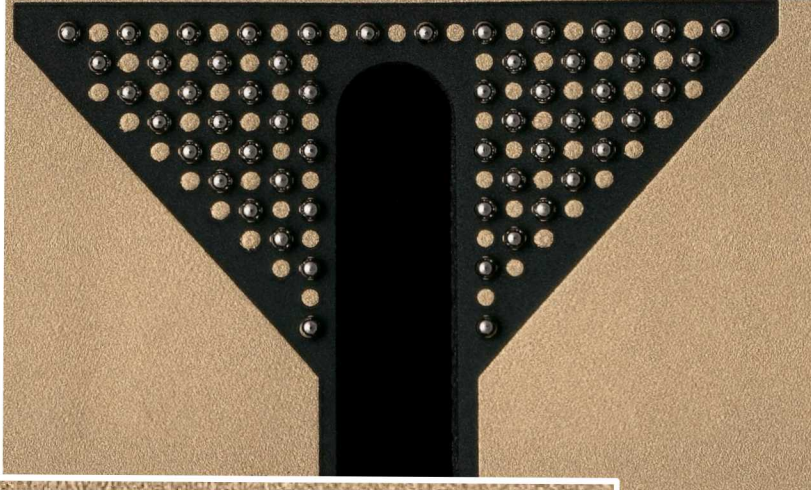
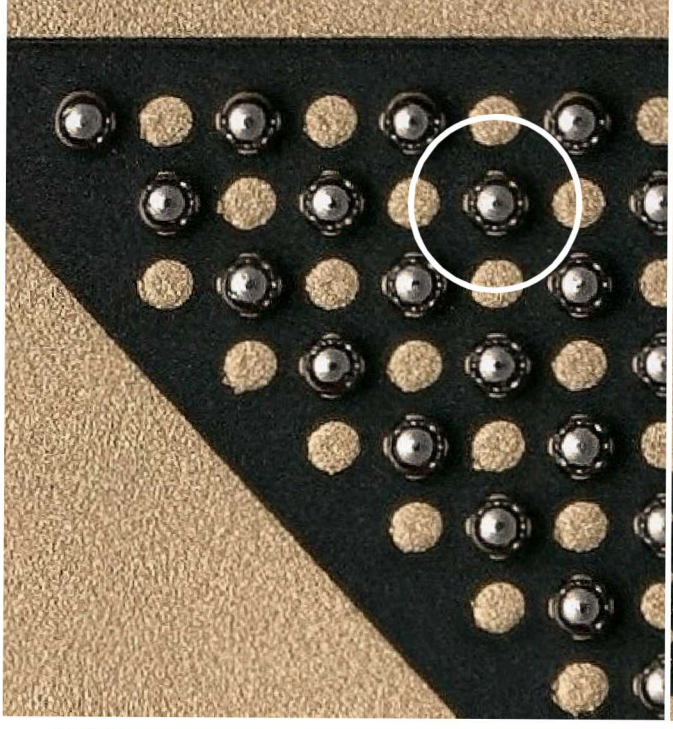
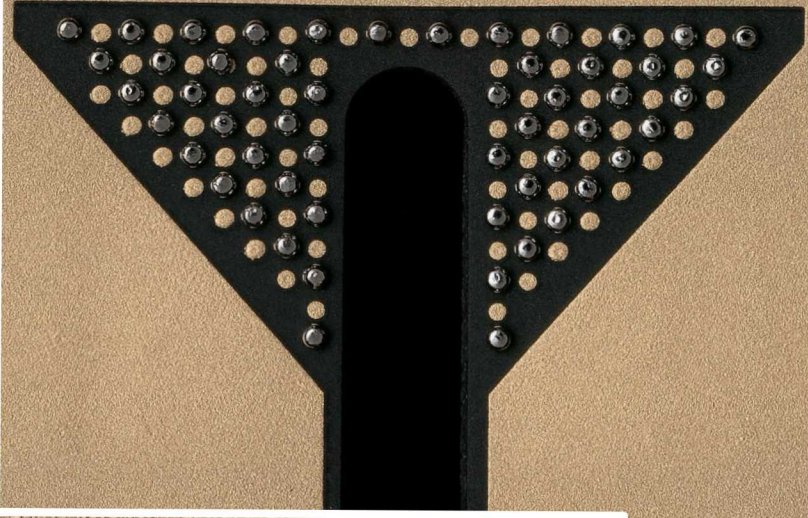
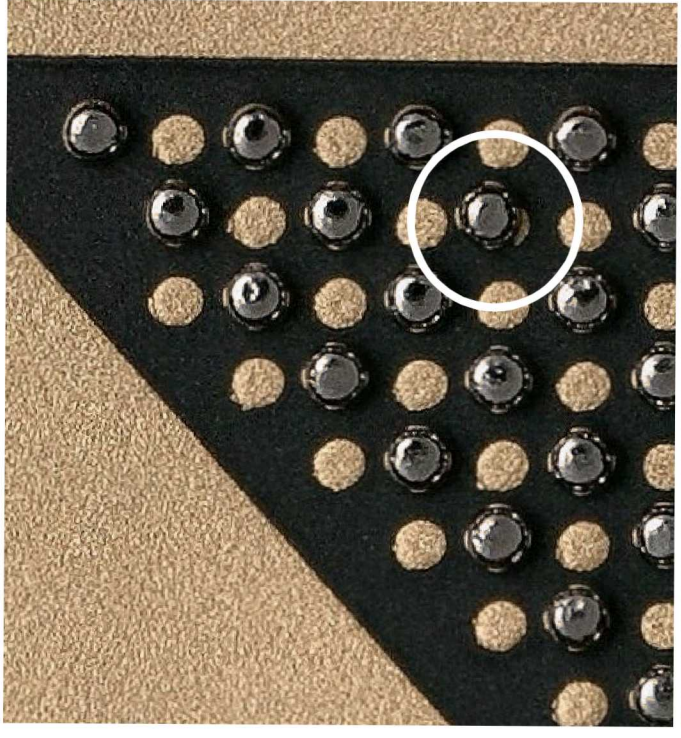
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- Backwards compatible with prior HOA devices
- Metal coverage of top surface
- All metal is signal or ground (no floating metals)



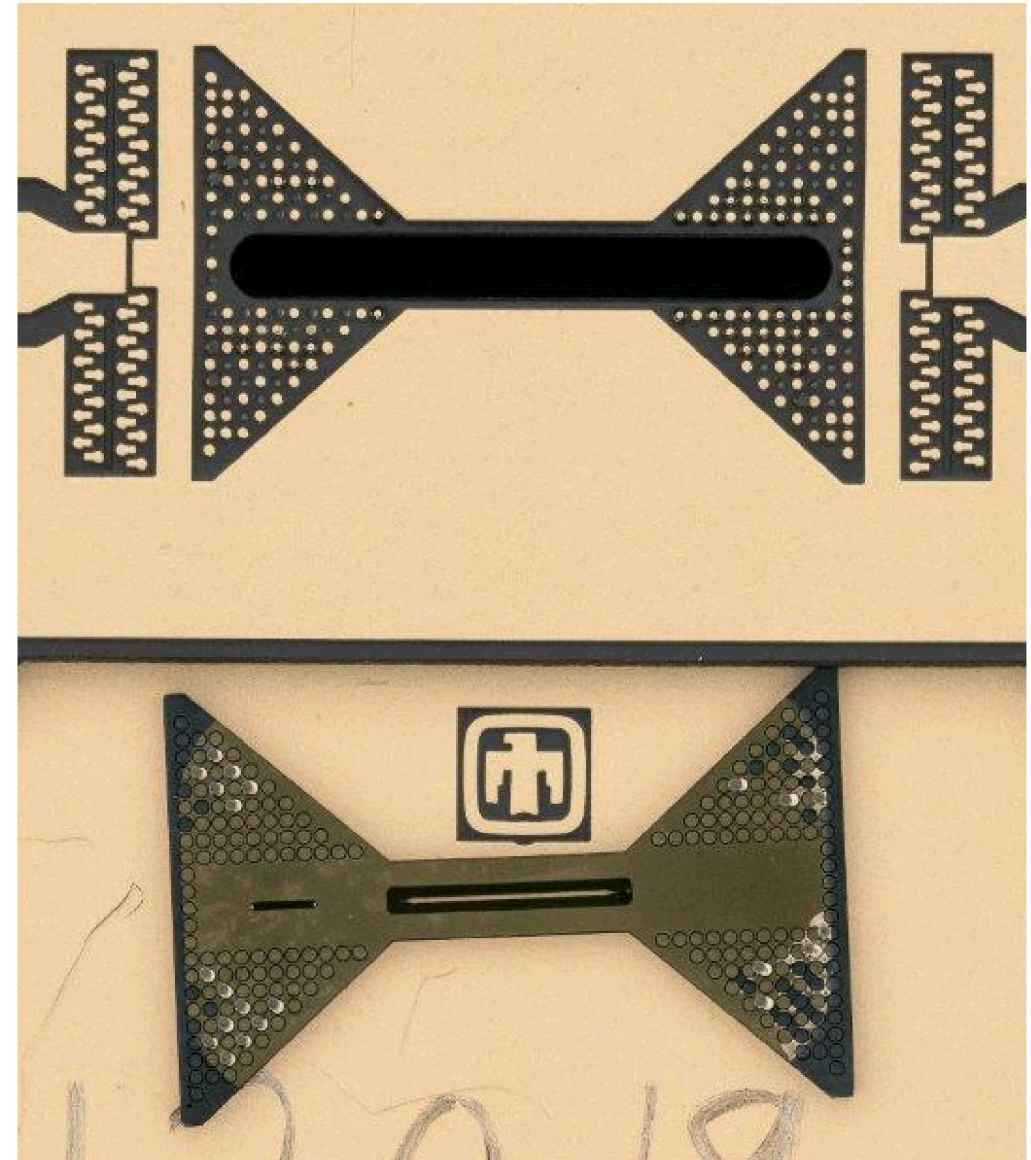
## Phoenix assembly using solder die attach

- Removes all organics from trap assembly
- Solder spheres laser solder “jetted” onto package surface
- Spheres auto-center on pads after reflow process
- To be done: shear testing, LN2 dunk and shear tests
- Smaller solder spheres and populate every pad

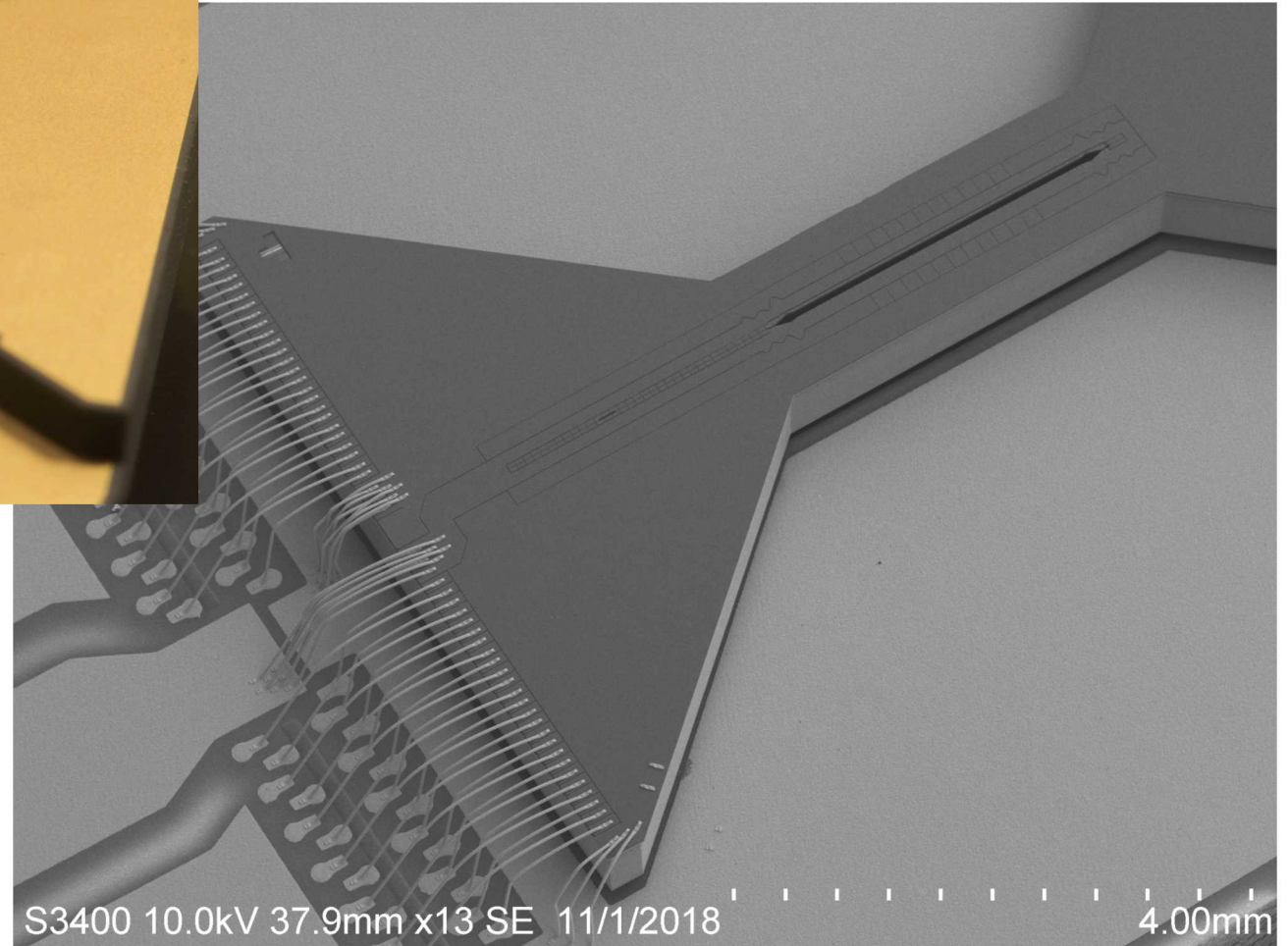
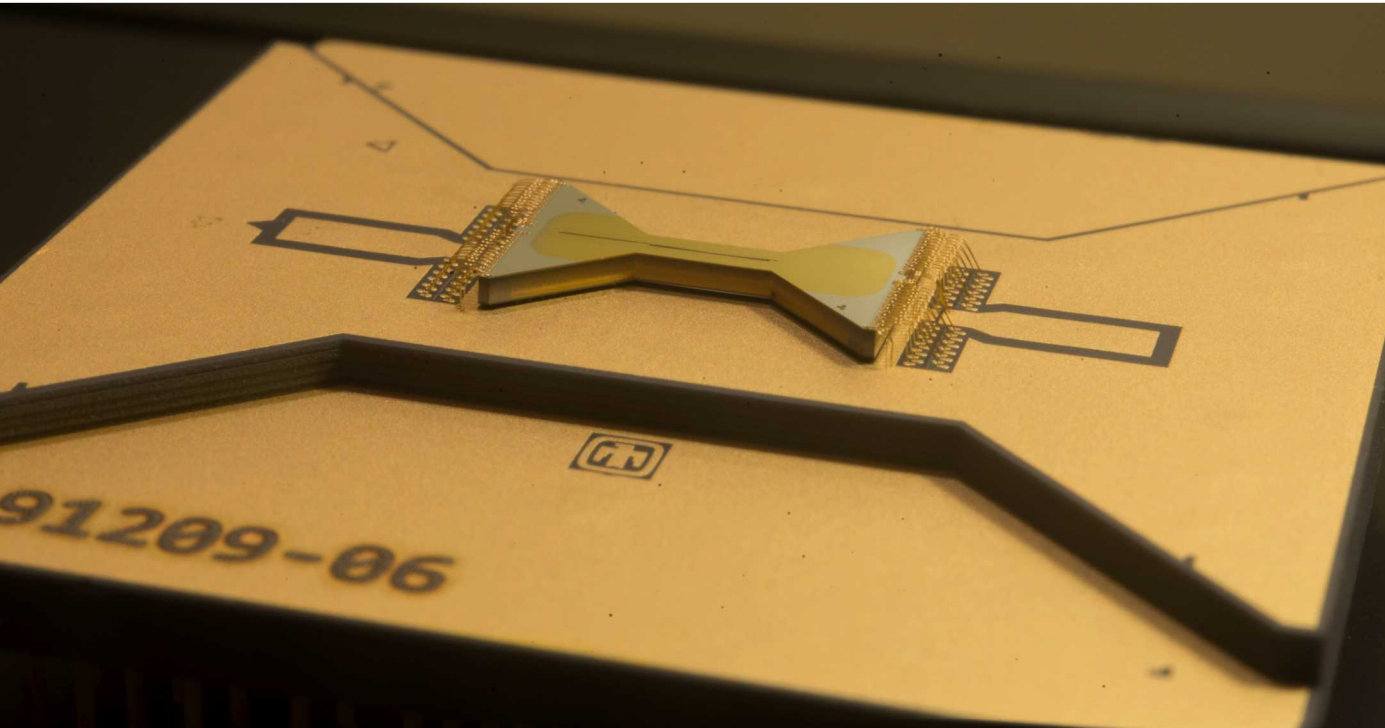


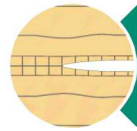
## Solder die attach characterization

- After solder die attach
  - Shear force  $\approx 50\text{N}$
- After temperature cycling between room temperature and 77K
  - All die still attached
  - No cracks or other problems
  - Shear force  $\approx 50\text{N}$

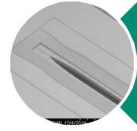


# Custom trap package Is available

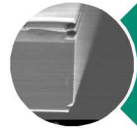




Phoenix trap design



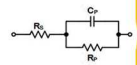
Phoenix trap fabrication and testing



Prompt-onset fields and ion heating



Phoenix package



Rf-dissipation



Peregrine trap



Quantum Scientific Open User Testbed (QSCOUT)

## Phoenix trap design, Reduced rf dissipation

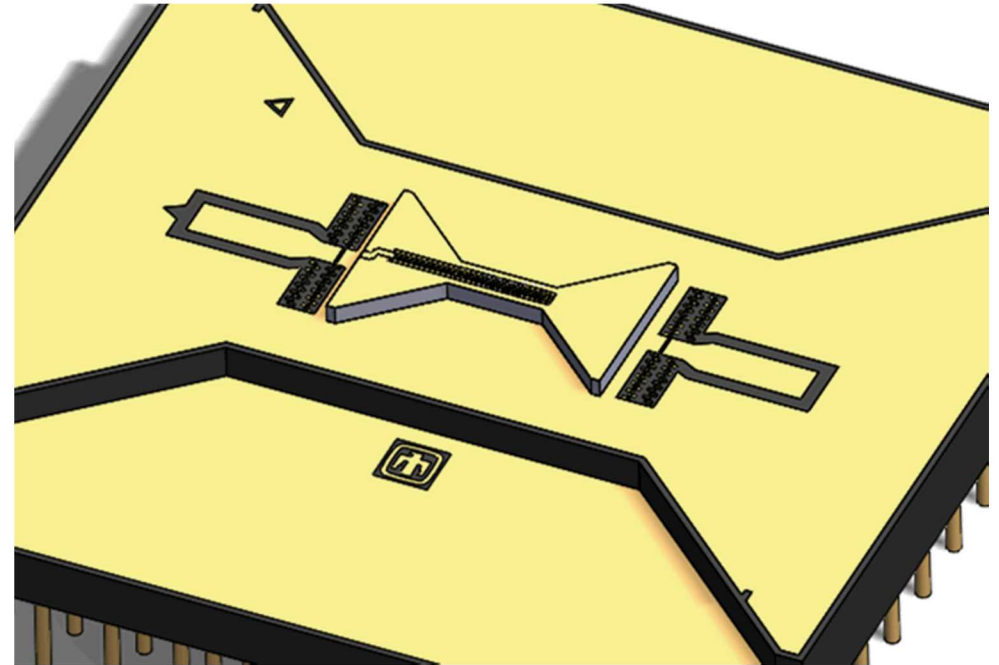
RF dissipation was identified as a challenge in HOA-2 traps

Resistive losses in device  $P_s$

$$P_s \approx \frac{1}{2} R_s U^2 \omega^2 C_p^2 \propto L^3$$

Approach to reduce rf dissipation in Phoenix traps

- Reduce rf capacitance
  - Reduce length of trap
  - Separate rf and ground as far as possible
- Reduction of resistance, systems approach
  - Dimension of rf routing between bondpad and electrodes
  - Dedicated rf and ground signals on custom package
    - Rf routed on outside
    - Parallel vias for rf and ground



## Rf-dissipation in traps electrical characterization of fabricated Phoenix devices

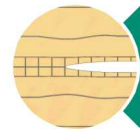
For 100 V amplitude at 100 MHz:

Trap	Temp	$C_p$	$R_s$	$R_p$	$P_s$	$P_p$
Peregrine (measurement) (estimate)	300 K	5.4 pF	0.36 $\Omega$		20 mW	
	4 K		0.05 $\Omega$		3 mW	
Phoenix (measurement) (estimate)	300 K	7.1 pF	0.4 $\Omega$		35 mW	
	4 K		0.05 $\Omega$		5 mW	
HOA-2.1	300 K	7.6 pF	0.9 $\Omega$	1.6 M $\Omega$	100 mW	3.1 mW
	77 K		0.7 $\Omega$		80 mW	
	4 K		0.5 $\Omega$		60 mW	
Au/FS	300 K	1.93 pF	2.0 $\Omega$	1.4 M $\Omega$	15 mW	3.7 mW
	77 K		1.3 $\Omega$		10 mW	
	4 K		0.8 $\Omega$		5.9 mW	
Thunderbird	300 K	2.4 pF	0.6 $\Omega$	1.5 M $\Omega$	6.7 mW	3.3 mW

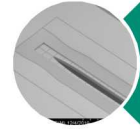
$$P_s \approx \frac{1}{2} R_s U^2 \omega^2 C_p^2$$

$$P_p = \frac{1}{2} \frac{\omega U^2}{R_p}$$

Phoenix traps: 3x lower dissipation than HOA-2 traps  
Peregrine traps: 5x lower dissipation than HOA-2 traps



Phoenix trap design



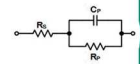
Phoenix trap fabrication and testing



Prompt-onset fields and ion heating



Phoenix package



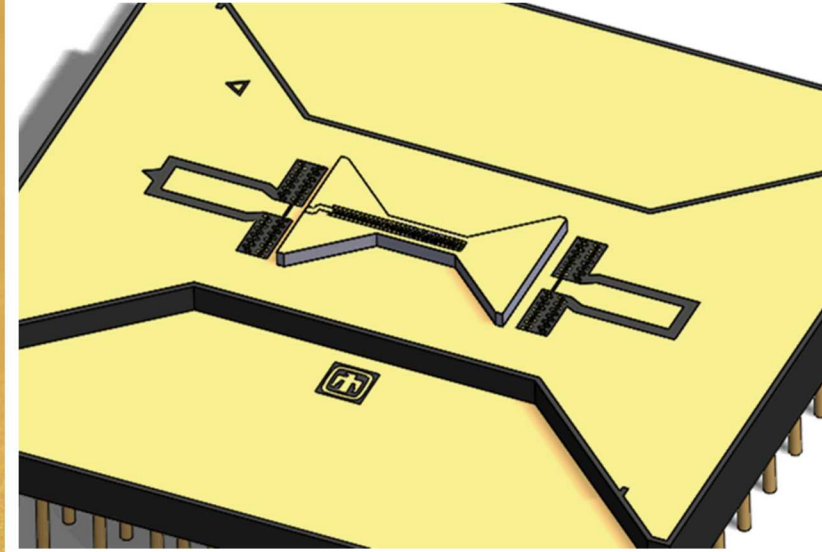
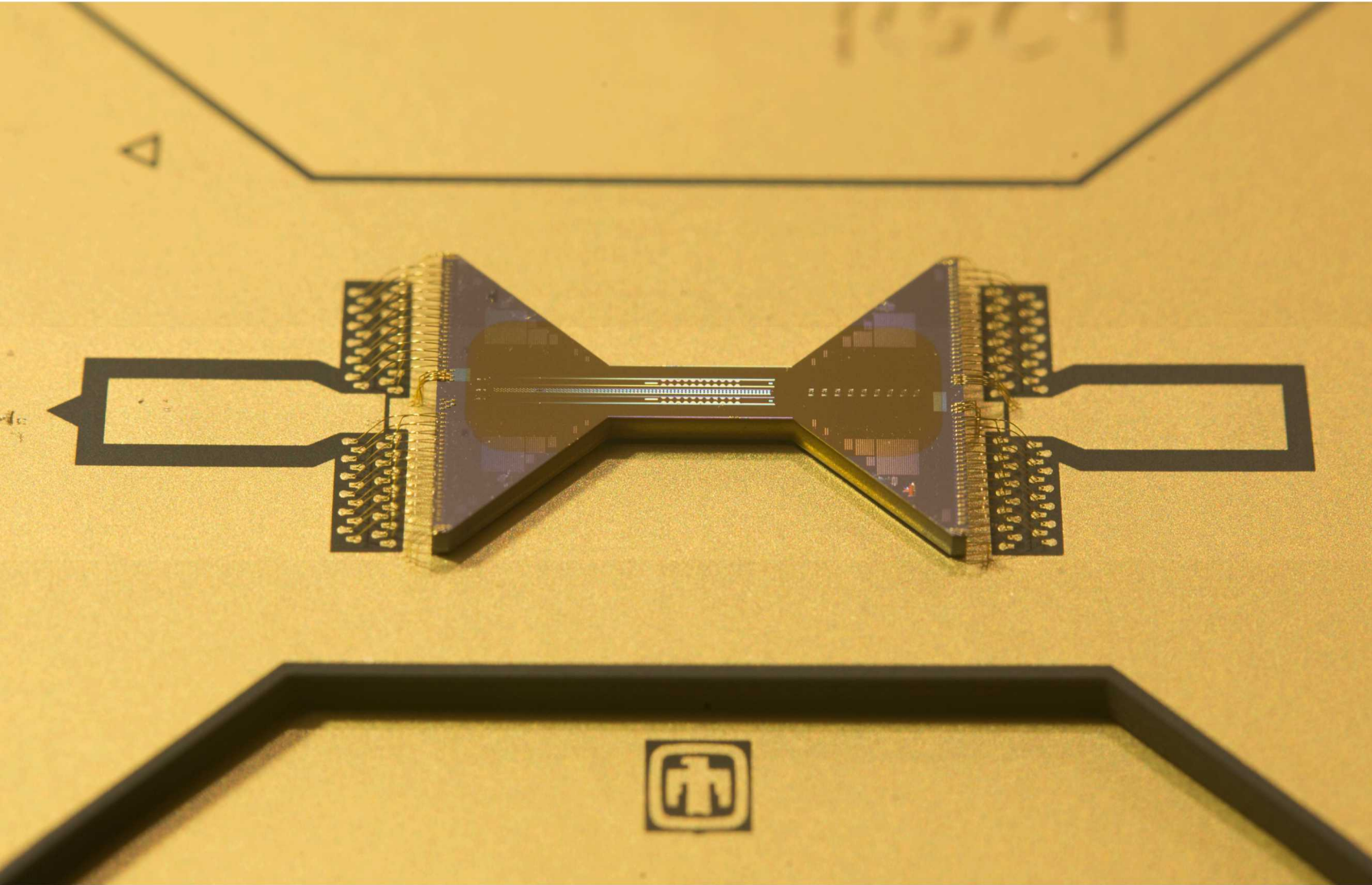
Rf-dissipation



Peregrine trap



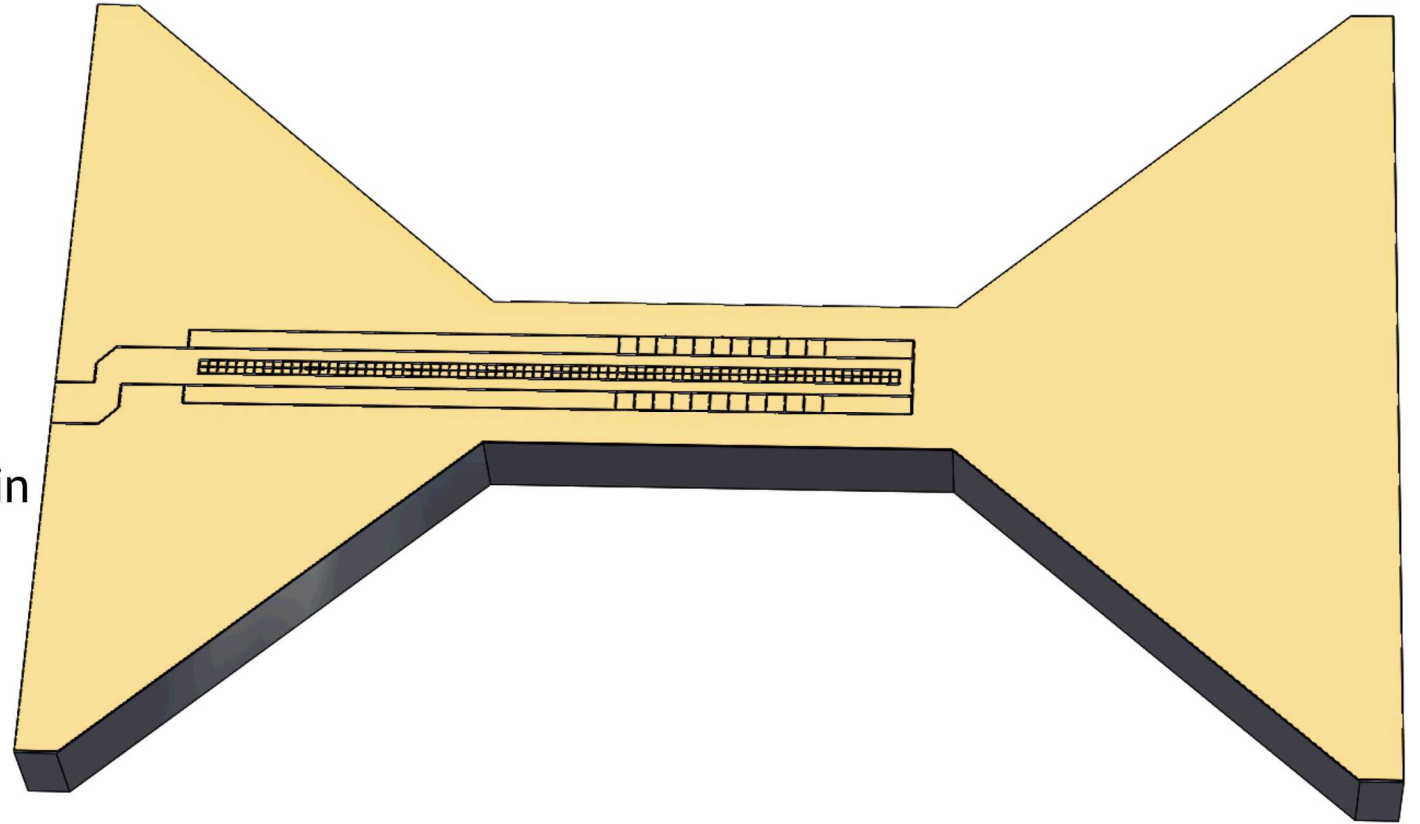
Quantum Scientific Open User Testbed (QSCOUT)



## QSCOUT Peregrine surface trap

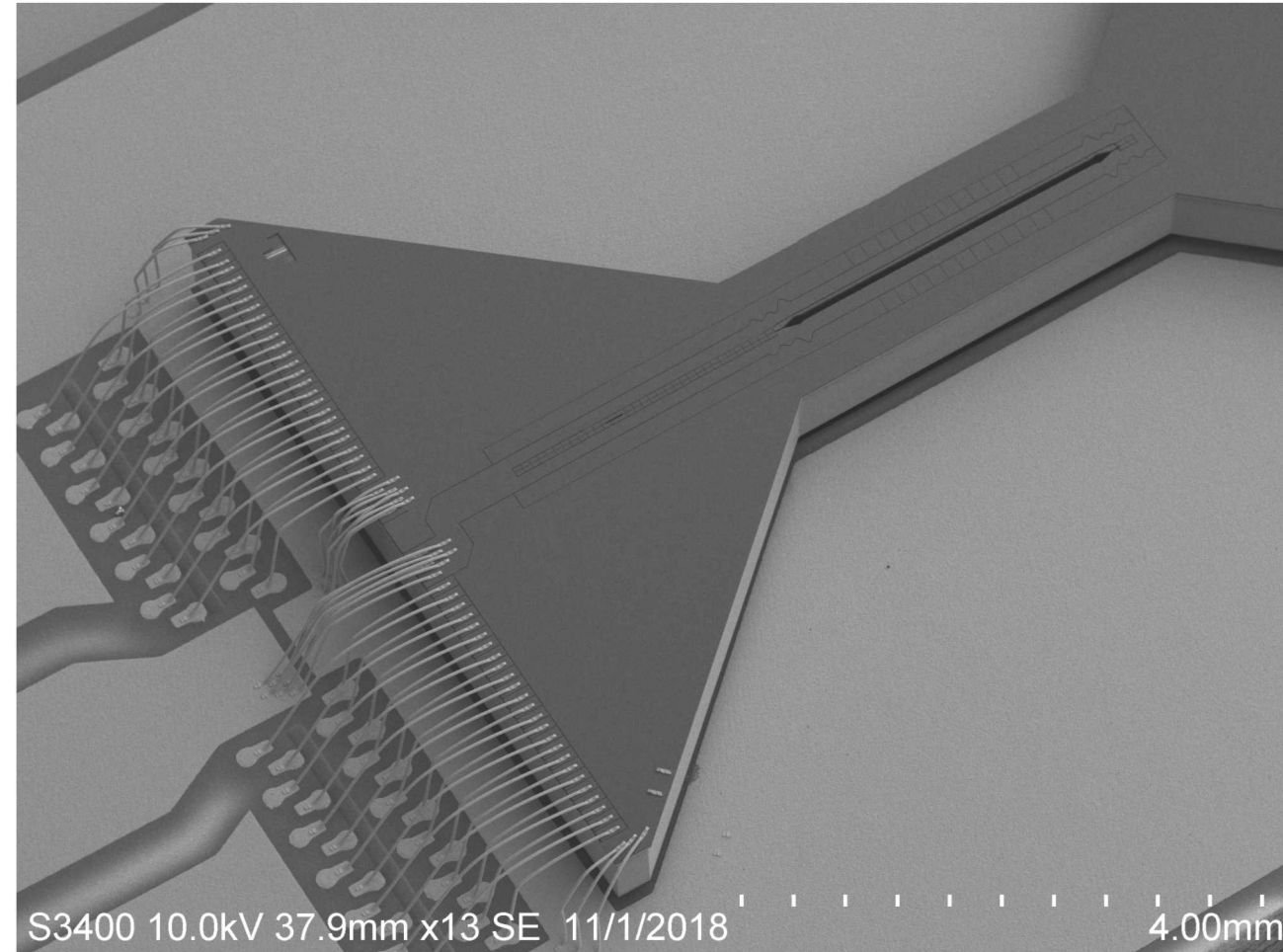
DOE Quantum testbed for Science project QSCOUT  
Surface trap fabrication

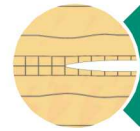
- Co-fabricated with LogiQ Phoenix trap
- Pure surface trap  
all electrodes on top metal layer
- Identical loading hole
- Identical electrode wiring
- Can be available to researchers interested in testing the trap and providing feedback



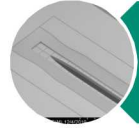
## Timeline for Phoenix and Peregrine trap deliveries

- January 2020
  - Delivery of traps to Sandia experimental team for testing
- March 2020
  - Delivery of tested traps to LogiQ performers
- Traps will be available in
  - Pin grid array packages
  - Land grid array packagesCustom packages backwards compatible with HOA-traps

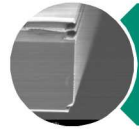




Phoenix trap design



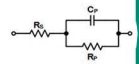
Phoenix trap fabrication and testing



Prompt-onset fields and ion heating



Phoenix package



Rf-dissipation



Peregrine trap

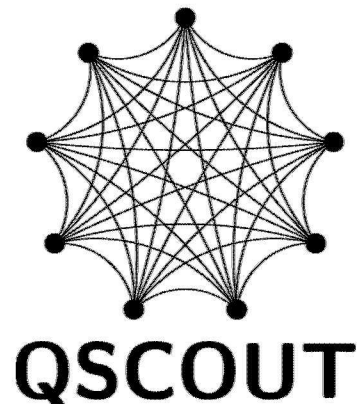


Quantum Scientific Open User Testbed (QSCOUT)

Testbed systems designed for open access to support scientific applications

- High-fidelity operations  $\#gates \propto (\#qubits)^2$
- Gate-level access
- Open system with fully specified operations and hardware
- Low-level access for optimal control down to gate pulses
- Open for comparison and characterization of gate pulses
- Open for vertical integration by users

<https://qscout.us>  
<https://qscout.sandia.gov>

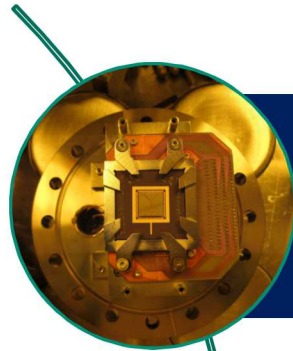


**Duke**  
UNIVERSITY

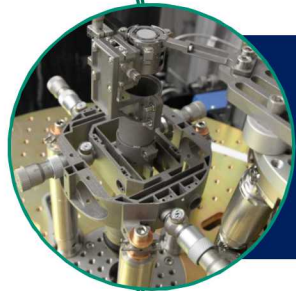
Ken Brown et al.



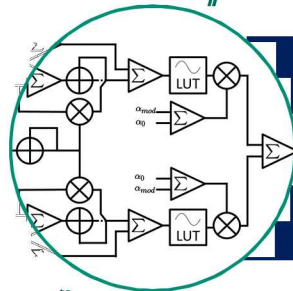
Peter Love et al.



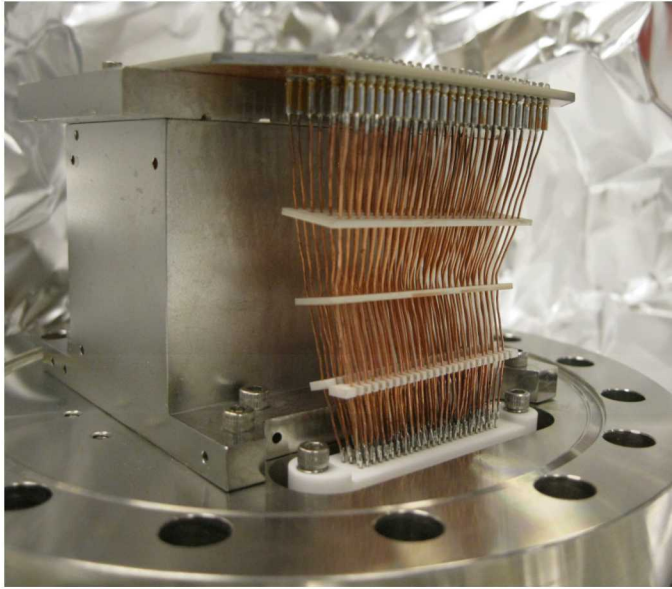
Reducing background collisions  
Vacuum technology



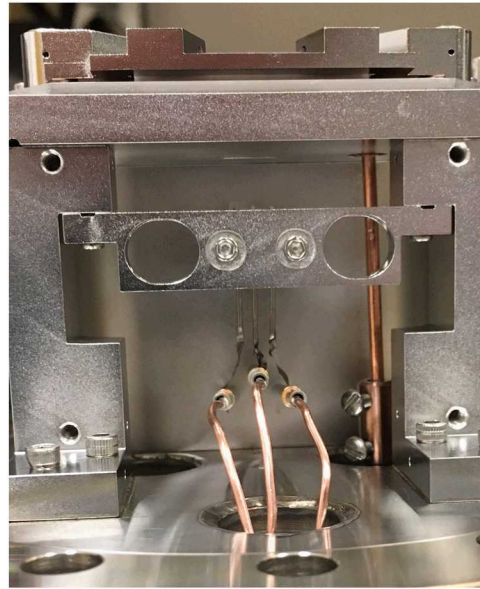
Individual addressing  
Optical and mechanical engineering



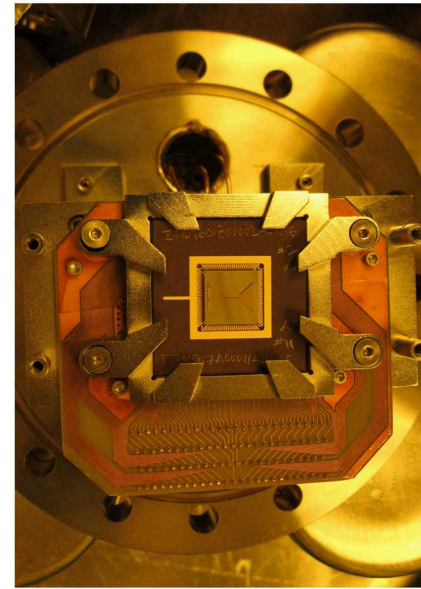
Coherent Pulse control  
Electrical engineering



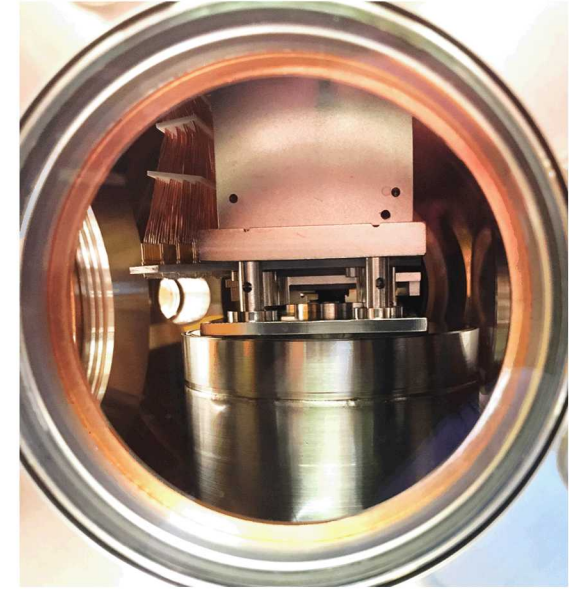
*Bare copper wires with Al<sub>2</sub>O<sub>3</sub> spacers*



*3 Yb ovens (loading slot, Peregrine loading hole, HOA loading hole)*



*Trap installed for final bake*



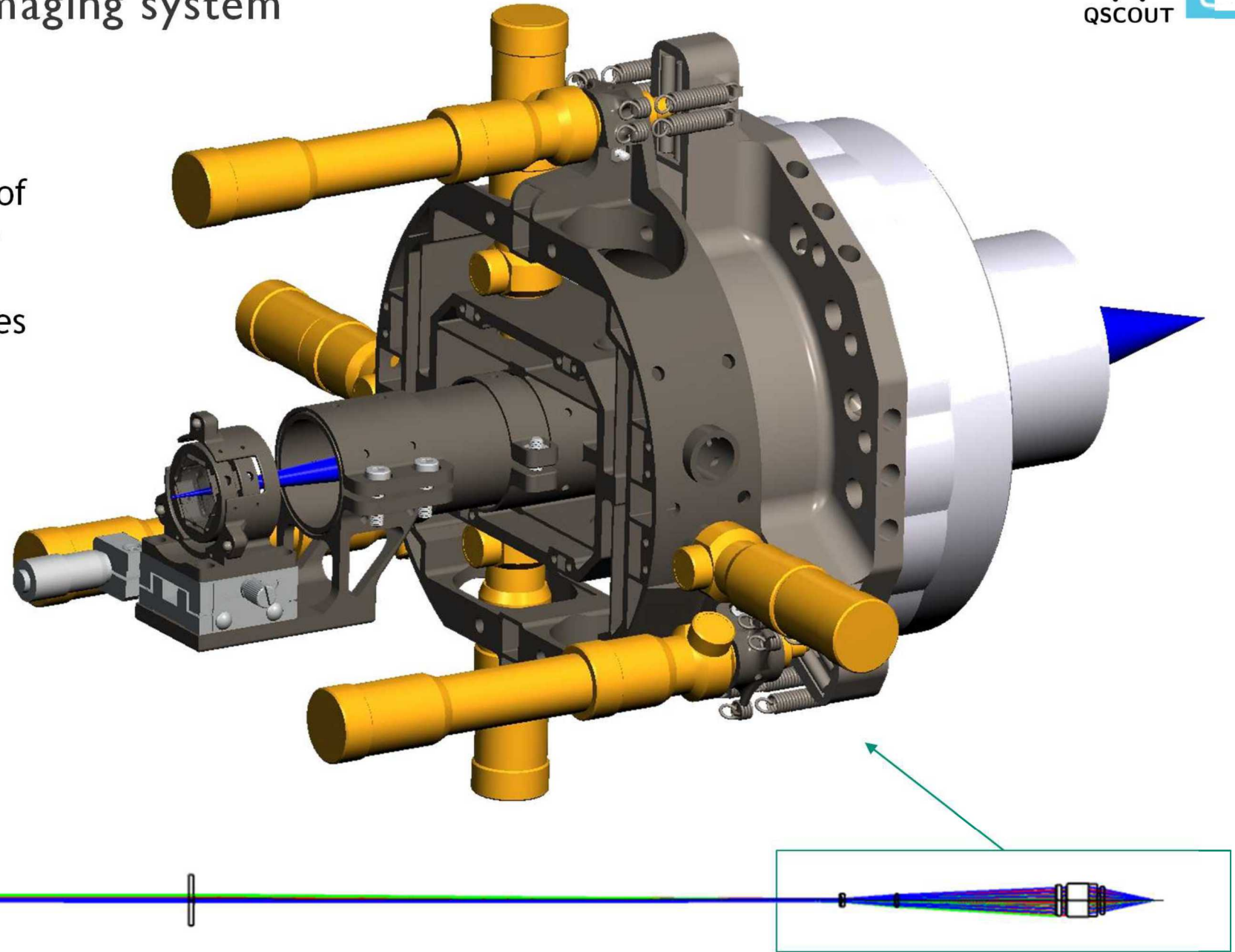
*Trap platform in chamber, both re-entrants visible*

### Features (hydrogen and organic mitigation):

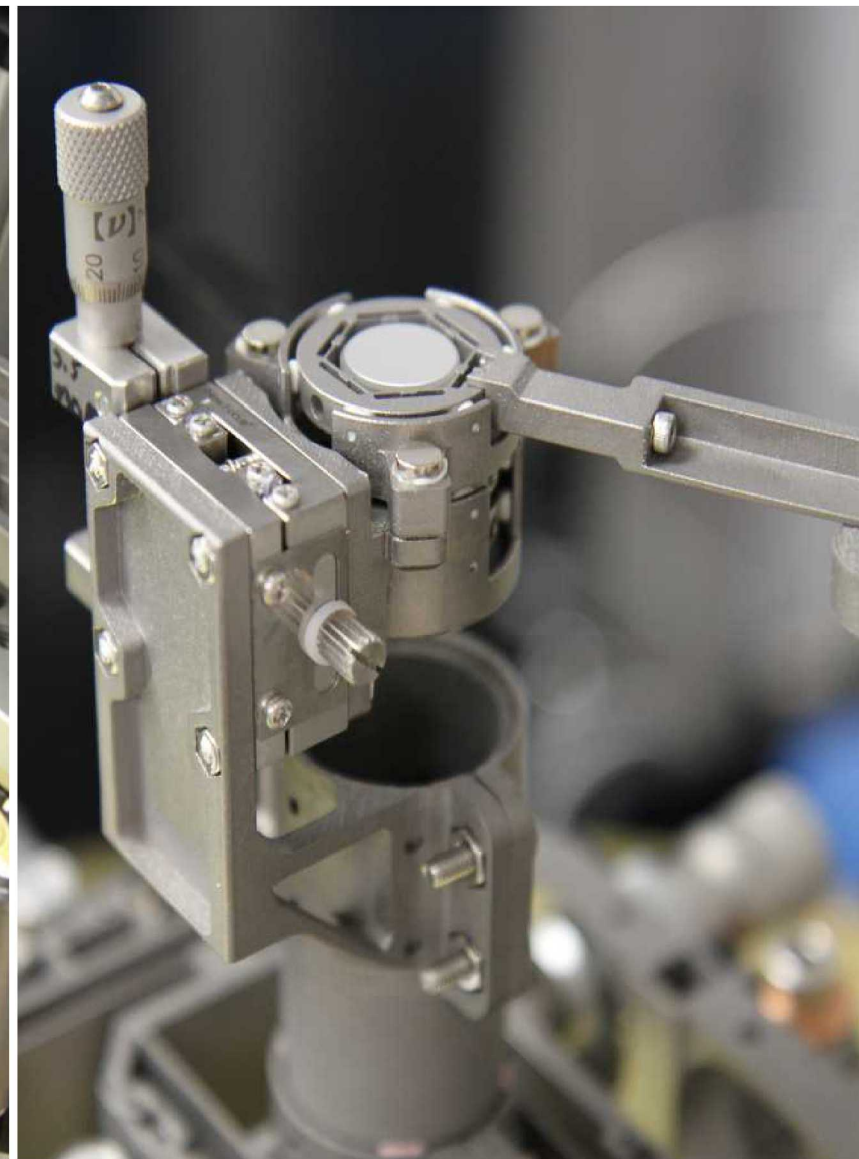
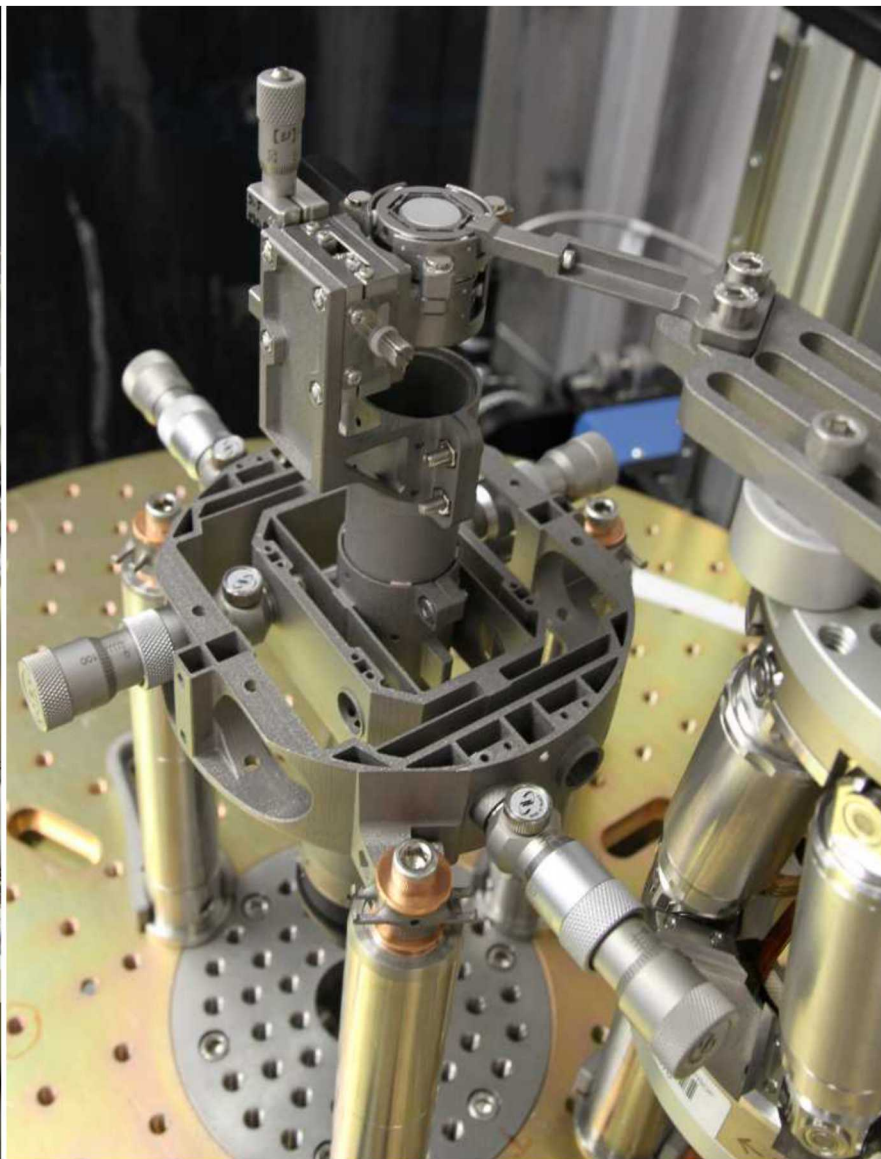
- 316L stainless steel subjected to high-temp bake process for UHV performance
- Organics free: Ceramics replacements
  - MACOR fuzz button spacer & Micro-D connector shell
  - AlN and Al<sub>2</sub>O<sub>3</sub> circuit board
- Bare copper wires for RF and DC voltages

Custom design to

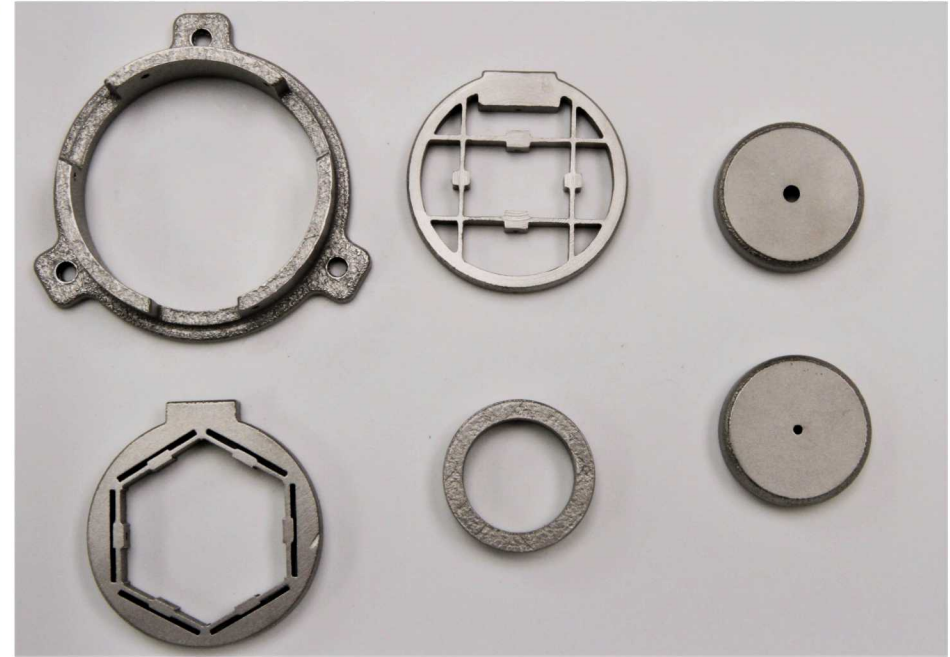
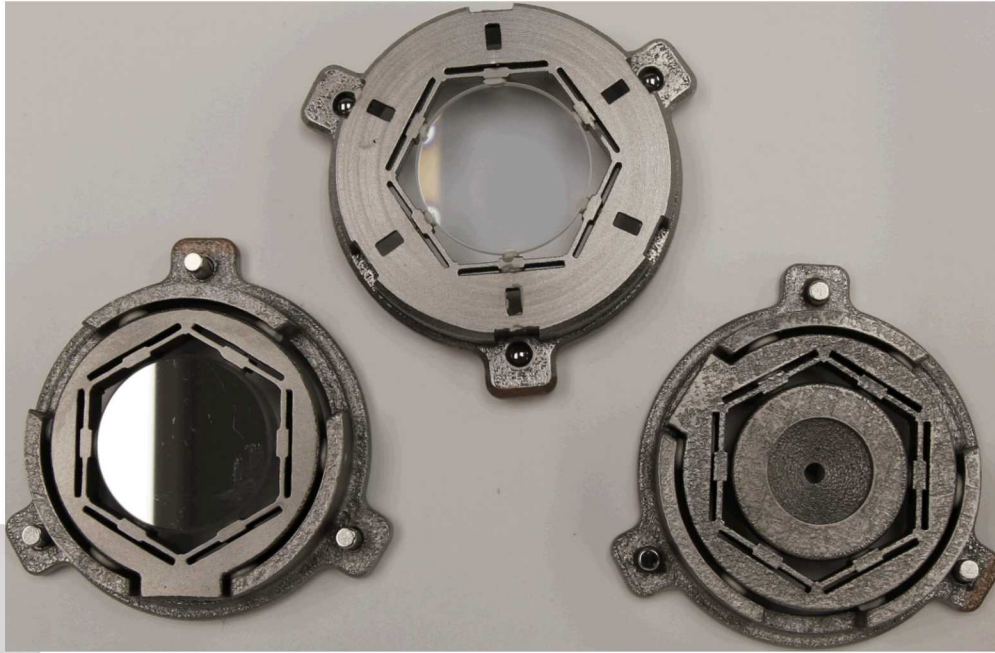
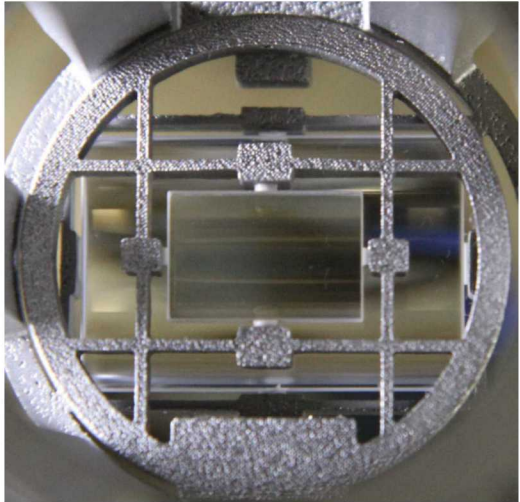
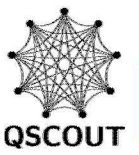
- Accommodate needed degrees of freedom in very cramped space
- Resilient to temperature changes
- Provide the needed stability



# Individual Addressing Relay Subassembly

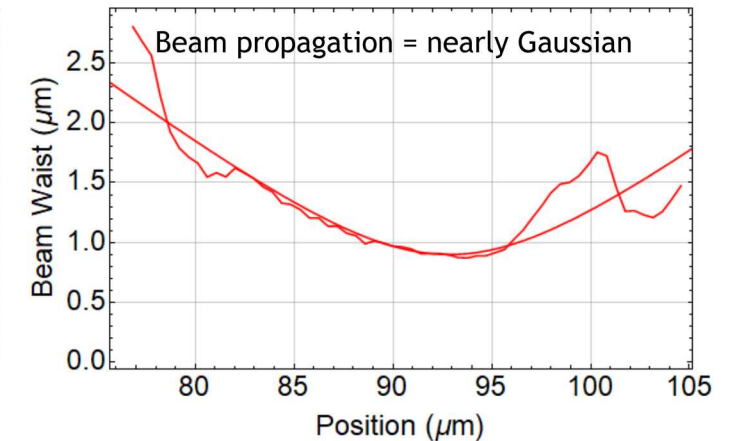
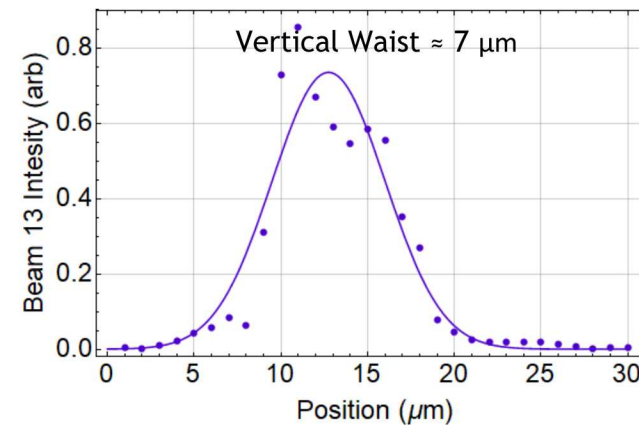
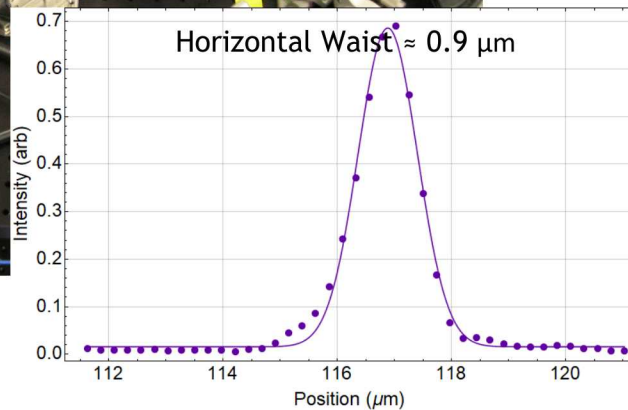
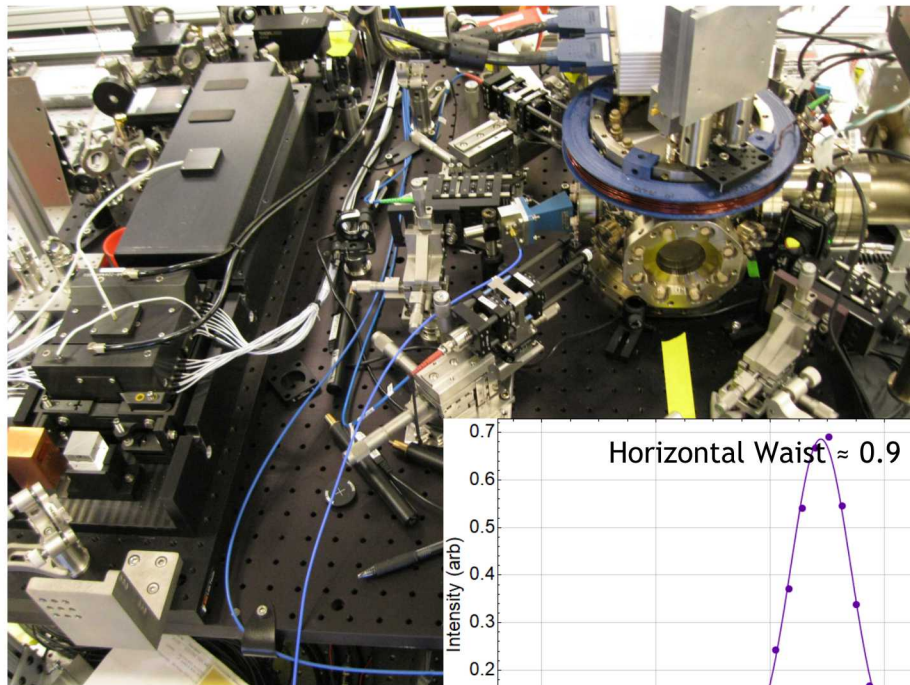
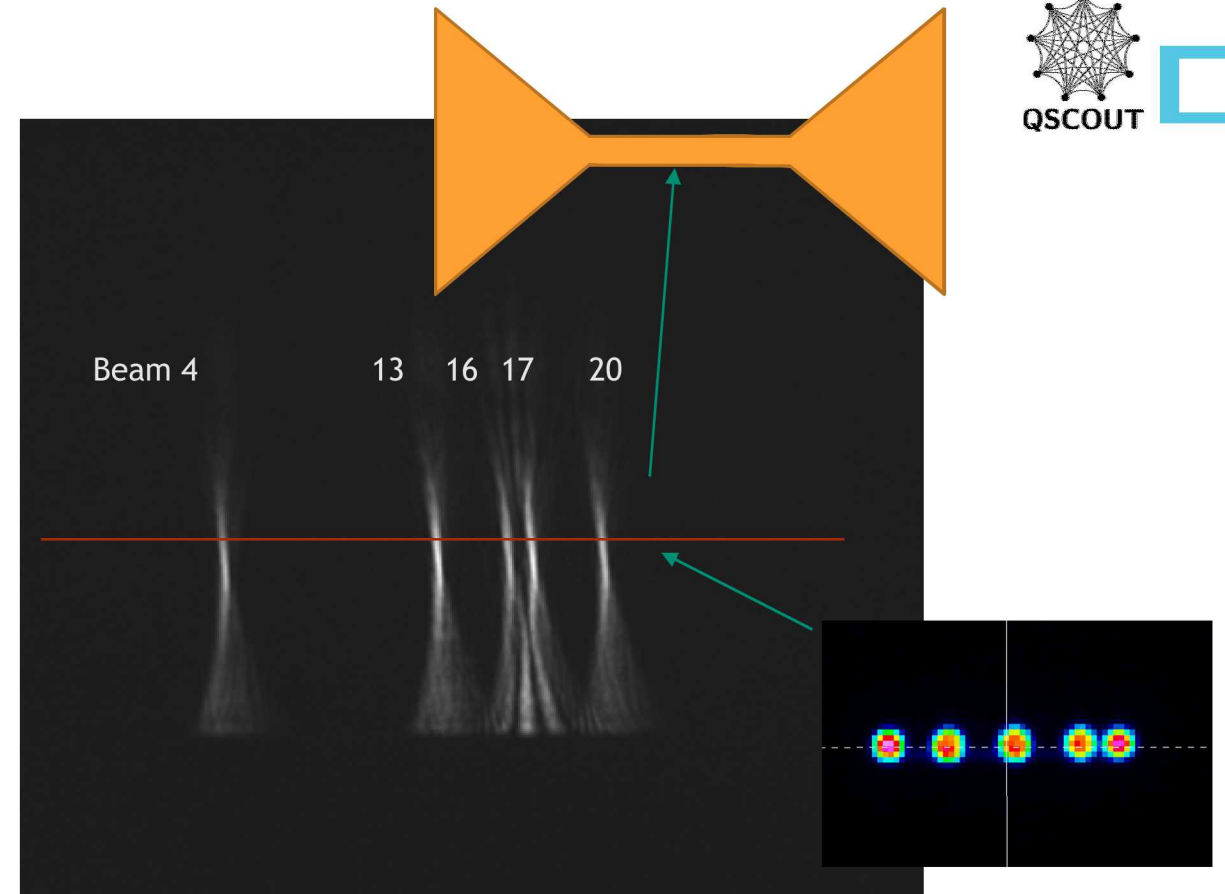


# Flexure mounts for active alignment

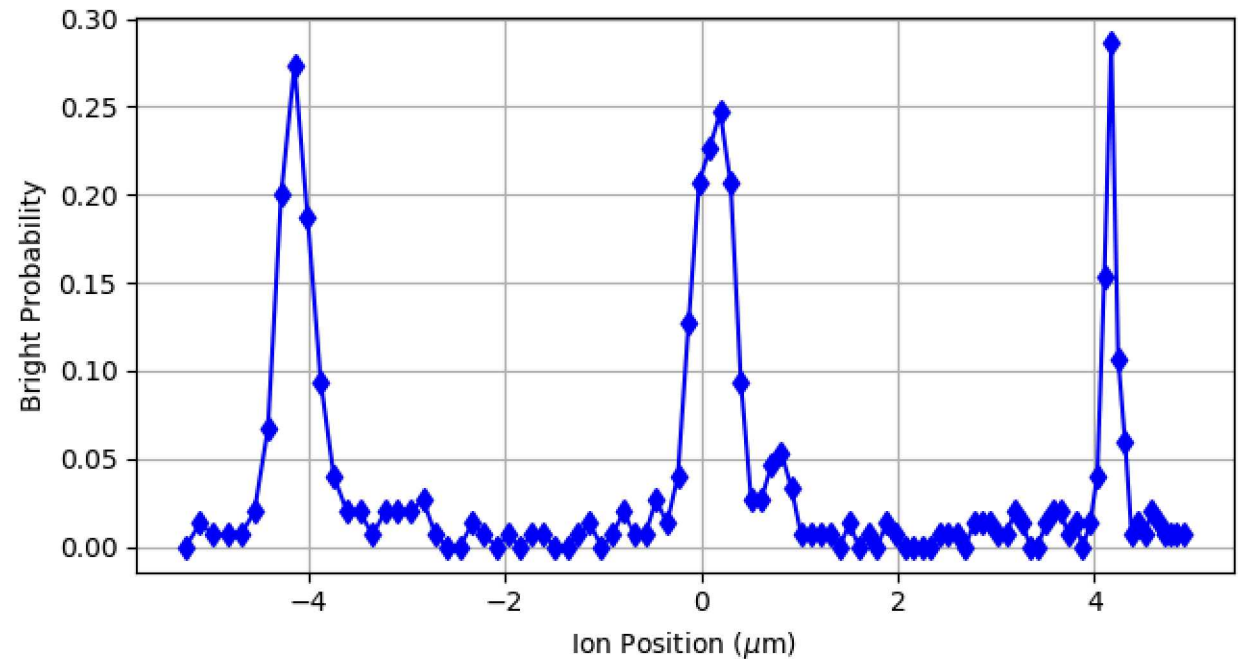
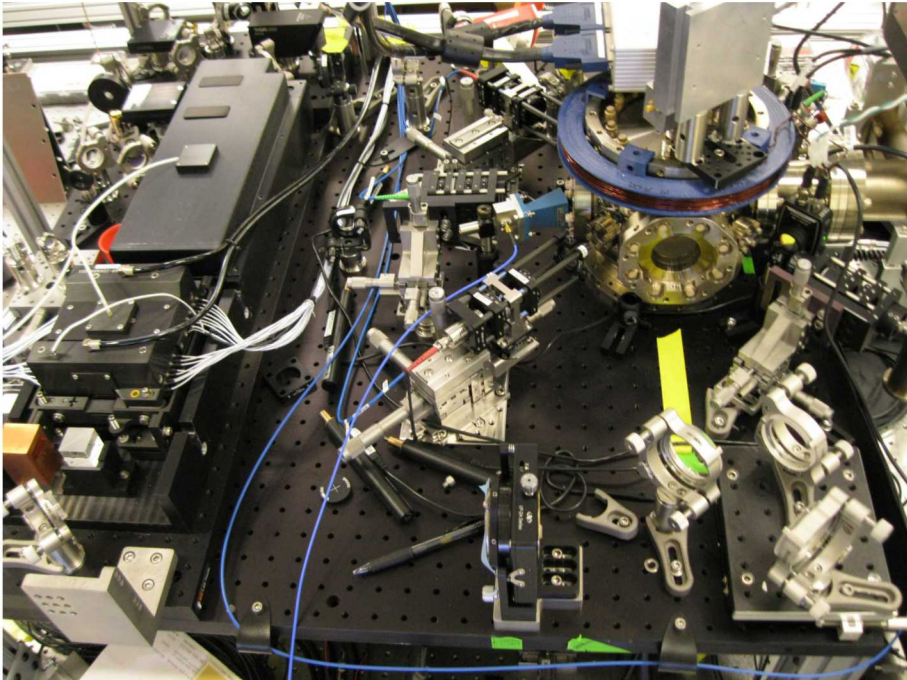


# Qubit Laser – Apparatus Test

- Adjacent beams are clearly separated, and about  $5\ \mu\text{m}$  apart.
- The beam waists are nearly the designed values.
- The apparent optical crosstalk is small, but we need to measure using an ion.



- Co-propagating Raman transitions
- Three central beams are illuminated
- A single ion is moved through the beam
- For each position the probability to flip the spin is measured

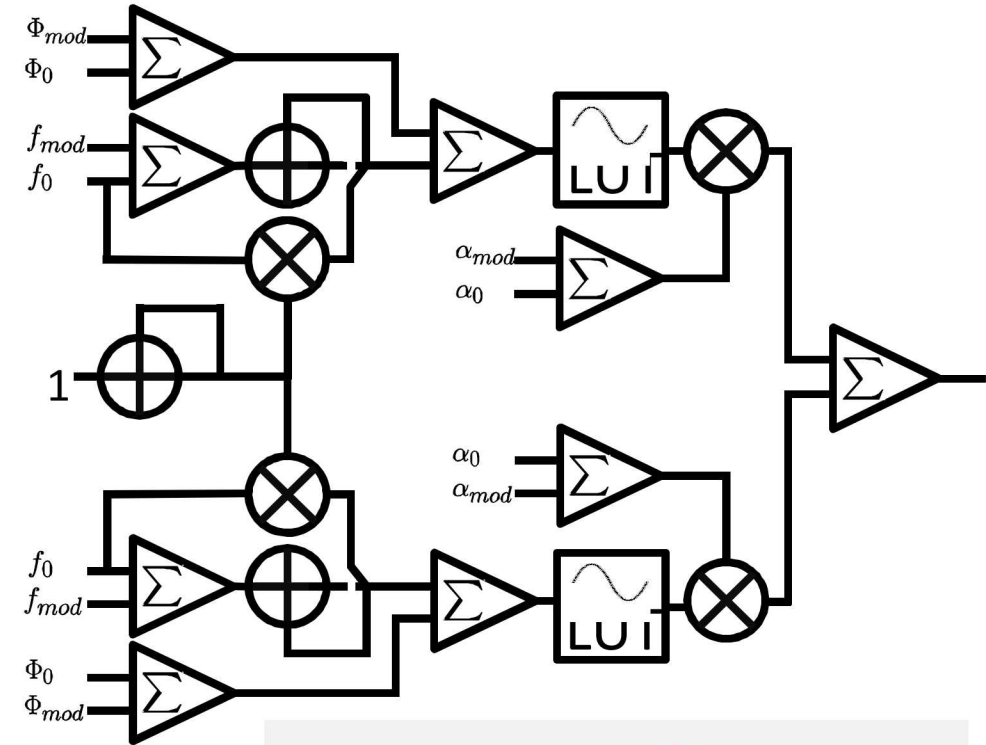
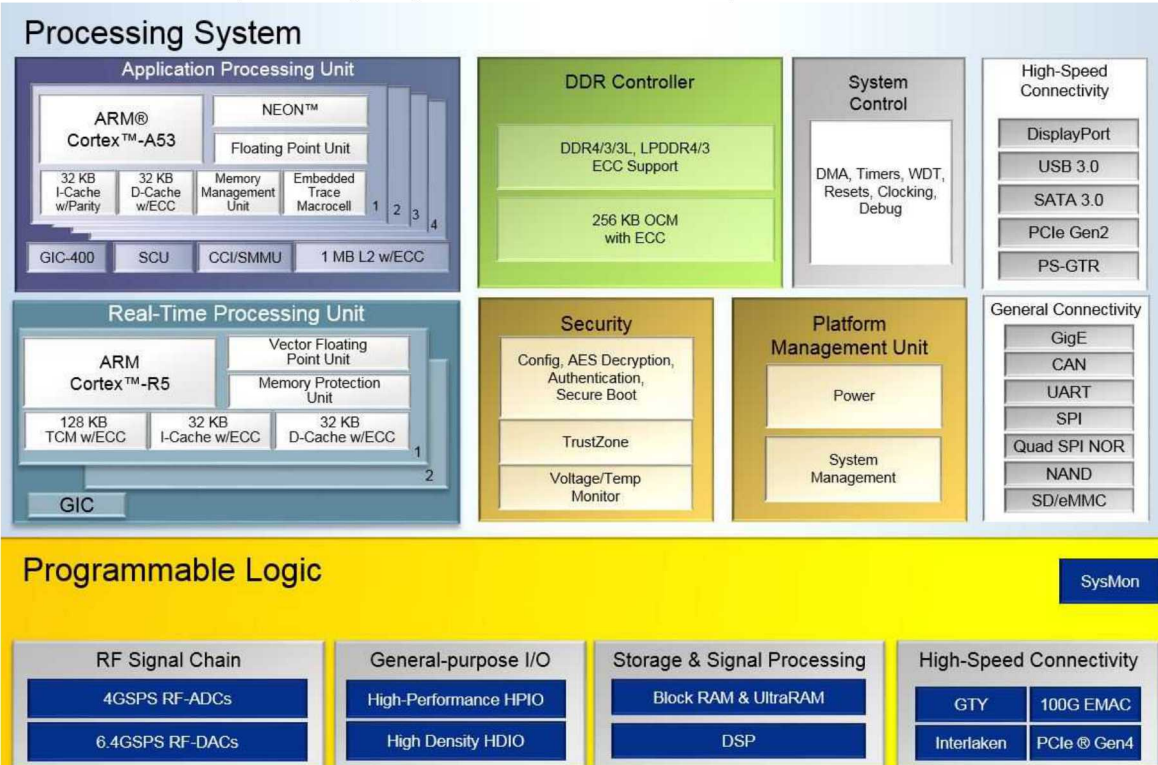


- Focal size

# RFSoc for coherent pulse generation

- Two tones per channel
- Coherent output synchronized between all channels
- Pulse envelopes and frequency- phase- modulation defined by splines
- Compact representation of gates for efficient streaming of circuits
- AOM Cross-talk compensation

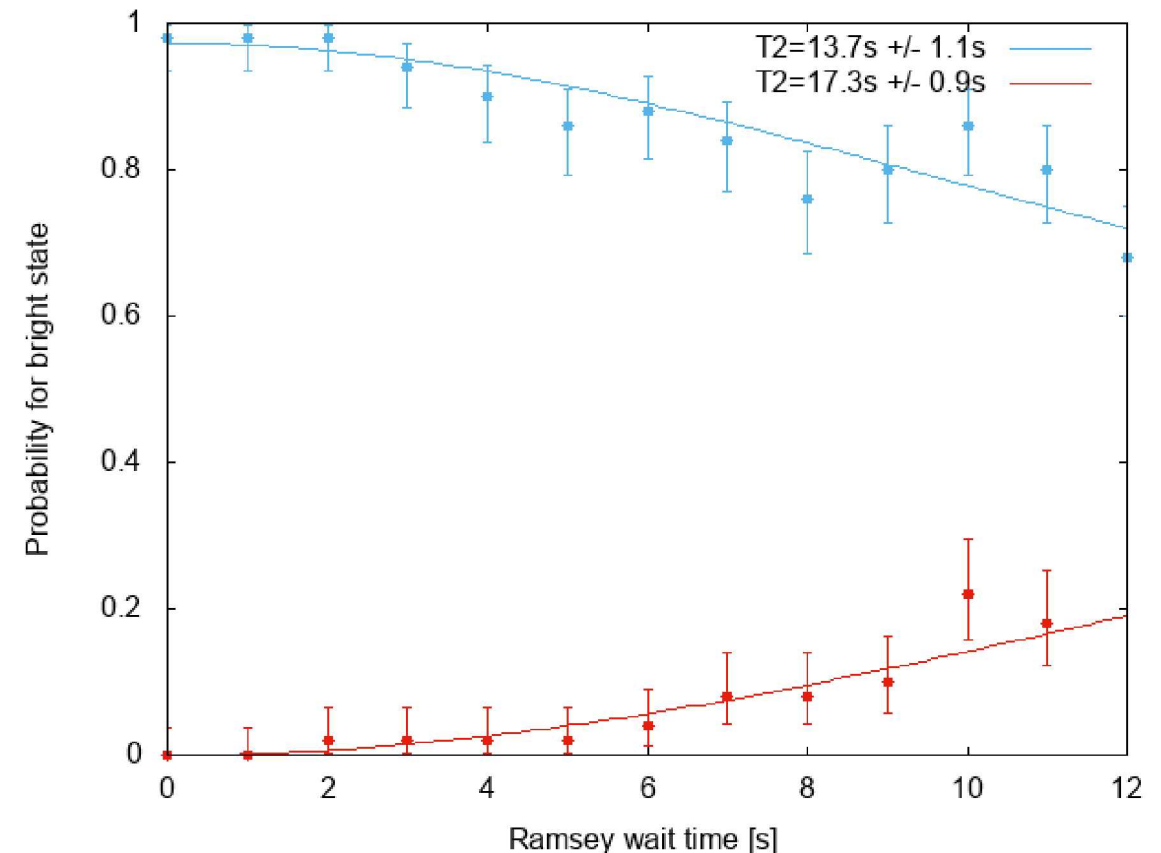
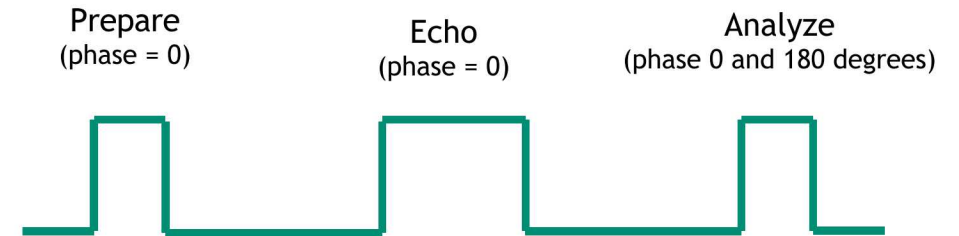
## Radio-Frequency System on a Chip



- QSCOUT apparatus
- Microsemi Cs clock and Ultra-stable oscillator
- RFSoc output single-sideband mixed with Microwave Dynamics 12.6GHz source
- No explicit magnetic field shielding or stabilization

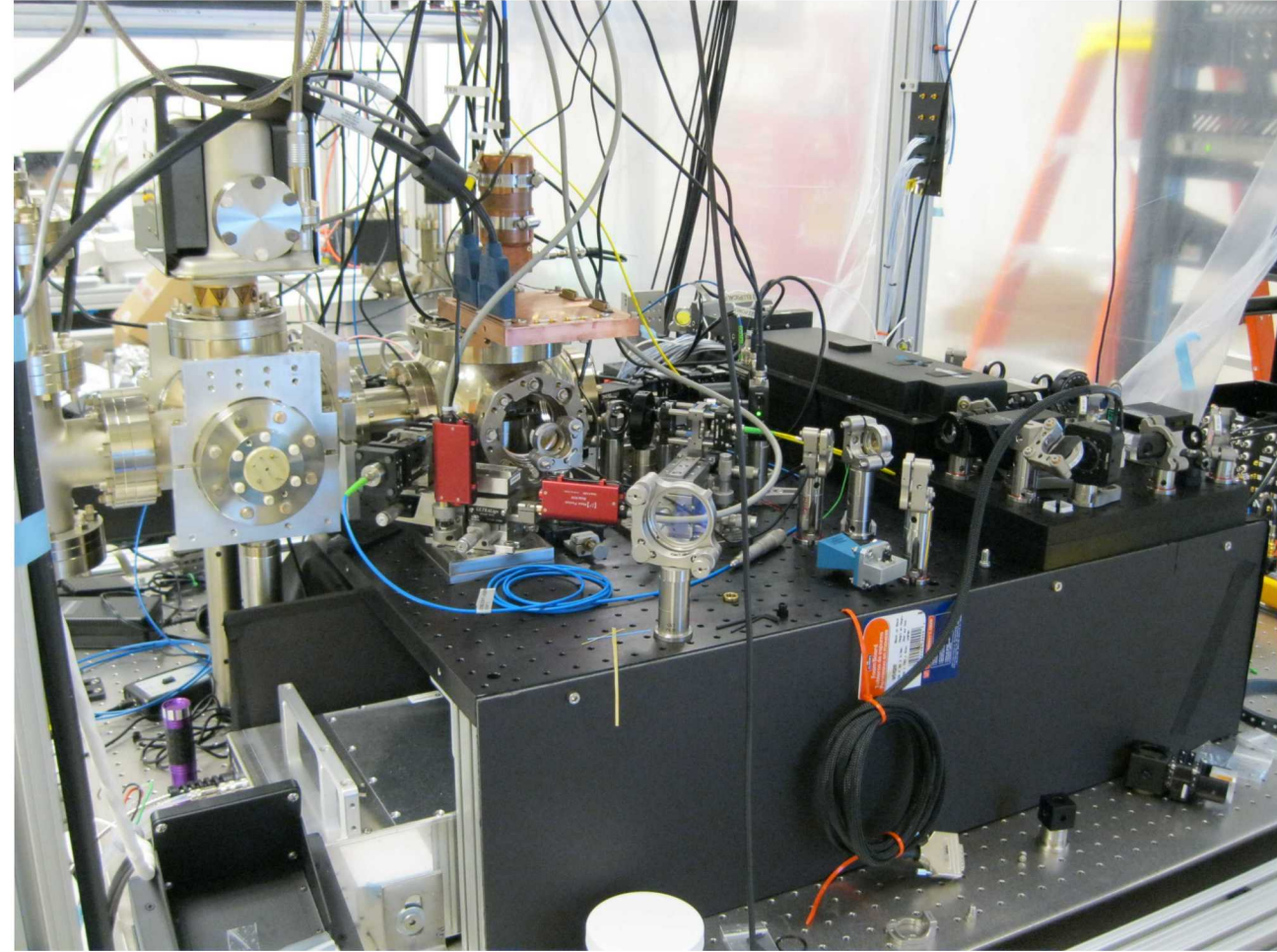
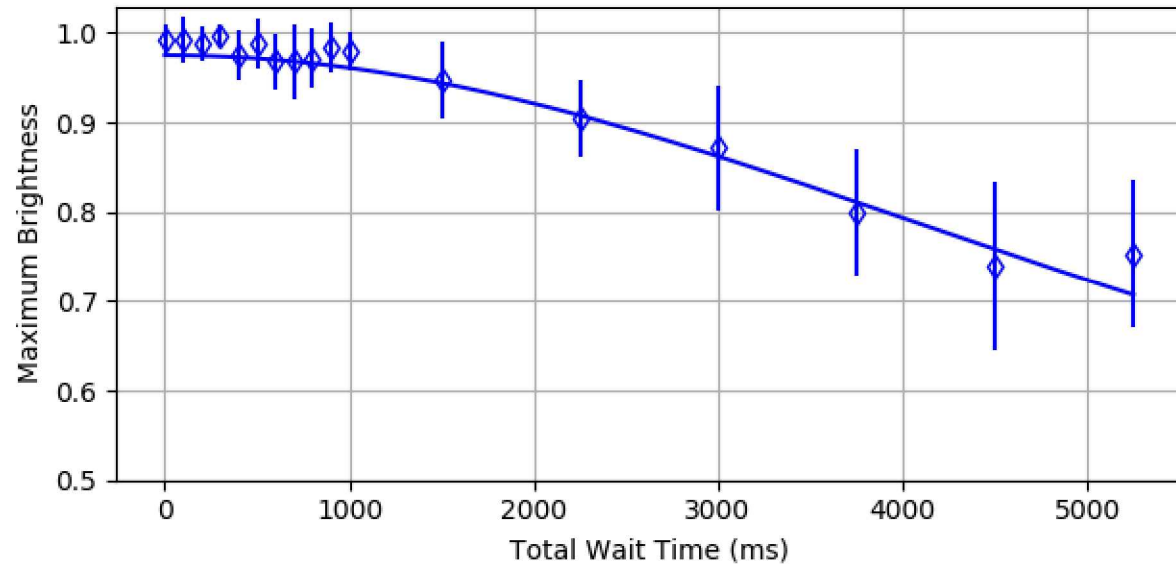
- Measured  $T_2^*$  coherence time  $13.7s \pm 1.1s$
- Bright state limited by ion heating in trap
- Dark state indicates a coherence time (excluding the effect of ion heating) of  $17.3s \pm 0.9s$

### Ramsey Sequence



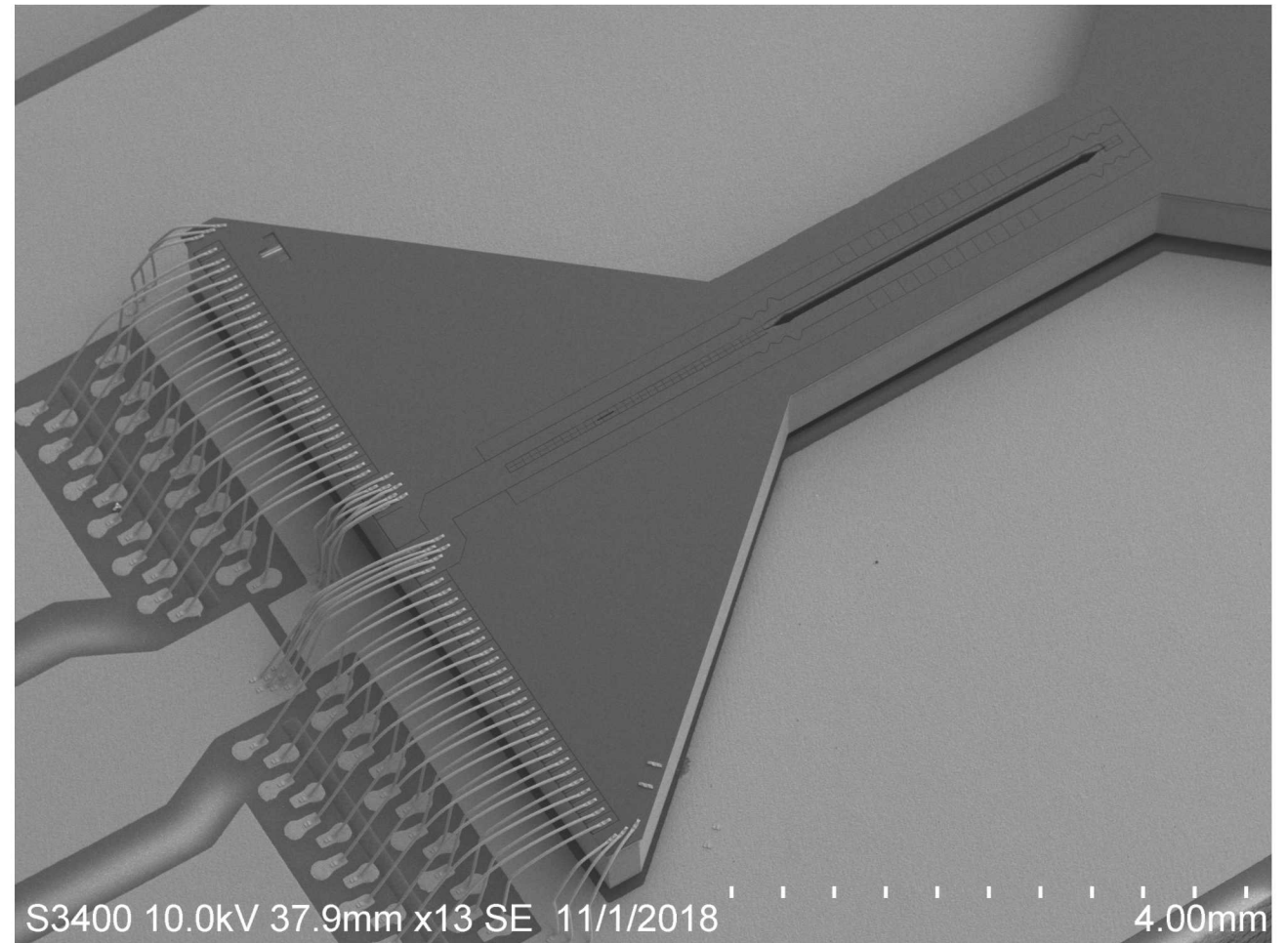
# RFSoc Raman coherence time

- Raman transitions using large global beam
- Beat-note lock of Paladin 355nm pulsed laser realized on RFSoc
- RFSoc drives both tones needed to realize Raman transitions
- Coherence time  $> 5\text{s}$



### Phoenix trap

- Finally completed fabrication
- Currently being tested
- Available to Performers in March 2020



# Thanks

## *Trap design and fabrication*

Matthew Blain  
Ed Heller  
Corrie Herrmann  
Becky Loviza  
John Rembetski  
Paul Resnick  
SiFab team

## *Trap packaging*

Ray Haltli  
Andrew Hollowell  
Anathea Ortega  
Tipp Jennings

## *Theory*

Setso Metodi  
Brandon Ruzic

## *Trap design and testing*

Peter Maunz  
Craig Hogle  
Daniel Lobser  
Melissa Revelle  
Dan Stick  
Christopher Yale

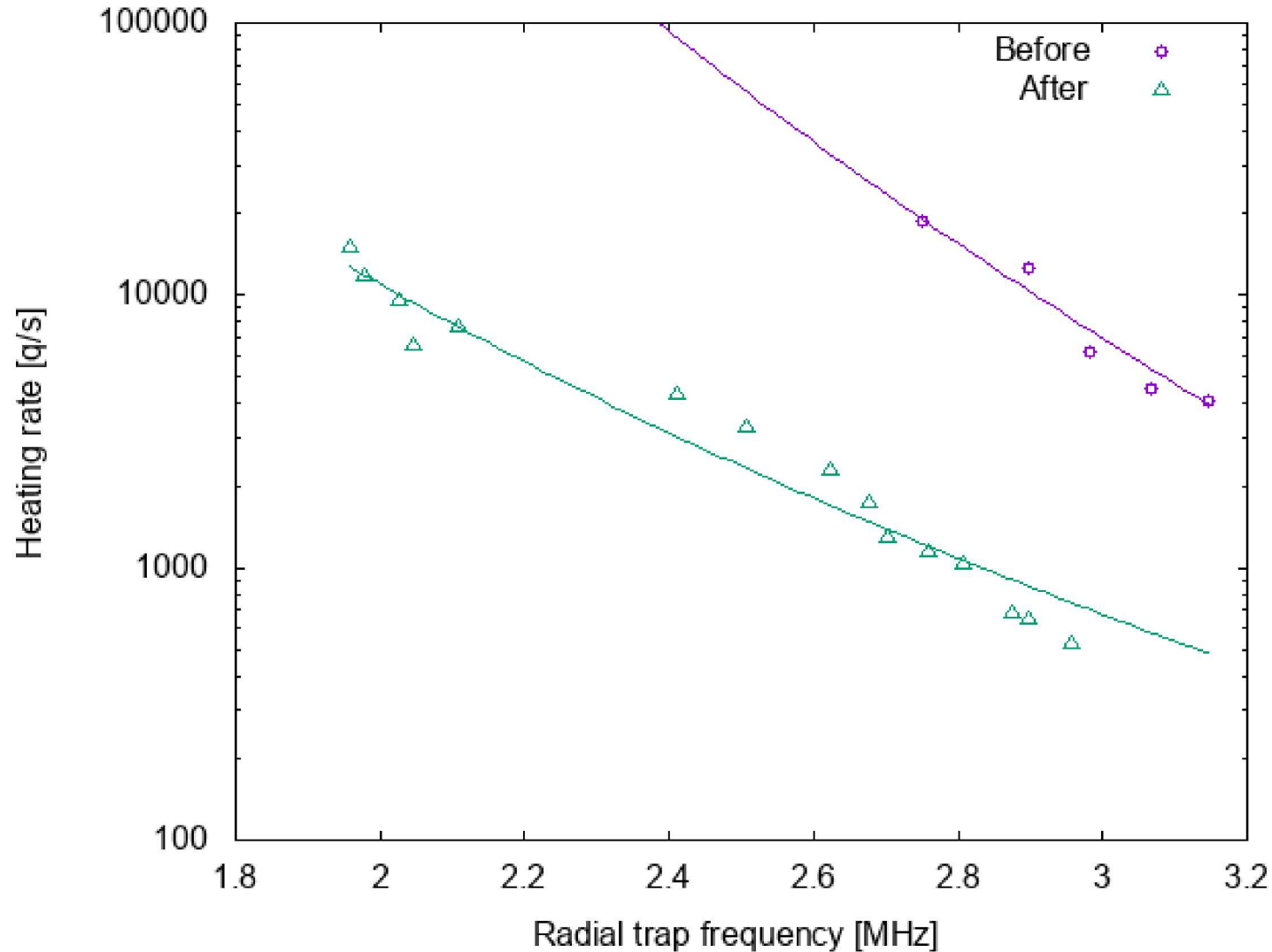
## *RF Engineering*

Christopher Nordquist  
Stefan Lepkowski



# Backup slides

# Heating rate dependency on radial trap frequency



Changes between 2/19 and 3/19

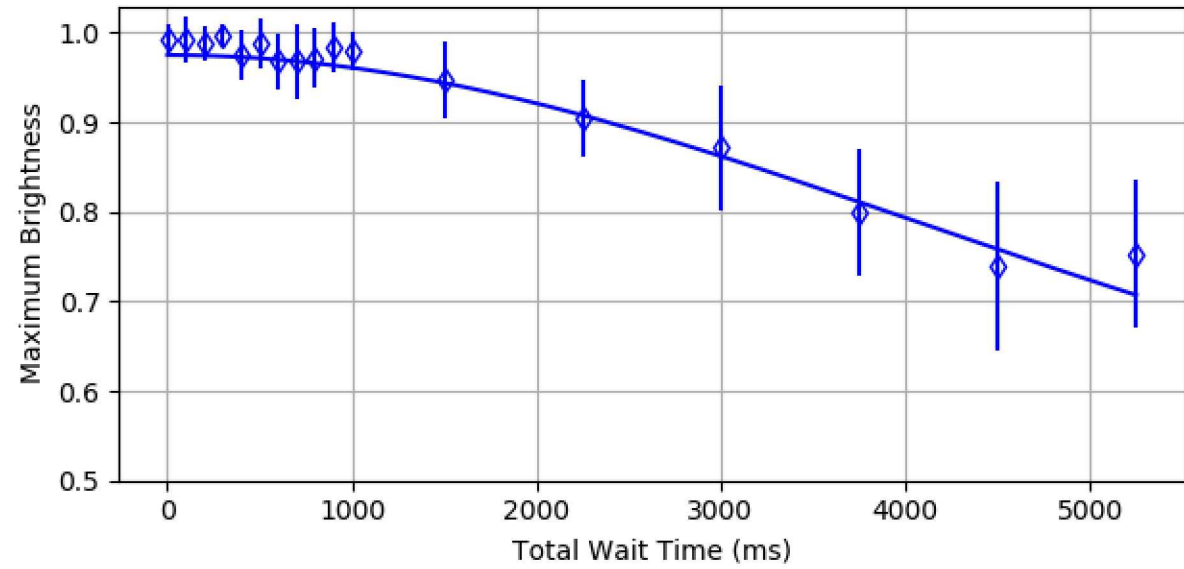
- Heating to 80K
- Reduced (room-temperature) pressure from  $7 \times 10^{-10}$  to  $7 \times 10^{-11}$

Purple (before heating) shown with approximated power law

$$\dot{n} \propto f^{-11}$$

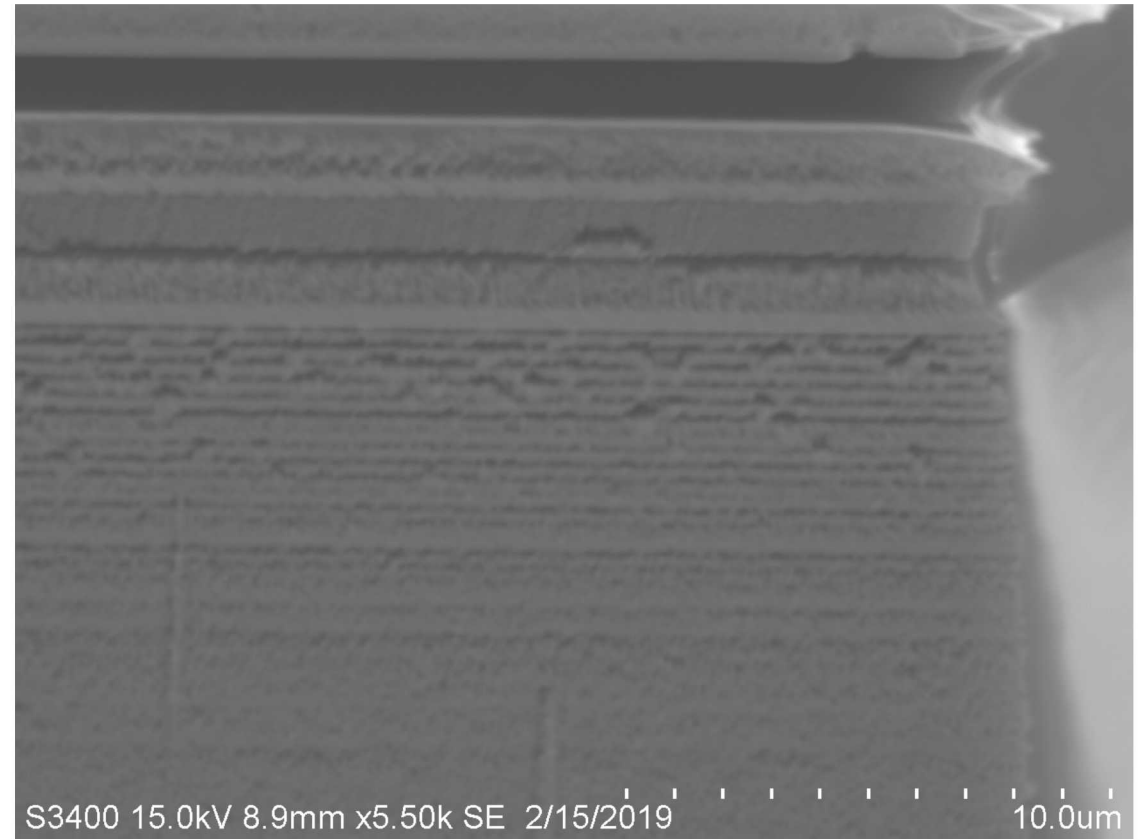
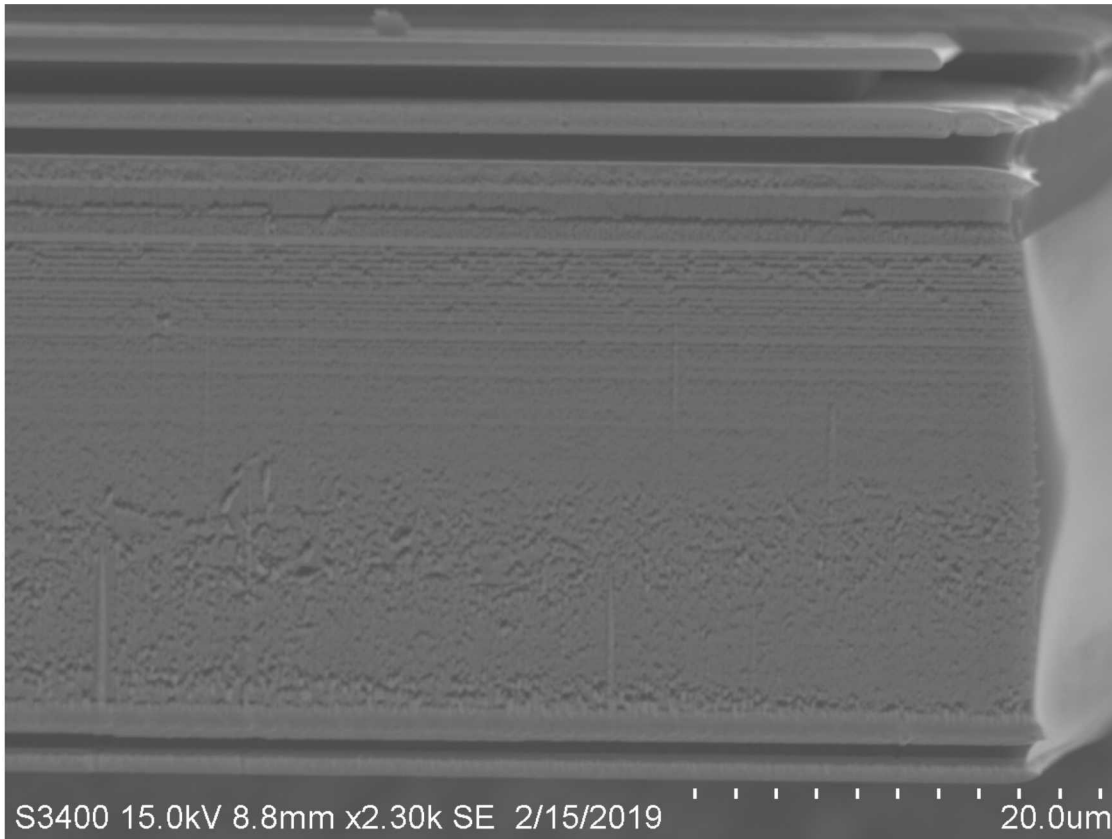
Green (after heating) shown with approximated power law

$$\dot{n} \propto f^{-7}$$



## Second look at sidewall coverage

Deep reactive-ion etching (DRIE) leads to undulated sidewalls

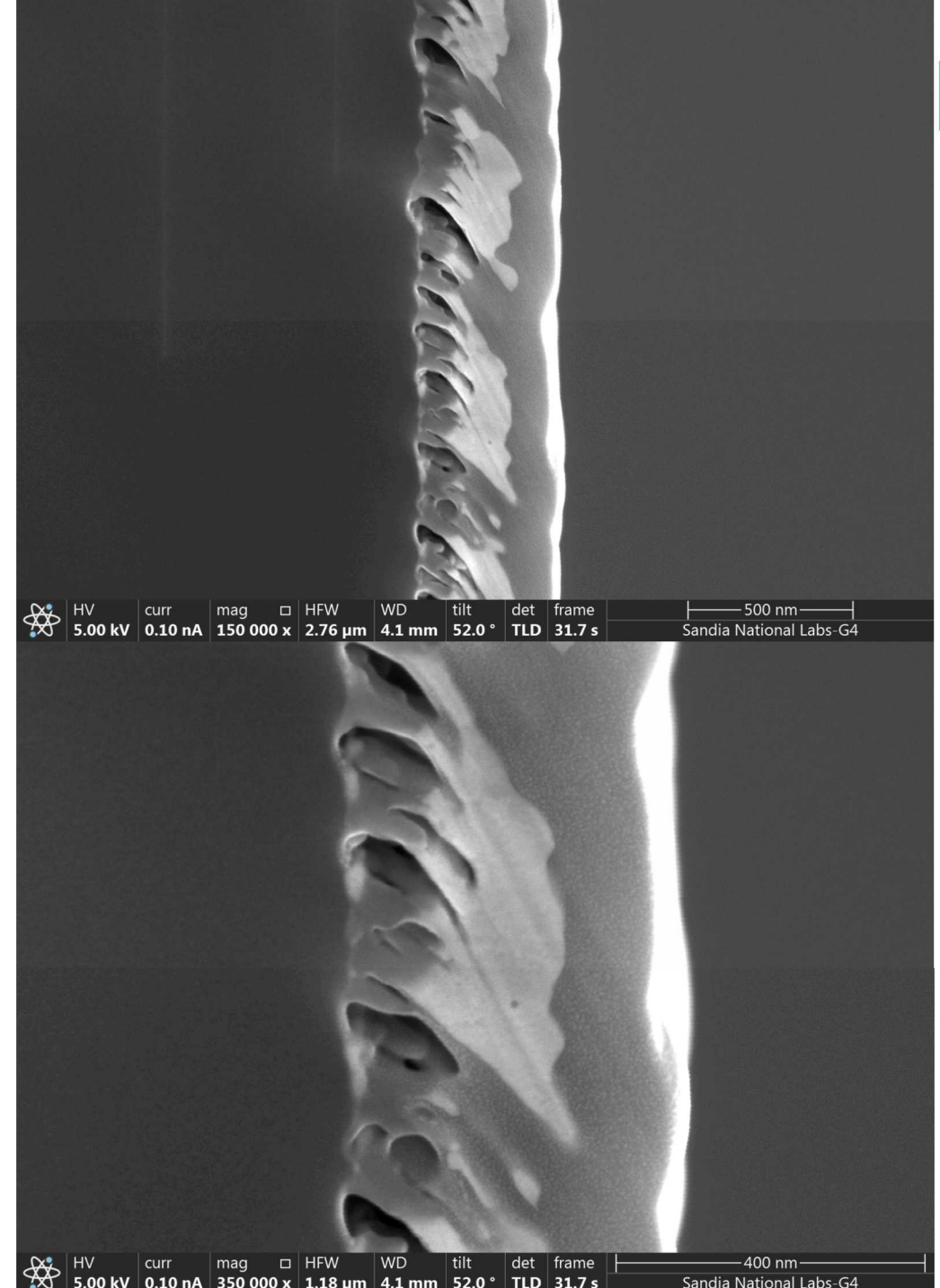
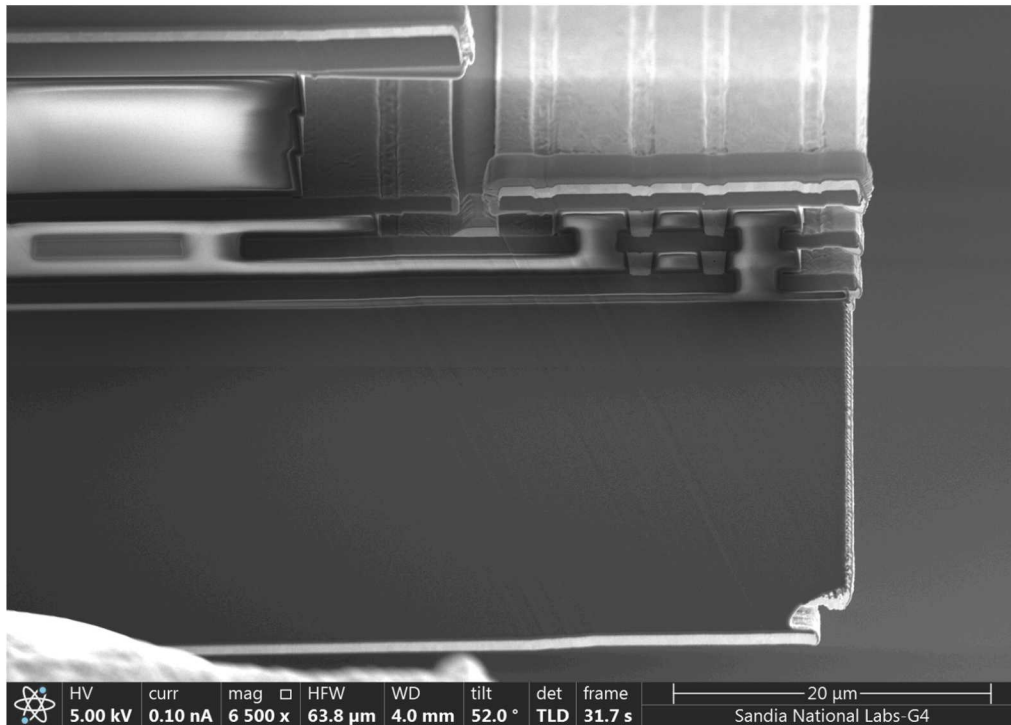


There might be exposed silicon that is susceptible to charging

# HOA-2.1 trap characterization

## Slot sidewall analysis:

- FIB cross-section profile imaging of Bosch etched slot feature in HOA 2.1 – Innsbruck
- Undulated sidewalls cause shadowing of Au evaporation resulting in voids in Au sidewall coverage



## Some interesting materials properties

- *Continuous* passivation of the Si slot sidewall using a metal silicide is suggested, e.g.  $\text{WSi}_2$

Metal	Work function (eV)
Be	4.98/5.0
Mg	3.66/3.68
Ca	2.51/2.87
Sr	2.59
Ba	2.52
Yb	2.6
Cd	4.07
Au	5.1
Al	4.06
W	4.55
Cu	4.48-5.1
Si	4.55 – 4.70
Stainless Steel	4.4

Metal Silicide	Work function (eV)
TiSi <sub>2</sub>	4.53
CoSi <sub>2</sub>	4.77
NiSi <sub>2</sub>	
MoSi <sub>2</sub>	4.82
Pd <sub>2</sub> Si	5
TaSi <sub>2</sub>	5.471
Pt <sub>2</sub> Si	5.17
ReSi <sub>2</sub>	
WSi <sub>2</sub>	4.62/4.88

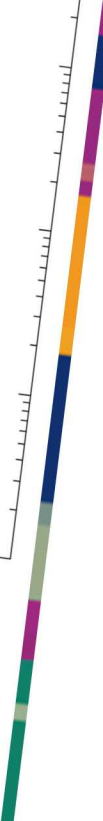
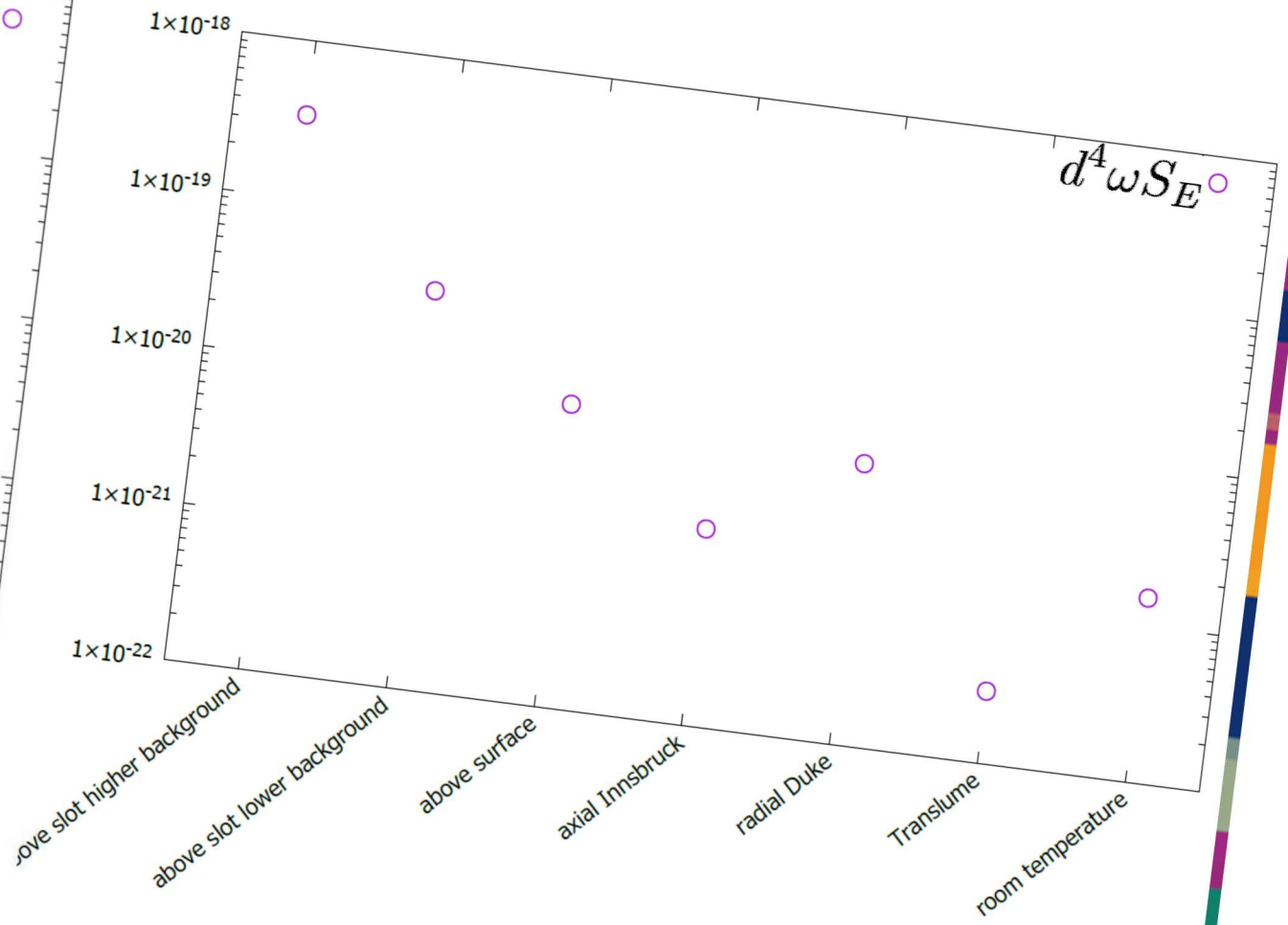
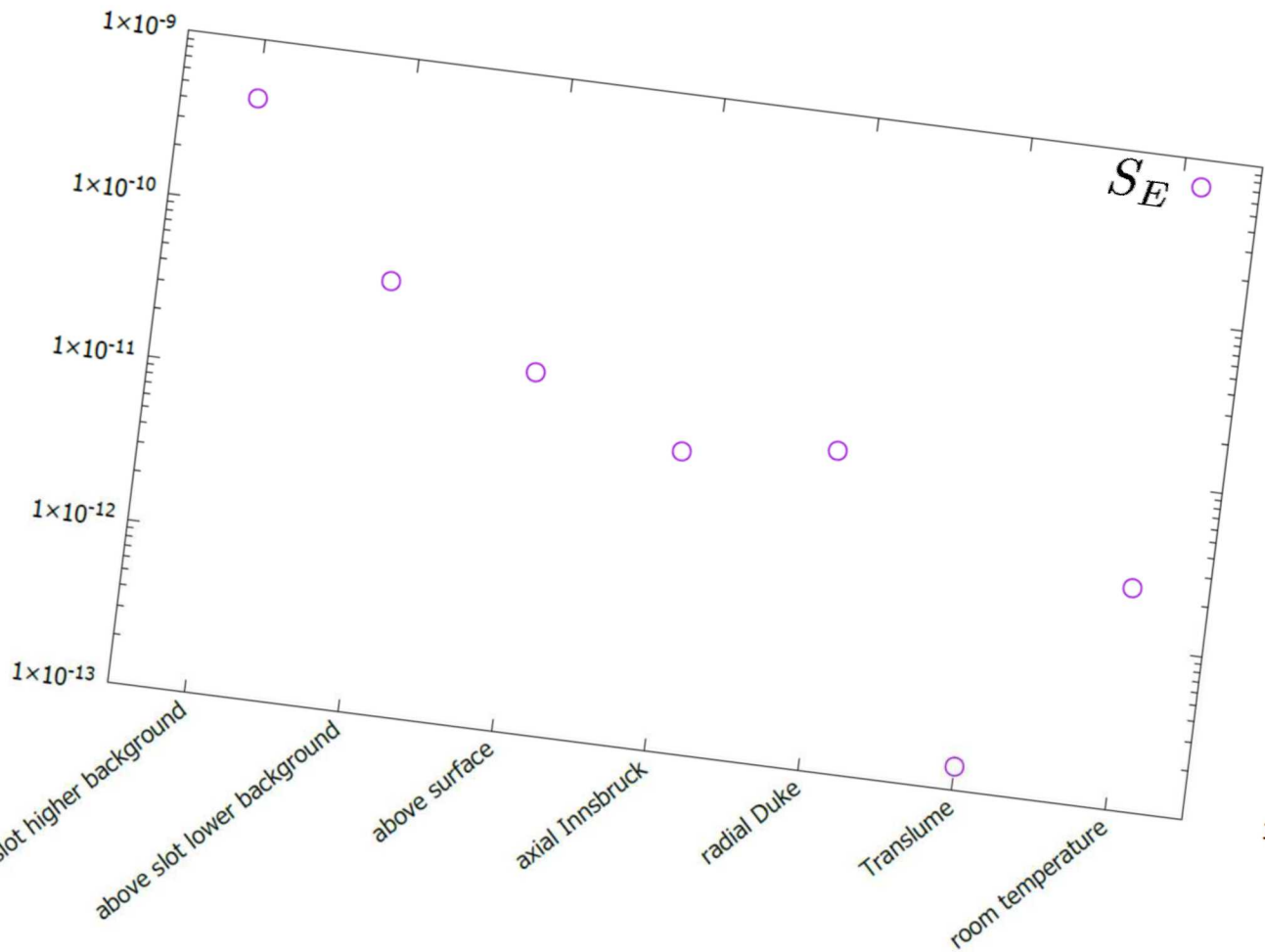
Wavelength	Energy (eV)
355 nm	3.5
370 nm	3.36

## Observed heating rates in cryogenic HOA-2.1 traps

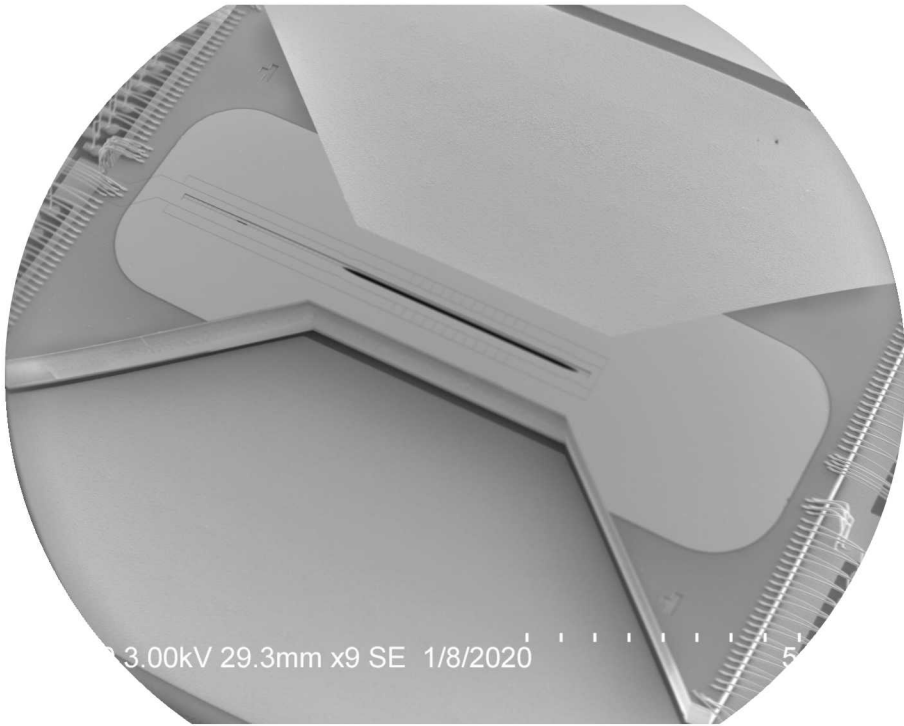
In contrast to observations in other traps, reduction of heating rates at cryogenic temperatures for HOA traps has not been observed.

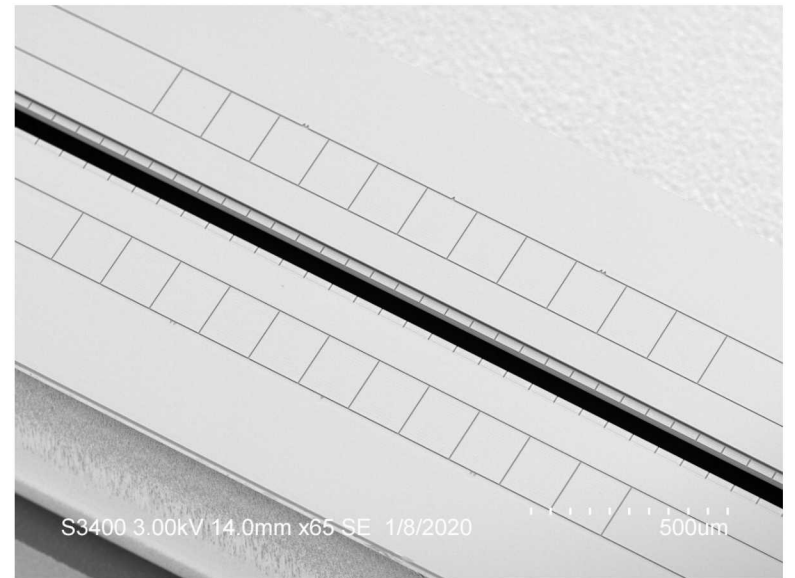
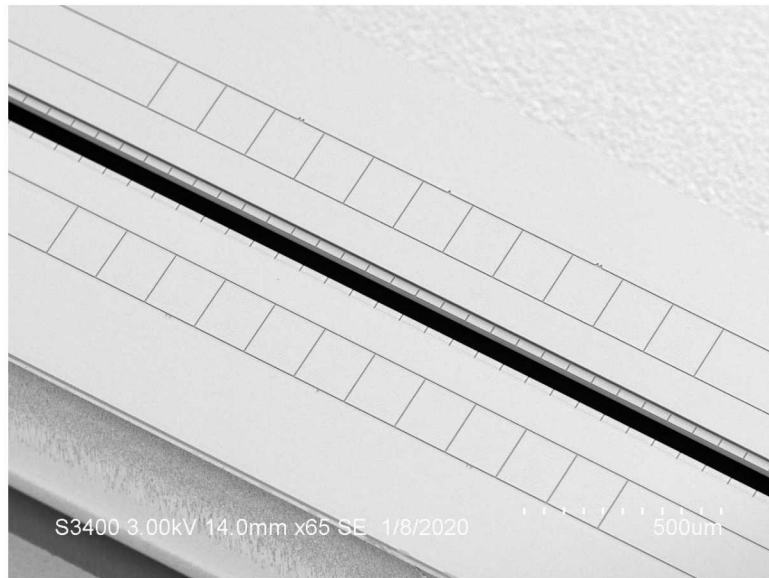
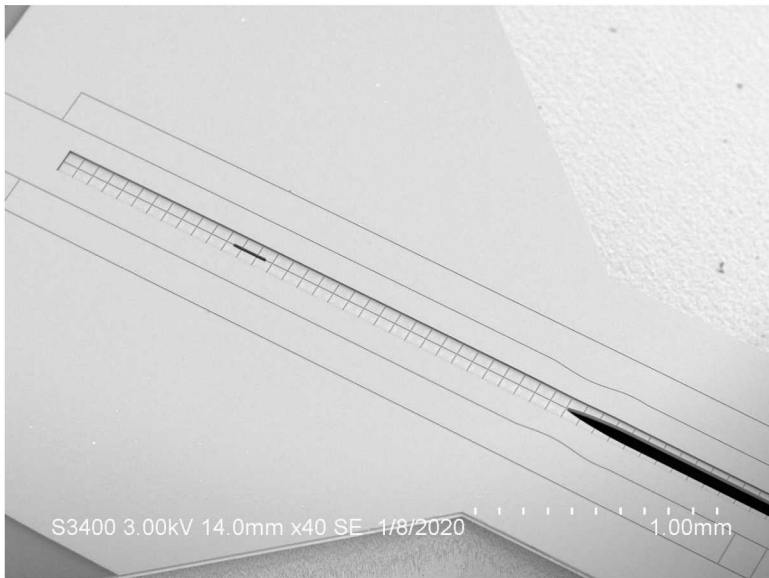
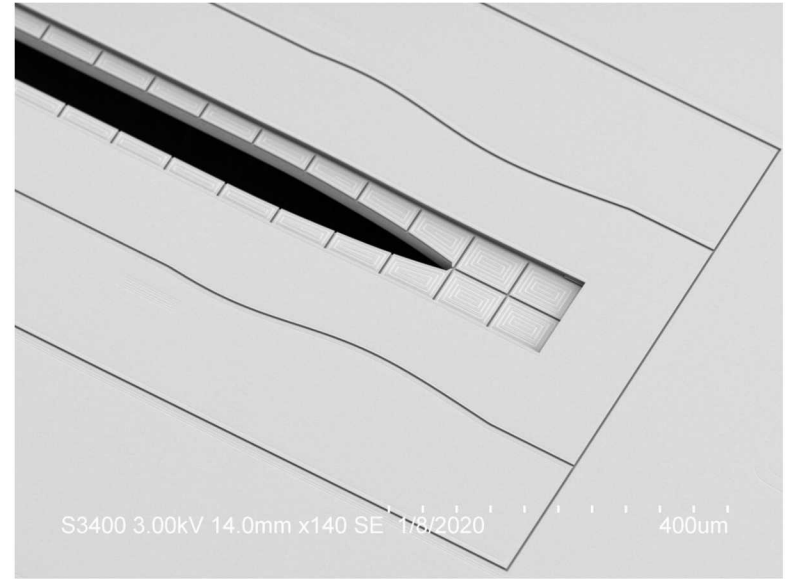
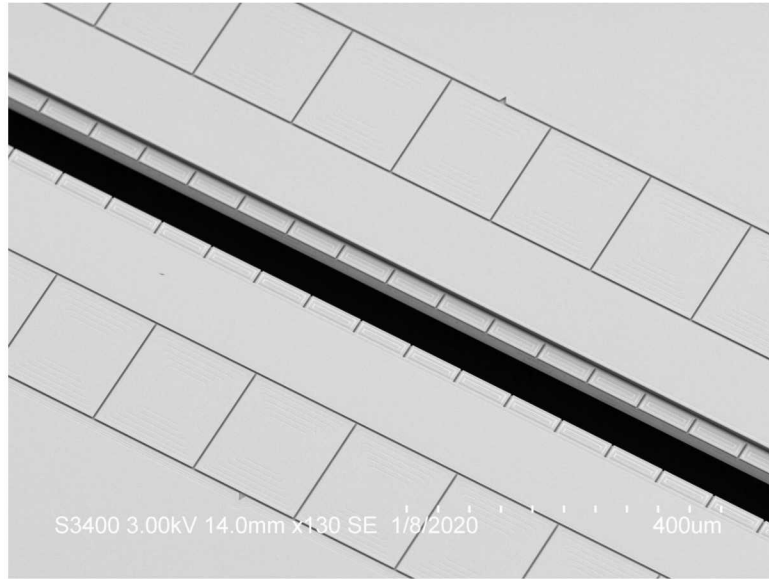
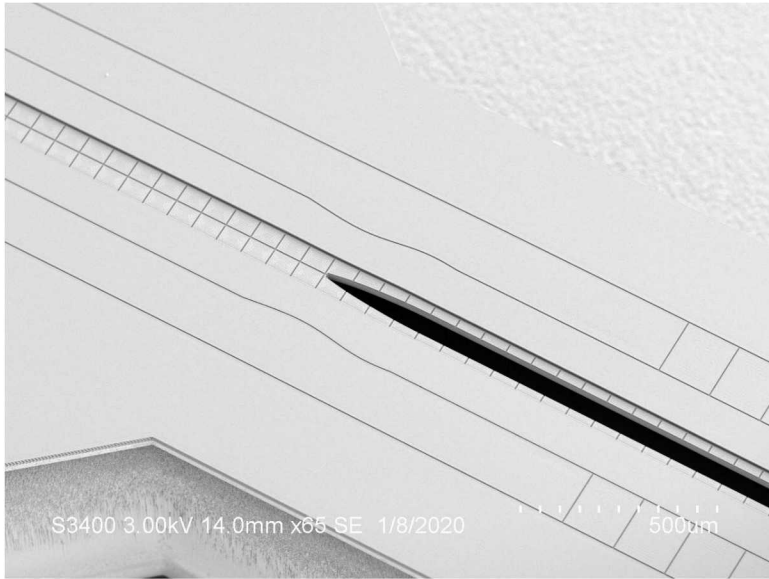
Institution	Trap	Ion	Temp	Mode	q	n_bar /s	S_E (V <sup>2</sup> *s/m <sup>2</sup> )	w S_E (V <sup>2</sup> /m <sup>2</sup> )	d <sup>4</sup> w S_E (V <sup>2</sup> *m <sup>2</sup> )	Ion metal distance	Comments
Sandia	HOA-2.0	Yb	300K	rad 2.6MHz	0.14	30	2.3e-12	3.8e-5	1.5e-21	80um	Above slot
UMD	HOA-2.1	Yb	300K	rad 2.6MHz		87					
Sandia	HOA-2.1	Yb	40K	rad 3MHz	0.17	5000	4.4e-10	8.3e-3	3.4e-19	80um	Above slot higher background pressure
Sandia	HOA-2.1	Yb	40K	rad 3MHz	0.17	500	4.4e-11	8.3e-4	3.4e-20	80um	Above slot lower background pressure
Sandia	HOA-2.1	Yb	40K	rad 2.1MHz	0.12	255	1.6e-11	2.1e-4	8.5e-21	80um	Above surface
Innsbruck	HOA-2.1	Ca	cryo?	ax 1MHz	0.31	1000	6.9e-12	4.3e-5	1.8e-21	80um	
Duke	HOA-2.1	Yb	cryo	rad 2.6MHz	0.15	120	9.2e-12	1.5e-4	6.2e-21	80um	
Innsbruck	Translu me	Ca	cryo	ax 1MHz		20	1.4e-13	8.7e-7	2.9e-22	135um	

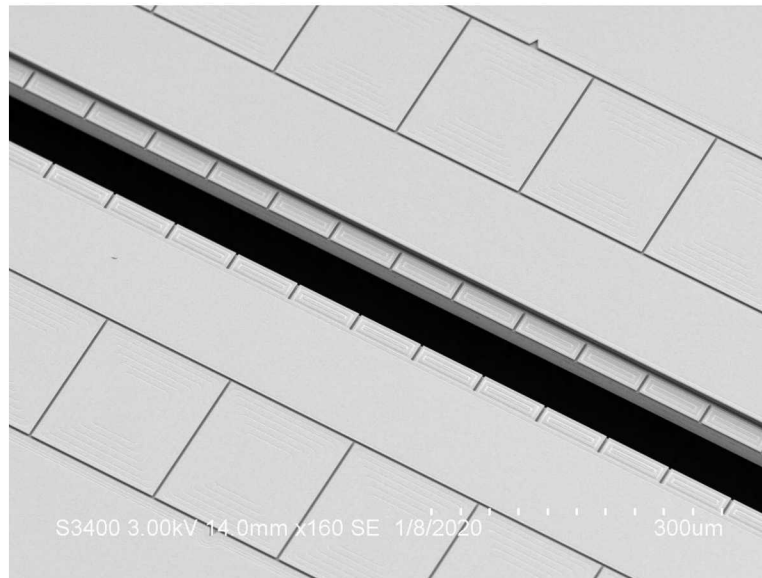
# Heating rate summary



# Phoenix trap







# Phoenix Packaging

## Solder Die Attach

- Removes all packaging organics from chamber
- Solder spheres laser solder “jetted” onto package surface
- Smaller solder spheres are an option
- Spheres auto-center on pads after reflow process
- To be done: shear testing, LN2 dunk and shear tests
- Smaller solder spheres and populate every pad

