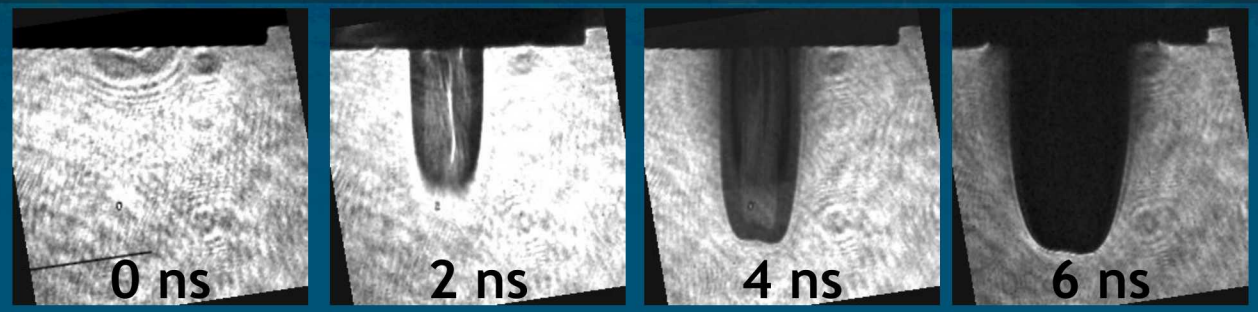
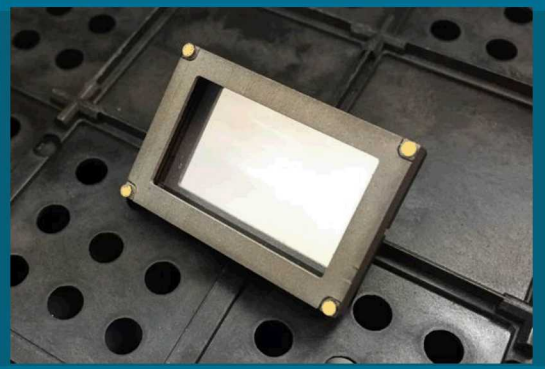
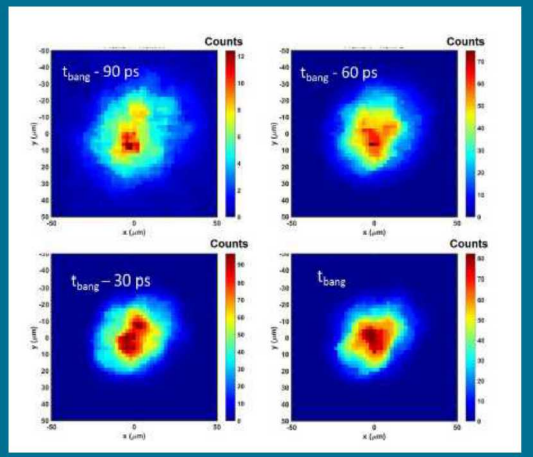
On the future of hCMOS







PRESENTED BY

Liam D. Claus, 12/05/2018

SAND2018-13489PE

SAND2018-10802 PE

hCMOS schedule

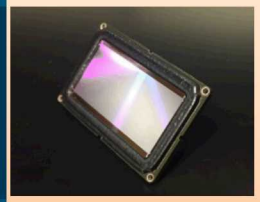
We are continuing to drive new hCMOS sensor technology with an emphasis on more frames and faster integration time

FY15	FY16	FY17	FY18	FY19	FY20	FY21	FY22
Hippogriff	Icarus V1		Icarus V2	Daedalus		Daedalus HE	Horus
Delivered	*Delivered*		*Delivered*				

Furi / Hippogriff

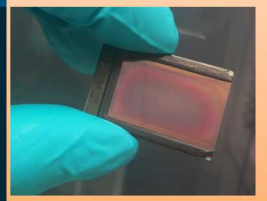
- 1st full-scale multi-frame sensors
- 1.5-2ns minimum shutter
- Optimized for 1-10 keV x-ray detection

IcarusV1/ IcarusV2



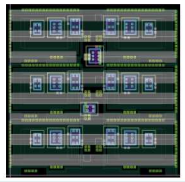
- 1st cameras compatible with pulse-dilation
- 1 ns min. shutter with 2 or 4 (Icarus-2) frames per hemisphere
- Optimized for soft x-ray, visible, and e- detection

Daedalus/ Daedalus HE



- 3 frames per hemisphere (≥6 frames with interlacing)
- 1-side abuttment for spectroscopy and z-pinch imaging applications
- Large well for high energy x-rays while maintaining low end sensitivity
- **GaAs/Ge detector**

Horus



- 1st sensor in new foundry process

  Design goals include

  - 6 frames per pixel w/ independent quadrants (≥12 frames with interlacing)
  - 0.5 ns minimum shutter

UXI Sensors

hCMOS status

Icarus has been well characterized and is being fielded across multiple diagnostics, all fabricated wafers will soon be hybridized and packaged

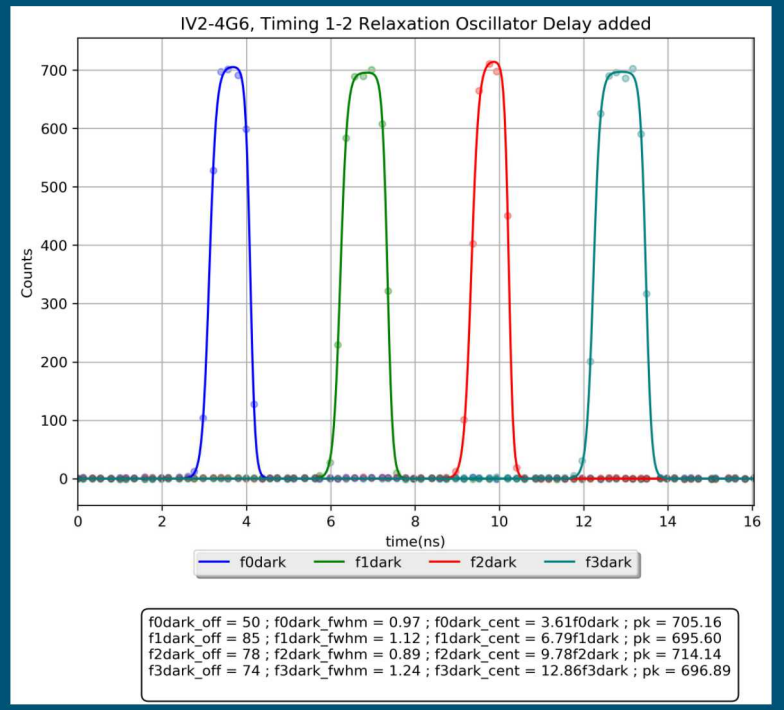
Hybridization supply chain issues have been resolved

- nHanced Semiconductor has delivered functional DBI hybridized devices
- SNL has delivered functional indium hybridized devices

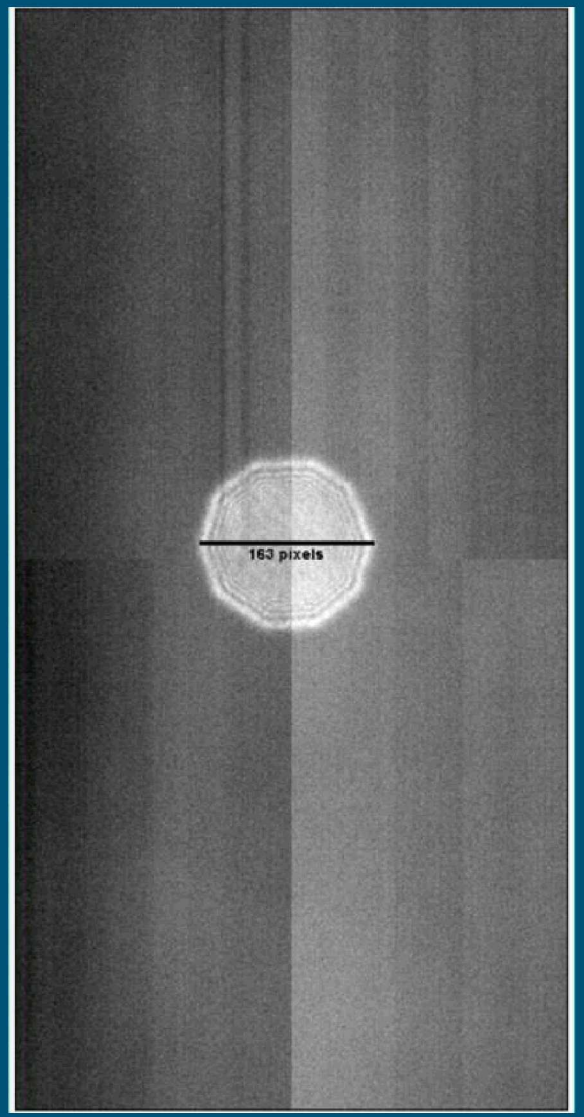
Icarus-V2 with four frames per pixel are available and performing as expected

- All 6” wafers in stock will be bonded and packaged (9 wafers are in bonding)
- ~160 additional devices are expected

LLNL and Z Machine continue to obtain extensive characterization data



1 ns timing shutter profile, aperture exposing ~4 % of the array, 5.6% full well illumination, 8 µm thick photodiode



Aperture shutter profile

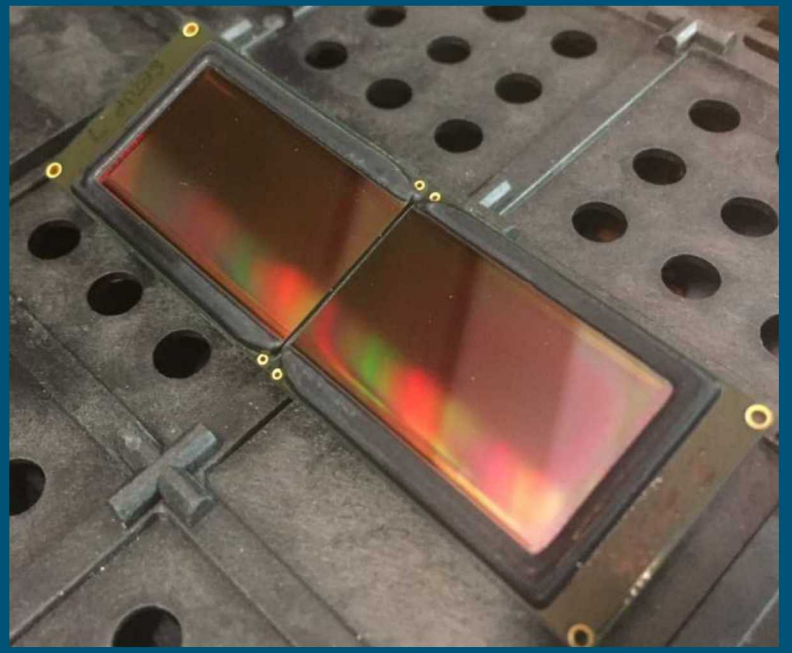
Daedalus has been tested electrically and is fully functional while the first hybrids are approaching completion

Bare ROIC has been successfully packaged and tested
- The package has been iterated to fix an issue found and is in house

Epoxy underfill issues have delayed indium-bonding, but possible solution in the works
- Detector die will be cut smaller to allow for additional room for under-fill at the expense of the corner diode diagnostic

6 wafers are undergoing DBI bonding with nHanced Semiconductor
- LLNL funded
- First DBI-bonded units expected Q2, FY19

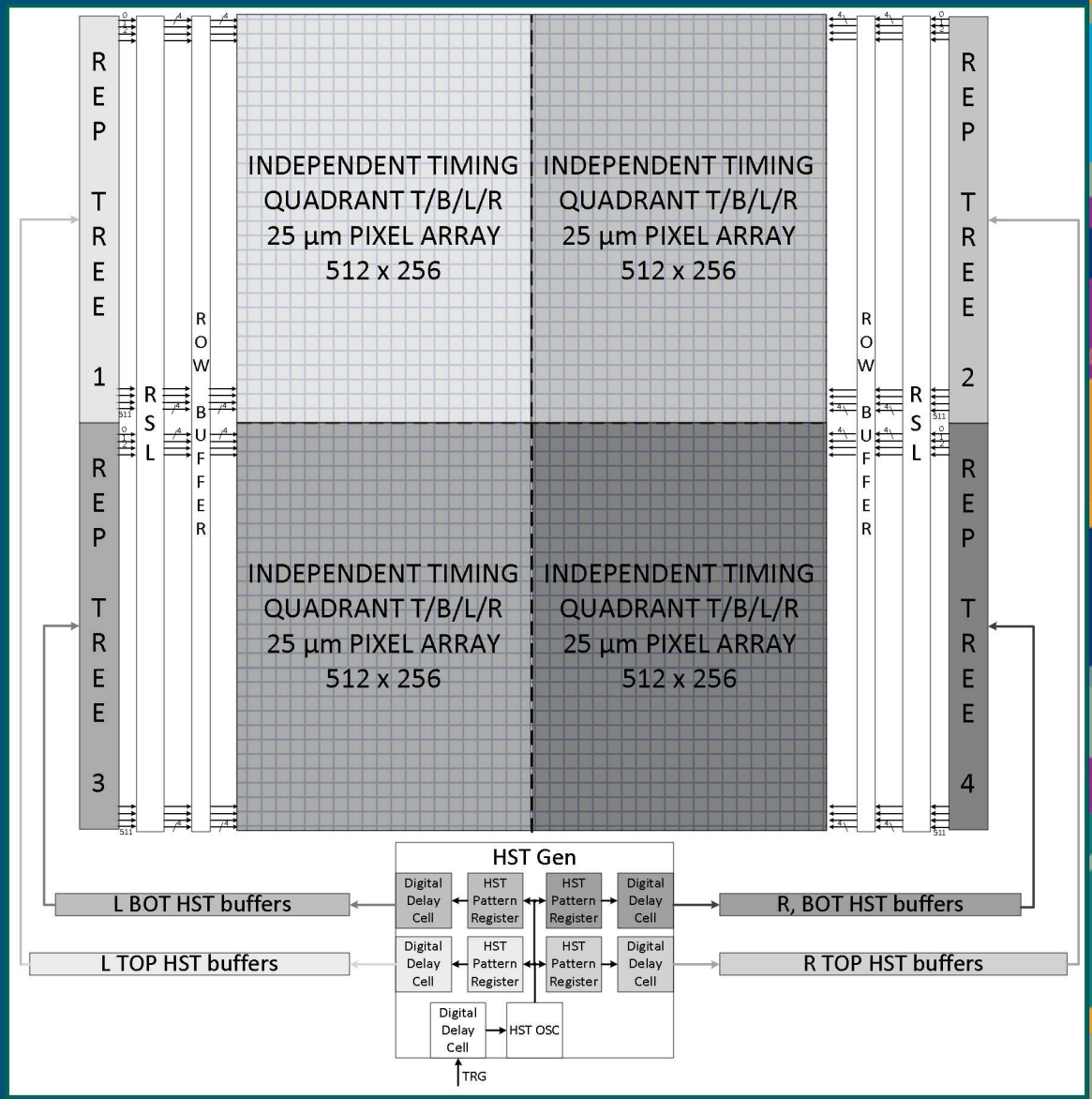
Daedalus specs
- 3 frames per pixel + interlacing options
- 512x1024, 25 μm pixels
- 1-side abuttable
- 1.5M e^- full well (4 M e^- for a single frame)
- 1 ns minimum gate width (design goal)



Two packaged Daedalus ROICS abutted
Active array size: 12.8 mm x 51.2 mm

Horus is the proposed next generation UXI sensor but will require an intermediate step to realize these performance improvements

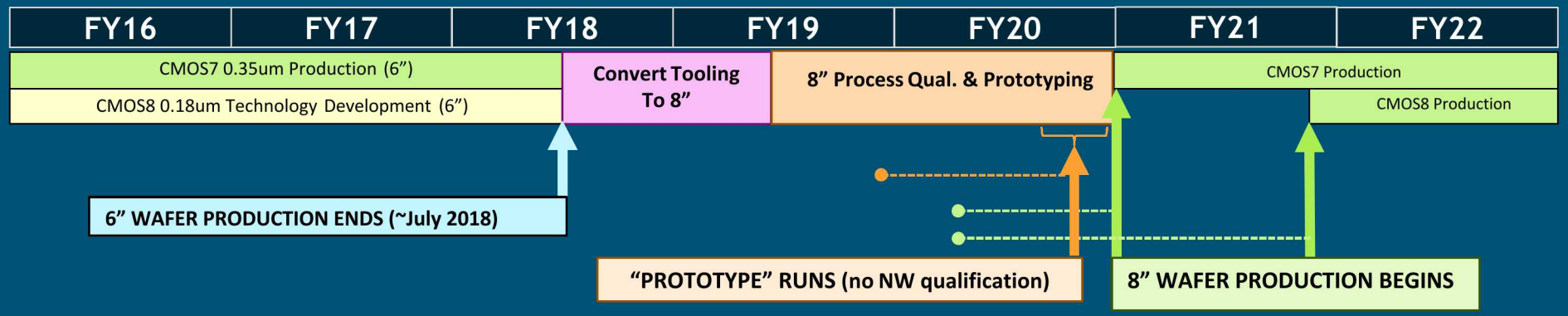
- 1024 x 512 pixel array
  - 25.6 x 12.8 mm active area
- 25 µm pixel
- 6 frames
- 500 ps Integration time
- 500 ke^- full well
- 200-500 e^- noise floor
- Independently timed and tuned quadrants
- 1 side abutable
- ZDT + interlacing



Sisyphus provided an early test of the CMOS8 process, but we now have concerns about the process maturity and timeline

- Sisyphus has been fabricated
  - First CMOS8 lot has a number of issues
    - Gate poly CMP issue caused significant transistor fall out
  - Testing is ongoing, but so far we have been unsuccessful applying power to the ROIC
    - High Idd leakage has been observed on other ICs fabricated on this lot
      - Requires operating parts at 0.9V
  - Unit blocks broken out as individual components will be tested next

Requirement	Sisyphus	Holy Grail
Array size	**256 x 256**	1024 x 512
Pixel size	**25 µm**	25 - 40 µm
Number of frames	**4**	6 - 24
Min integration time	**0.25 - 0.5 ns**	250 - 300 ps
Min inter-frame time	**0.25 - 0.5 ns**	250 - 300 ps
Timing skew	**< 10%**	< 10%
Gain errors	**< 10%**	< 10%
Full well	**500 ke$^-$**	5 M e$^-$
Noise floor	**500 e$^-$**	250 e$^-$
Dynamic range	**60 dB (10 bit)**	> 60 dB (11 bit)
Abutable?	~~**1 side**~~	2 side



What might be possible if we stay in CMOS7?

Iterate Icarus and/or Daedalus for minor improvements
- Considered low risk
- These sensors are used in many applications that may appreciate an incremental improvement

Integrate high-K-dielectric, MIM caps to enable a 4-frame Icarus like sensor with full well approaching Daedalus or possibly even higher
- Considered low risk
- Reasonable cost and timeline for integration to CMOS7b

CMOS8 metal stack on established CMOS7b transistors
- Reduces risk of going strictly to CMOS8
- *Possibly* enable 6 frames
- *Possibly* enables integration times below 750 ps
- Significant development cost needs to be established
- Requires fab commitment
  - Cost and schedule could be significant

Requirement	Holy Grail
Array size	1024 x 512
Pixel size	25 - 40 µm
Number of frames	6 - 24
Min integration time	250 - 300 ps
Min inter-frame time	250 - 300 ps
Timing skew	< 10%
Gain errors	< 10%
Full well	5 M e^-
Noise floor	250 e^-
Dynamic range	> 60 dB (11 bit)
Abutable	2 side

What will be needed to drive improvements to UXI sensors?

Primary program needs are more frames, ~500 ps integration time and higher full well

Integration time with 4 frames is close to achieving 750-500 ps
- Daedalus fastest integration time needs to be identified

1.5 Me^- and 4 frames is achievable in CMOS7 with reasonable effort
- High K MIM's in CMOS7 enable this

5 Me^- full well requires a more significant effort
- Current mode pixel design

More than 4-6 frames with the existing architecture and pixel pitch is difficult
- Requires a new timing distribution architecture
  - In-pixel (pixel cluster) timing
  - Improved transistor density
  - > 5 metals

Requirement	Holy Grail
Array size	1024 x 512
Pixel size	25 - 40 µm
Number of frames	6 - 24
Min integration time	250 - 300 ps
Min inter-frame time	250 - 300 ps
Timing skew	< 10%
Gain errors	< 10%
Full well	5 M e^-
Noise floor	250 e^-
Dynamic range	> 60 dB (11 bit)
Abutable	2 side

Jazz 130nm process node may be a good alternative to Sandia CMOS8

Positives

- Mature commercial process with well-established design rules
- ‘Reasonable’ cost and schedule for dedicated lots
- Higher transistor density to enable more frames per pixel
- MIM caps with higher capacitive density than CMOS7 or CMOS8
- Non-sensitive process may enable easier technology transfer

Negatives

- Top metal design rules won’t accommodate present architecture driving all shutters from the edge of the array
  - Need to migrate to in-pixel timing to enable > 4 frames in present pixel pitch
- Maximum reticle size is smaller than CMOS8
  - Requires shrinking the sensor active area in the long dimension below the size of Icarus and Daedalus
- Design team has limited experience in this process node
- Radiation hardness may be less than CMOS8

Jazz 180nm may also be an option – cost is $160k less per dedicated lot than 130nm with similar fabrication time

- 130nm provides greater transistor density, faster speed, and an additional metal layer for future sensor designs
- Evaluation will be done on trade-offs between 130nm and 180nm

The proposed 'Icalus' ROIC design concept enables 3 pixels for evaluation while incurring the cost of a single diode/hybridization run

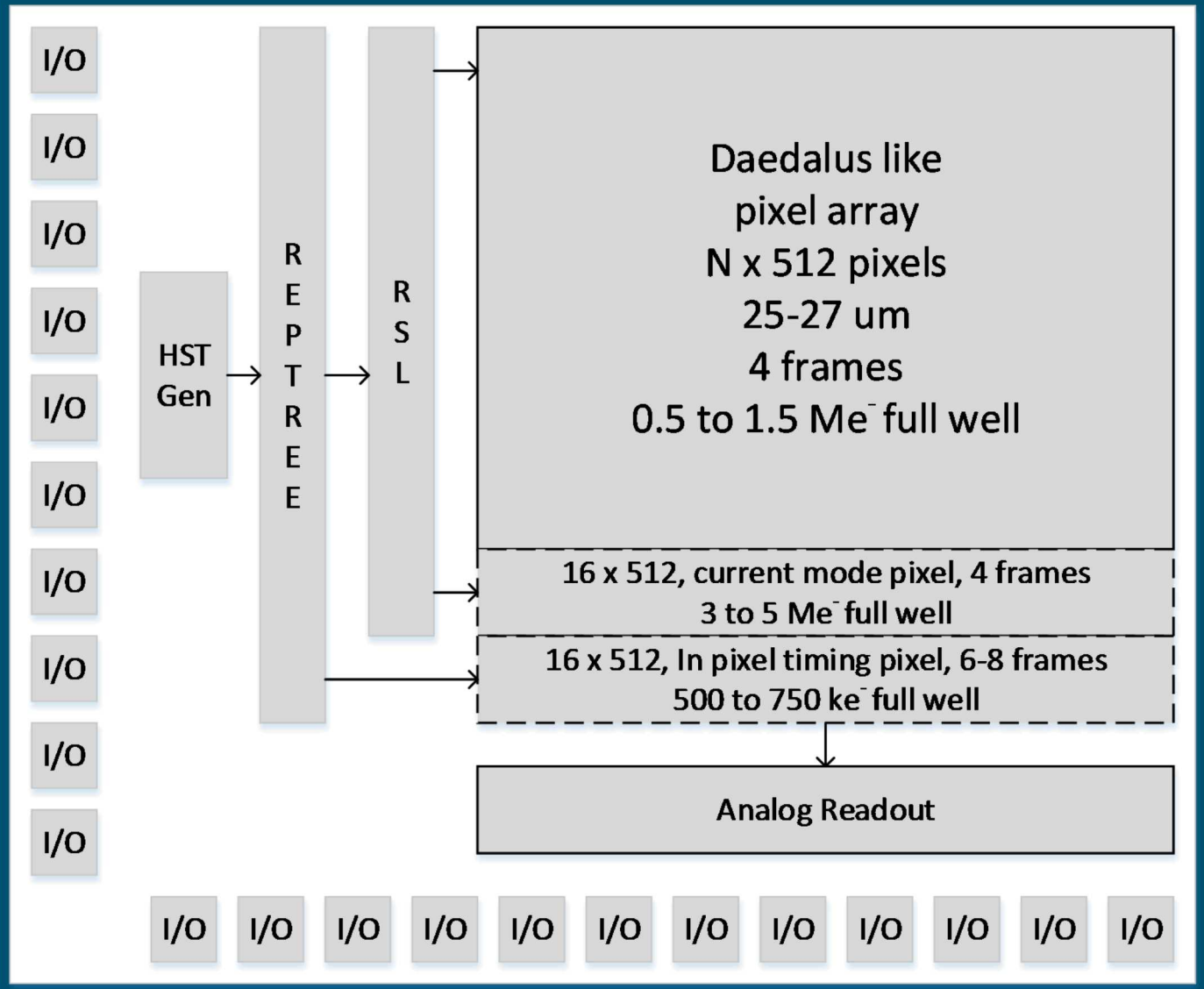
Pixel array of Icarus/Daedalus like pixels allow us to baseline the process against the known performance of the existing CMOS7 sensors

Goal will be two side abutable
- Needs further evaluation

Maximum pixel array size with a 25 µm pixel pitch is projected to be ~840-900 x 512

Test pixel banks leverage support circuitry needed for any design

Pixel design priority will be
1. Icarus/Daedalus like
2. In-pixel timing, 6-8 frames
3. Current mode, HFW



A decision matrix helps understand the most logical path forward

	Horus CMOS8	Horus Jazz 130 nm	"Daedalus like" Jazz 130 nm	Daedalus like CMOS7	
Frames	6	6	4	4	6
Architecture	Daedalus like	In-pixel timing	Daedalus like	HFW	HFW
Pixel Pitch	25	25	27	25	35
Full Well	0.5 Me^-	>0.5 Me^-	0.5-1 Me^-	3-5 Me^-	2-3 Me^-
Array Size	1024 x 512	~900 x 512	~840 x 512	1024 x 512	1024 x 512
Process Maturity	Low	High	High	Med	
First possible tape out	Q1, FY21	Now	Now	Q2, FY20	
Cost/spin	$750k	$460k	$460k	$360k	
Fab time	8-12 months	4-6 months		6-8 months	
First functional unit (2 spins)	FY24	FY22	FY22	FY23	
Total cost	$$$$	$$$	$$$	$$$	

Recommended path forward

Step 1: Design and produce a 4-frame “Daedalus-like” sensor with a test bank of in-pixel timing, 6-frame pixels

- **Delivered Q4 FY20**
- Allows process development for 8” wafer hybridization which is needed for any future sensors
- Baselines the TowerJazz process with a sensor implementing the existing architecture in a pixel array large enough to provide useful data to the community

Step 2:

If step 1 is successful, implement a full array of 6-frame, in-pixel-timing pixels

- **Delivered Q3/4 FY22**

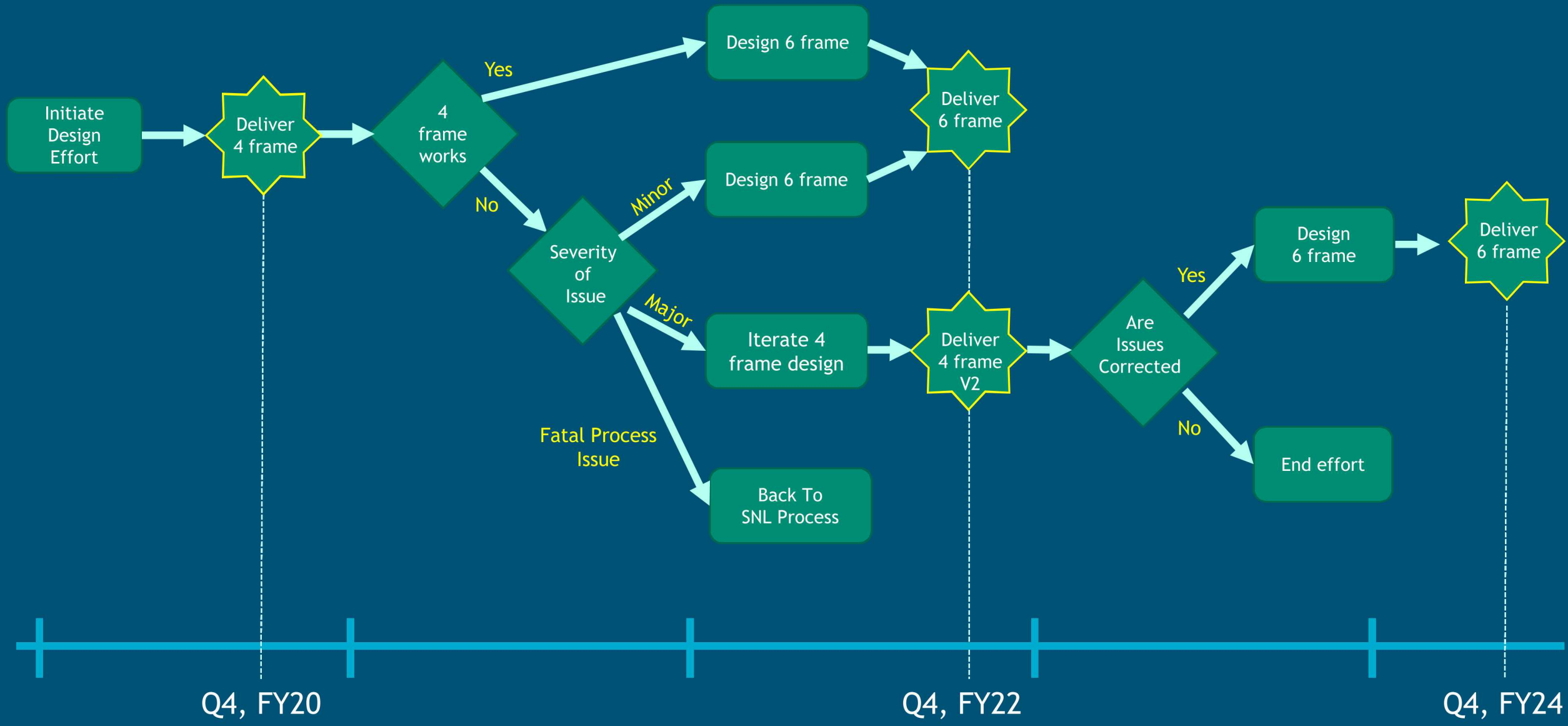
If step 1 is unsuccessful, step 2 depends on the failure

- Minor issues will be resolved and 6-frame, in-pixel timing will still be pursued
- Significant issues will require a re-spin emphasizing the 4-frame pixel
  - Delivering 4-frame arrays **Q3/4 FY22** and 6-frame arrays **Q4 FY24**

CMOS7b will be used to produce additional Icarus and Daedalus sensors as needed

- Soonest units available: Q2/3 FY21

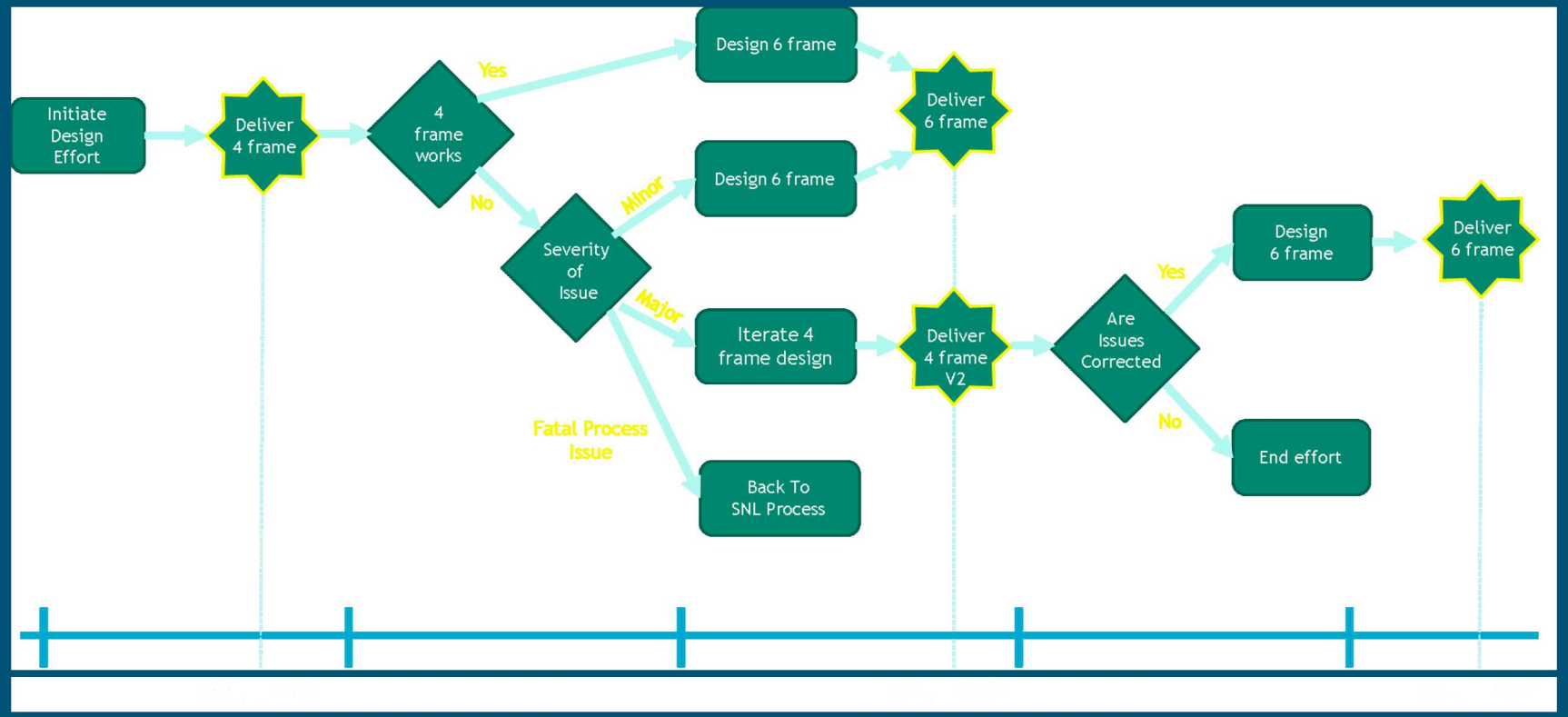
Decision tree for proposed ROIC development plan



Summary

Earliest possible date for 6-frame sensor is Q3/4 FY22

- This plan assumes a reasonable risk with in-pixel timing development while still providing a useful capability to the community with a 4-frame Daedalus-like pixel array



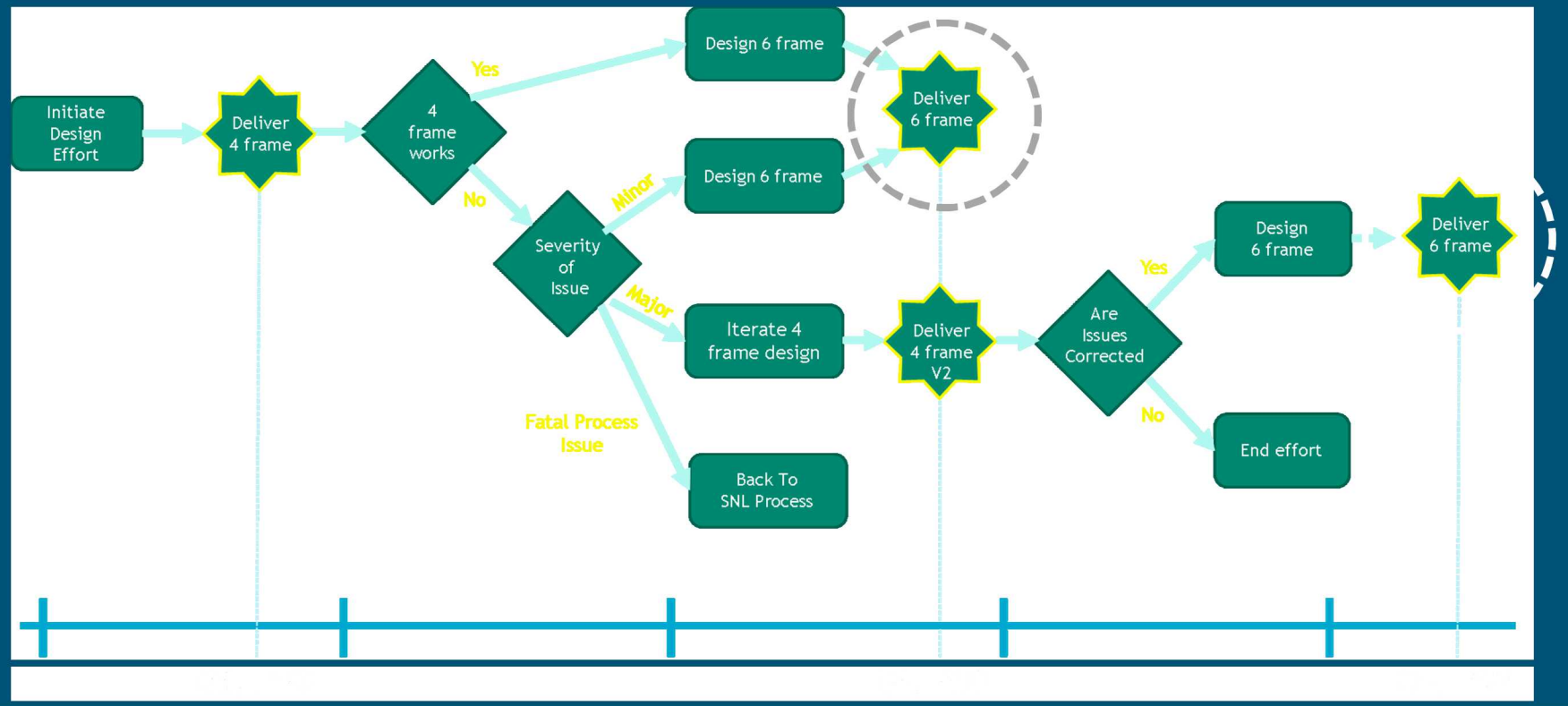
Summary

Earliest possible date for 6-frame sensor is Q3/4 FY22

- This plan assumes a reasonable risk with in-pixel timing development while still providing a useful capability to the community with a 4-frame Daedalus-like pixel array

Worst case delivery for 6-frame sensor is Q3/4 FY24

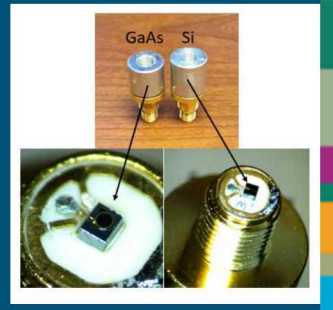
- While still providing useful Daedalus like sensors and learning for the design team



High Energy X-ray detection

GaAs detector development at Sandia

Non-silicon materials such as GaAs or Ge have the potential of adding significant sensitivity at X-ray energies up to 20 keV while maintaining similar temporal performance



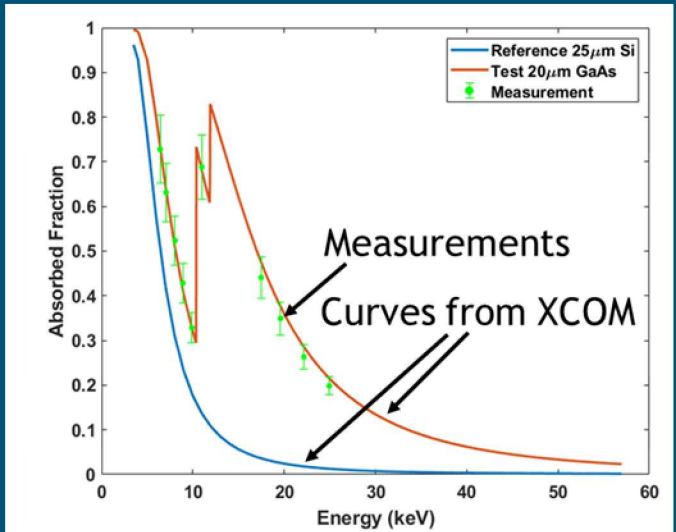
Internally funded Laboratory Directed Research and Development (LDRD) program from FY17 to FY18 provided a significant jump start on the development of pixelated arrays

- Demonstrated the ability to successfully grow high purity, thick GaAs via MBE
- Demonstrated discrete detector performance with GaAs and CdTe

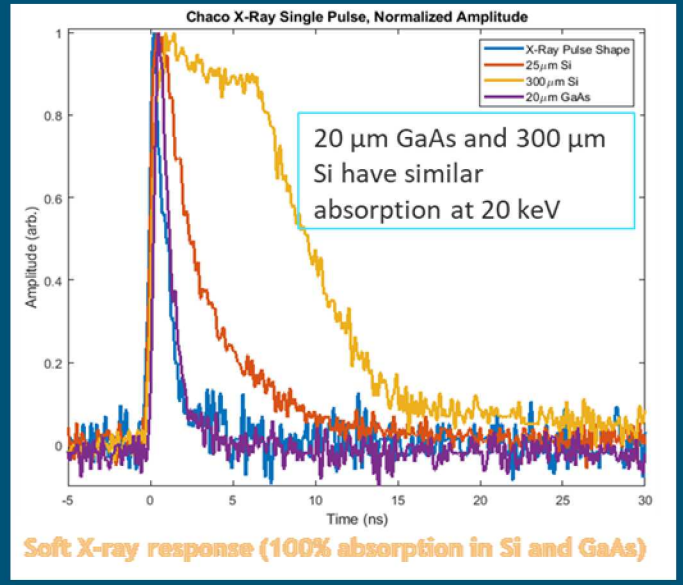
Measured response of SNL GaAs discrete diodes show very good temporal response

X-ray absorption matches prediction models

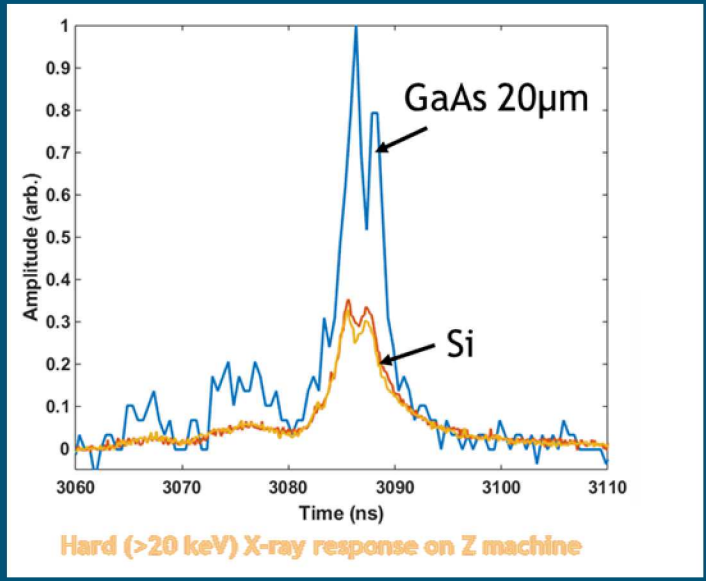
- 20 µm thick discrete GaAs diodes show better temporal response than Si reference



Test data demonstrating greater absorption in 20 µm thick GaAs detectors



Soft X-ray response (100% absorption in Si and GaAs)



Hard (>20 keV) X-ray response on Z machine

GaAs detector development is a priority for hCMOS development in FY19 and beyond

Goals for FY19:

- Design, build, and test a ~3 x 3 and ~36 x 36 pixelated back side illuminated GaAs array at a thickness of 20-40 μm
- Demonstrate bonding of these small pixelated arrays to a fanout wafer
- Design a 0.5 Mpixel GaAs array for bonding to Daedalus

Goals for FY20:

- Build and test a 0.5 Mpixel GaAs array bonded to Daedalus
- Design a High Energy ROIC and/or diode array with charge handling capabilities for photon energies up to ~40 keV

Goals for FY21:

- Deliver GaAs-Daedalus sensors for use on Z and NIF

Goals for FY22:

- Build and test a High Energy UXI ROIC and/or diode array for photon energies up to ~40 keV

Ge detector development at LLNL

LLNL LDRD has been approved and a process development plan is established

Ge P-i-N Photodiode

AP-CVD epitaxy
- Single pass, 50 µm feasible
- Three pass, up to 150 µm possible with development

Ge substrates

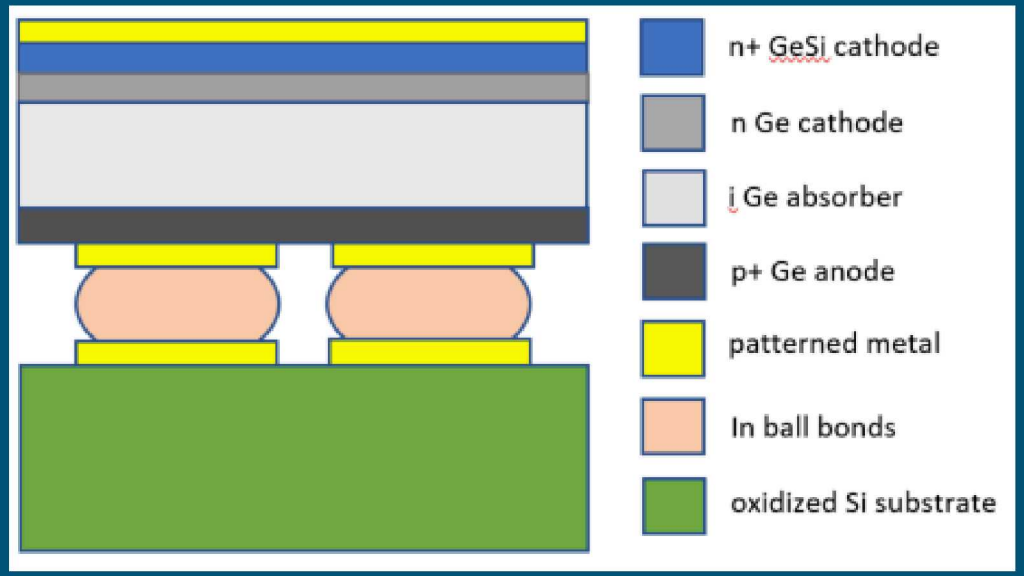
in-situ doped anodes, cathodes

Graded SiGe heterojunctions to inhibit dark current

Backside illuminated

Common-cathode photodiode arrays

Hybridization of the array utilizes indium bump bonding



Two In bump bonded Photodiodes

Ge detector development is a funded LDRD at LLNL

Goals for FY19:

- Single diodes
  - Complete detailed design and simulation
  - Fabricate single diode test devices, with different active-layer thicknesses, both with and without Ge1-xSix buffer layers

Goals for FY20:

- Small arrays
  - Fabricate diode arrays (2x2, 4x4, 10x10)
  - Initiate X-ray imaging testing with arrays

Goals for FY21:

- More complex designs
  - Fabricate PDs with graded i-regions AND heterojunctions
  - Compare results with 100 μm Si and current GaAs efforts at SNL

Goals for follow on work:

- Exit Plan
  - Conceptual and detail design of Ge PD array for hybridization to a CMOS ROIC
  - Fabricate large-scale Ge PD arrays to compliment Si Daedalus
  - Integrate this technology into the National Diagnostics Plan

High fluence mitigation-Pixel concerns

There is an internal effort to increase capacitive density by up to 15x

Improved capacitive density

- In-house programs to develop High-K dielectric MIMs
  - Demonstrated 3x improvement in density
  - There is a low risk path to 7x increase in C/μm^2
- In-house program to develop vertical trench capacitors
  - Consume active Si rather than metal layers as MIM caps do
  - Potential to use as in-pixel replacement current bypass caps or as storage caps
  - Initial trench etch experiments have been successfully conducted

Dielectric	Measured Capacitance per Area improvement
Alumina (10 nm)	5.81228
Alumina (15 nm)	3.79993
Alumina (20 nm)	2.78762
Alumina (5 nm)	16.34090
PECVD Si_3N_4	1.00000

C7 MIM caps demonstrated

Dielectric	Predicted Capacitance per Area improvement
Hafnia (10 nm)	15.11192
Hafnia (15 nm)	9.87982
Hafnia (20 nm)	7.24781
Hafnia (5 nm)	42.86434
PECVD Si_3N_4	1.00000

C7 MIM caps demonstrated projected

M. Suzuki *et al.*

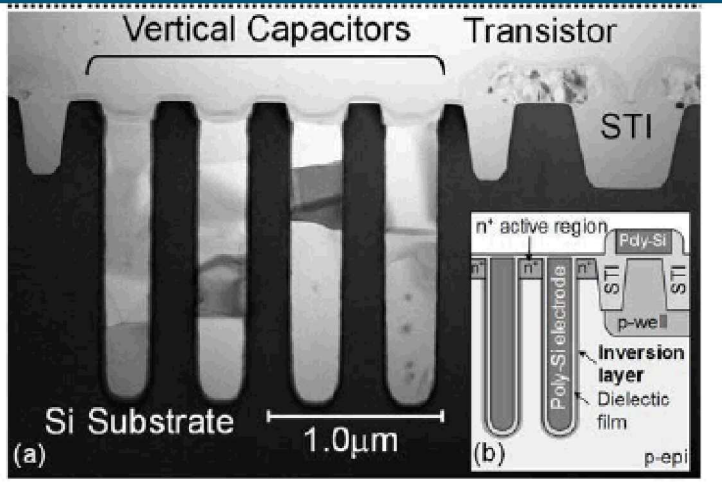


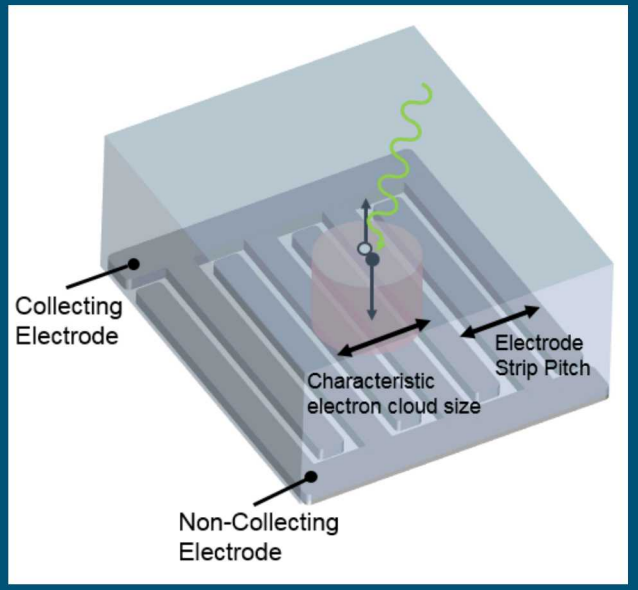
Fig. 6. Cross sectional (a) TEM view and (b) schematic illustration of vertical analog memory.

Vertical trench caps in the literature

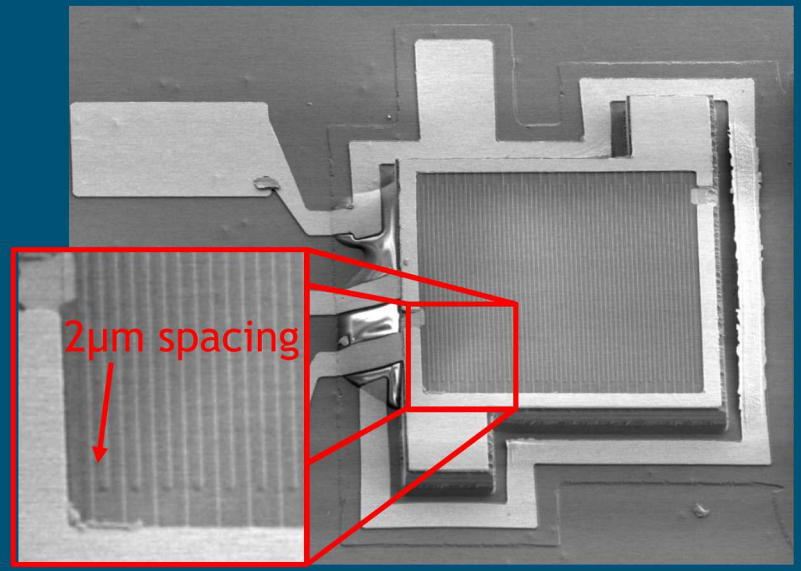
A partial solution exists without need for ROIC modification

Readout electrode current splitting

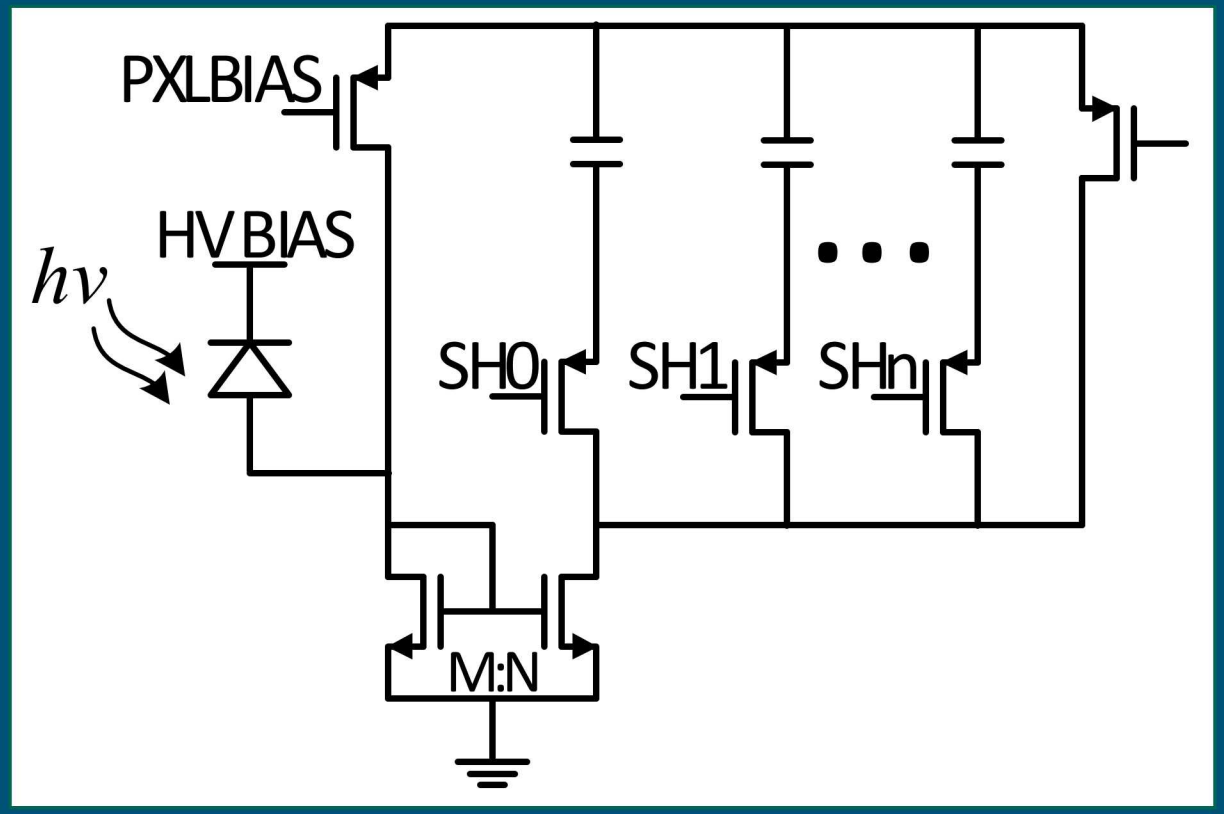
- Need ~5x signal reduction to keep present 1000:1 dynamic range at 30 keV
- Can use second electrode on detector to shunt charge, reduce observed signal
- Key is to keep overall structure size smaller than single photon charge cloud
- Can be implemented with new detectors only – no ROIC redesign needed
- Response will not be uniform – some lateral spatial variation, some depth dependence
- Not modifiable after hybridization



Test devices fabricated in Si and GaAs



Current mode attenuating pixels are being investigated to resolve pixel level high full well constraints (large C_{store})



- Fewest number of additional devices
  - 3 additional FETs
- Can also be implemented with PFET mirror for Common Anode PD
  - CC diode requires PFET SH switches
    - Requires larger (2.3x) W/L for comparable Id_{sat} to PFET SH switches
- Gain is set by ratio of current mirror FETs M:N
  - This can be a gain or attenuation

Backup

High fluence mitigation-Global concerns

Direct high energy X-ray detection introduces large fluence concerns for the ROIC

1, 20 keV photon creates 5500 ehps

1000:1, 20 keV photon dynamic range dictates a 5.5 Me^- full well

Two primary problems arise

- Pixel storage capacitors to accommodate this signal
  - C_{store} = 733 fF for 1.2 V pixel swing
    - *Directly conflicts with adding more frames per pixel while maintaining high spatial resolution*
  - RC of C_{store} and R_{on} of shutter switch MOSFET is ~ 733 ps for 733 fF and 1 kΩ R_{on}
    - 5 τ = 3.7 ns
    - *Directly conflicts with minimum shutter performance*

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Two primary problems arise

- Pixel storage capacitors to accommodate this signal
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    - Directly conflicts with adding more frames per pixel while maintaining fine spatial resolution
  - RC of C_{store} and R_{on} of shutter switch MOSFET is ~ 733 ps for 733 fF and 1 kΩ R_{on}
    - 5 τ = 3.7 ns
    - Directly conflicts with minimum shutter performance
- Full array total photocurrent illumination concerns
  - Bondwire inductance for photodiode bias becomes a major constraint
  - $$\Delta V_{\text{bias}} = L_{bondwire} \frac{di_{photocurrent}}{dt_{diode\ risetime}}$$
  - *5.5 Me^- with a 300 ps risetime photodiode results in 2.9 mA/pixel or **1.54 kA** for a 1024 x 512 pixel array*
  - *Dictates less than **1 pH** bondwire inductance for < 10% bias droop*

Further discussion

What potential opportunities exist for collaboration on these topics?

Materials expertise for high energy X-ray detectors

Fabrication expertise for high energy X-ray detectors

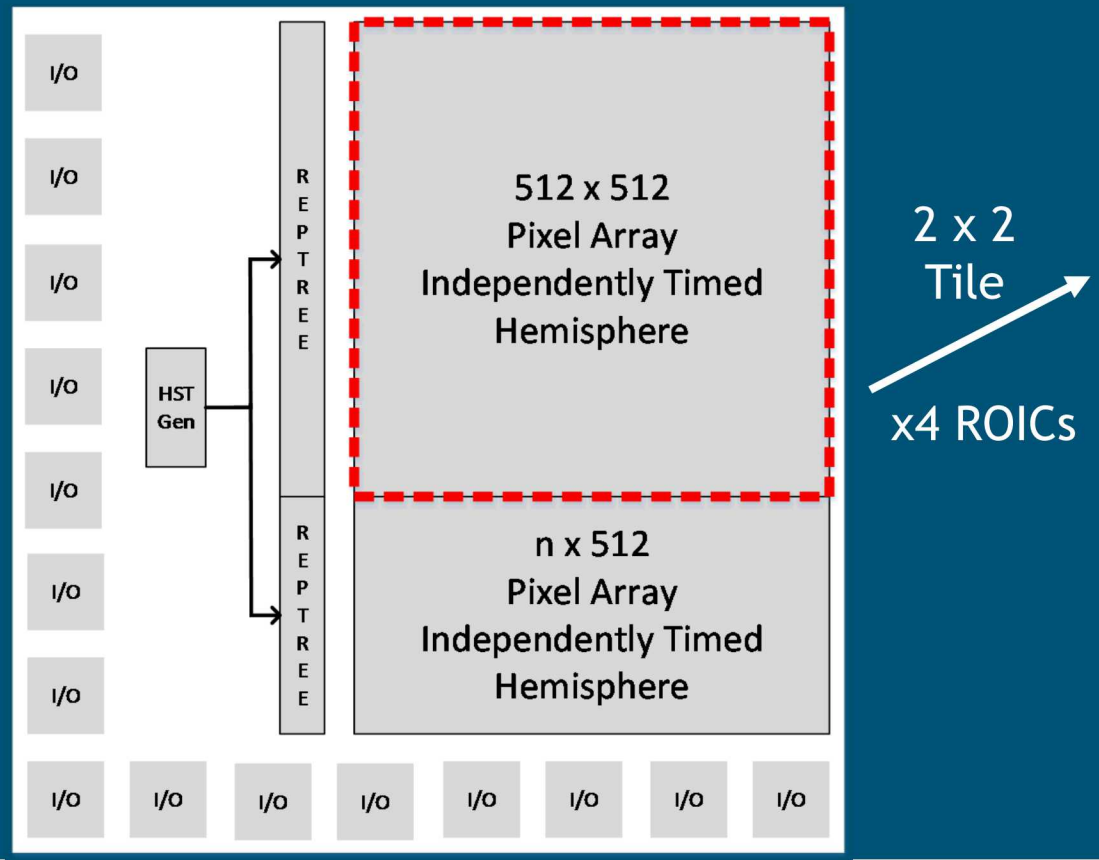
Characterization facilities or expertise for hard X-ray development

Others?

If two side abutable implementation is feasible, top/bottom hemisphere timing is still possible, but hemispheres will be not equal in size

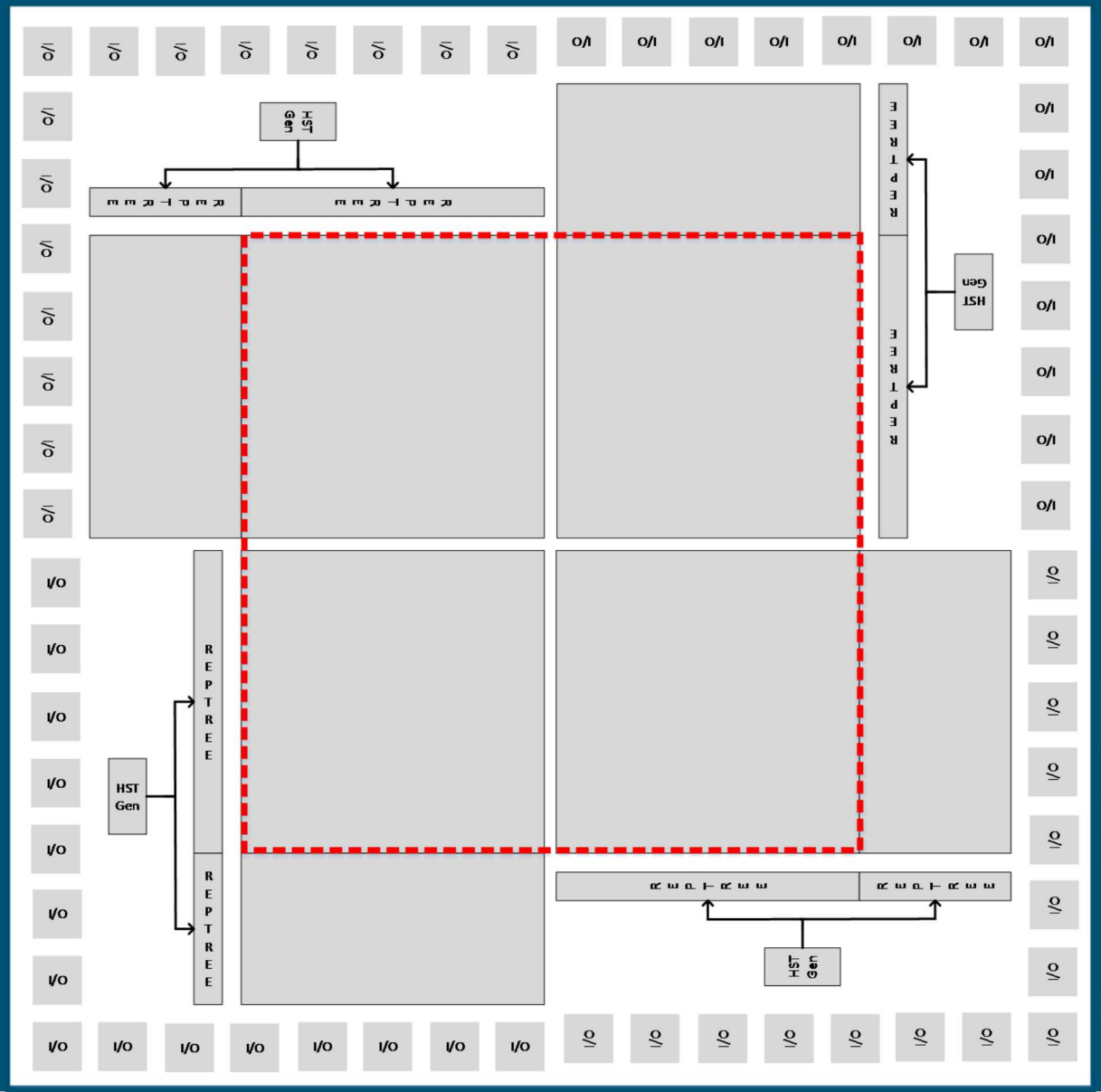
1, 1k x 1k square array with independent quadrants

4, n x 512 rectangular arrays independently timed

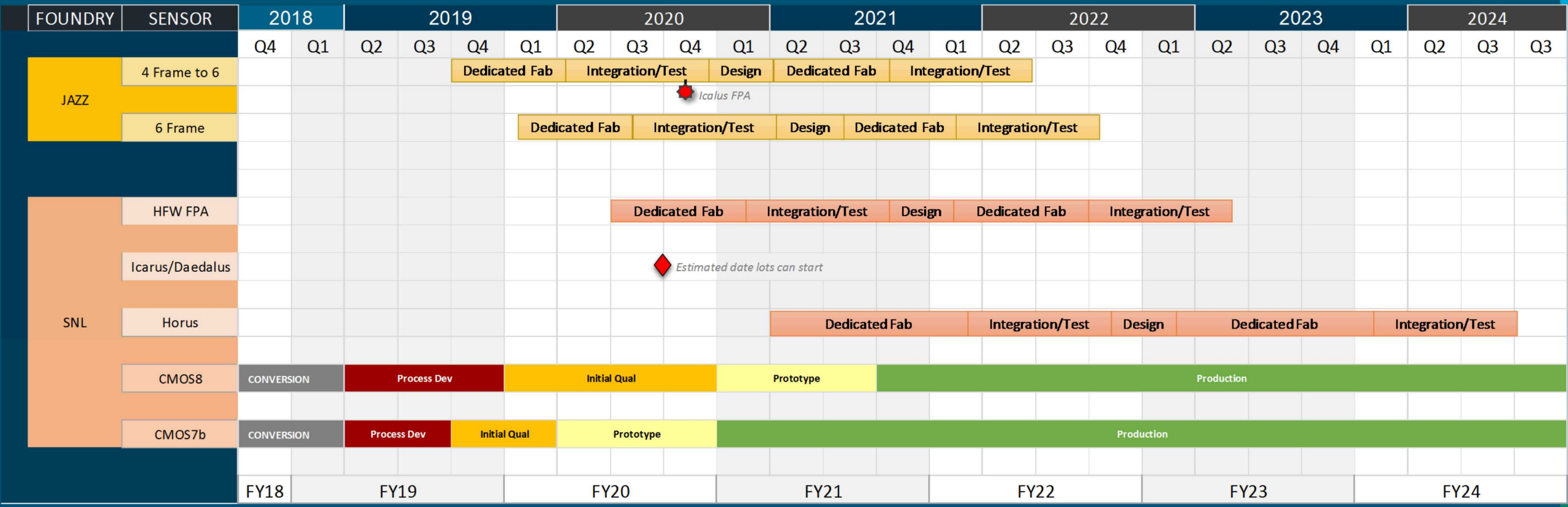


2 x 2 Tile

x4 ROICs



Icalus development timeline



Extensive testing of the Icarus sensors have yielded a deeper understanding of sensor performance

This information provides invaluable feedback to the design team

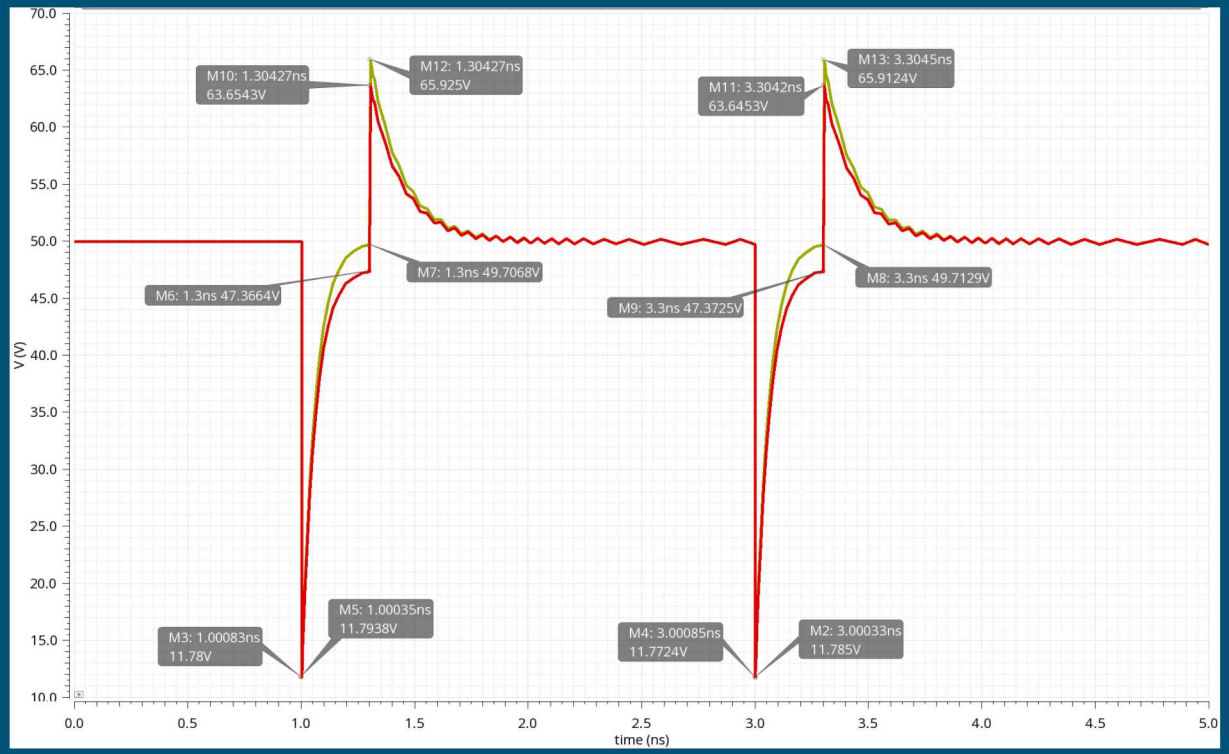
Allows users to extract the maximum performance and quality of data from these sensors

Global concerns are significant with large array illumination

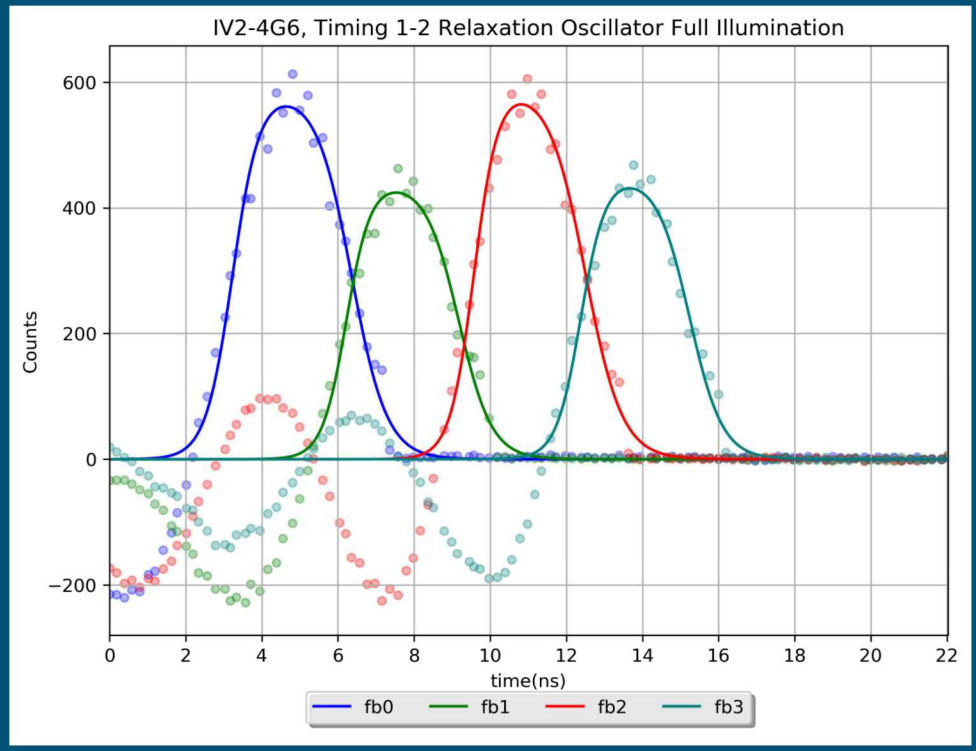
Simulations conducted at SNL to understand the primary limiting factors for large global photocurrent

500 ke^- full array illumination simulation for existing Icarus SOP packages

- 12 bondwires per corner array quadrant



Full array illuminated at 500ke^- full well simulation



LLNL full array illuminated Icarus data

Global concerns are significant with large array illumination

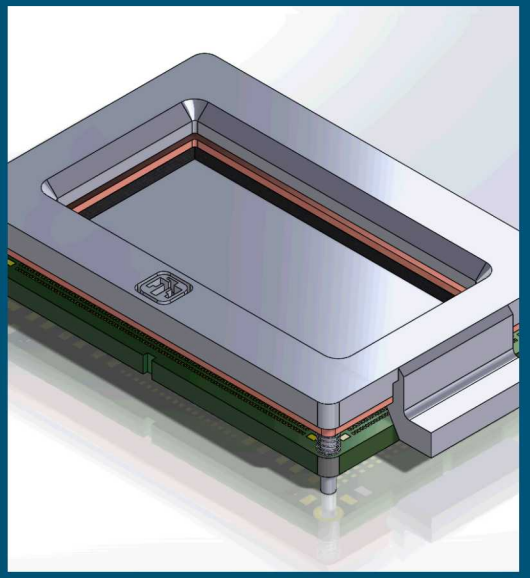
A removable copper lid has been designed to mitigate inductance on existing SOP packages
- EMI gasket provides an electrically conductive, low inductance, removable electrical contact for photodiode bias

Future packages must take photodiode bias distribution inductance into consideration

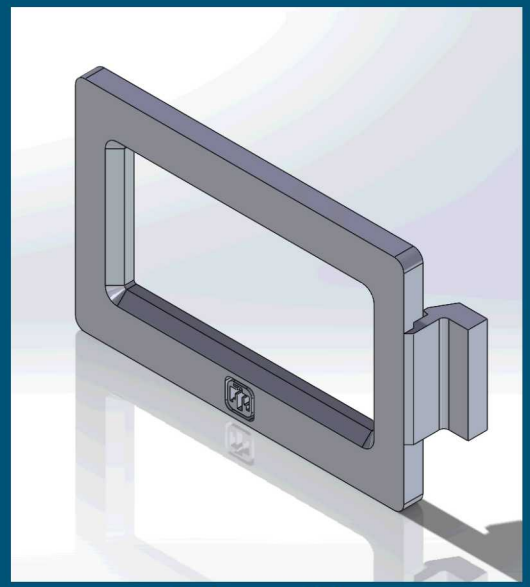
High voltage standoff needs for high energy detectors
- >300 V

One can also constrain the total illumination to a fraction of the array

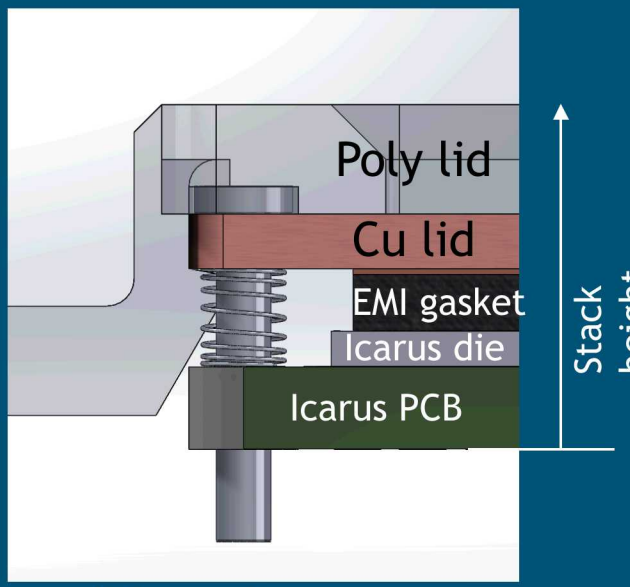
Cu lid



Assembly



Polymer lid



Cutaway of one corner

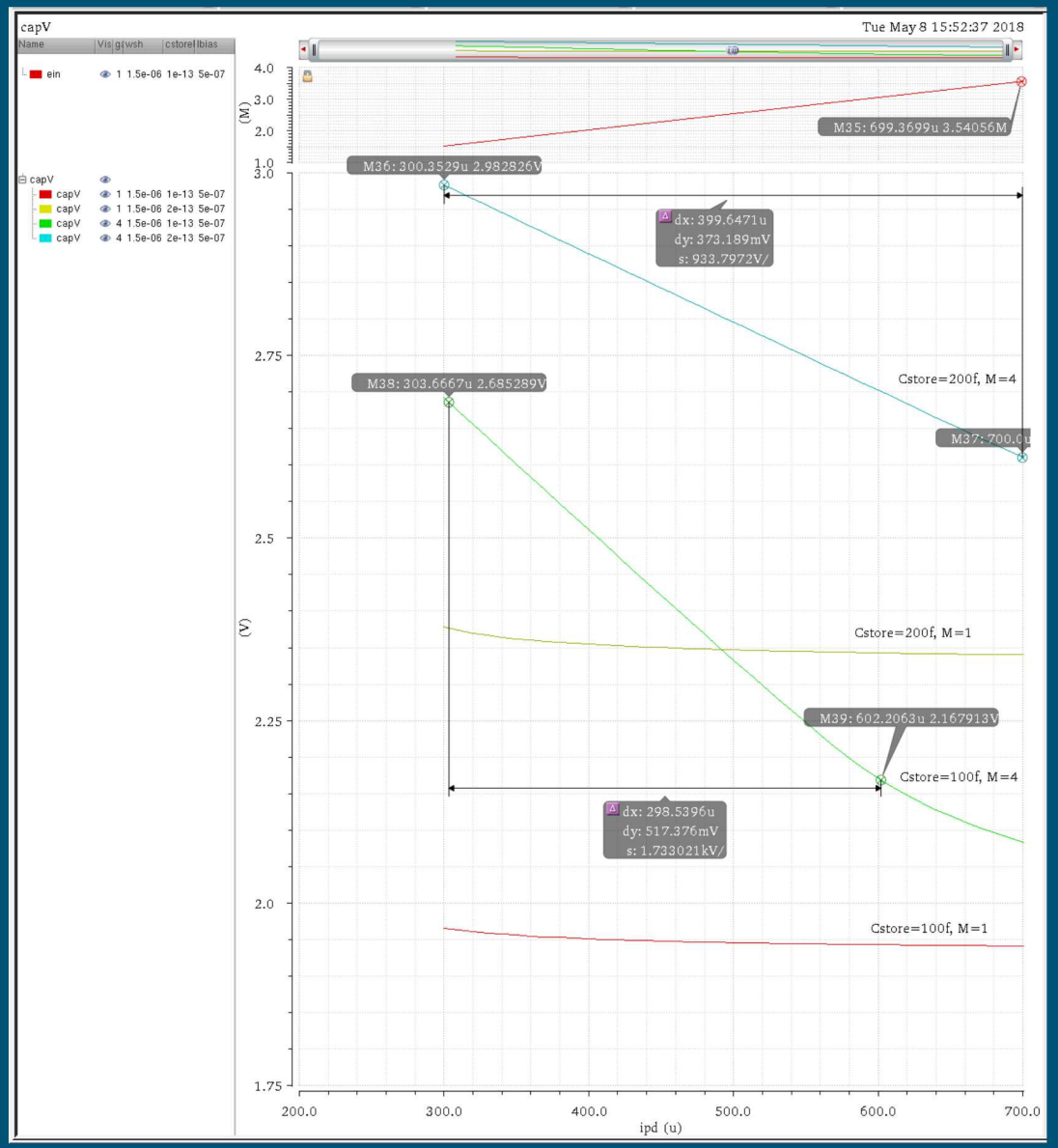
Sweeping dynamic range to 3.5 Me^- with respect to C_{store} and attenuation gain demonstrates good linearity

Left Sim DR sweep from 0 to 3.5 Me^-

Right plot = dV/di

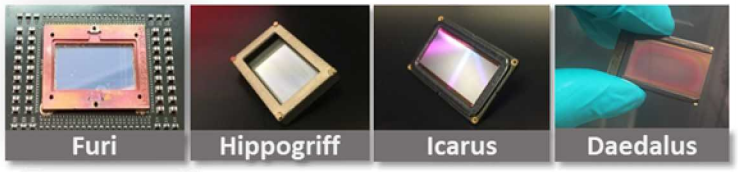
C_{store} = 100, 200 fF

Attenuation= 1, 4

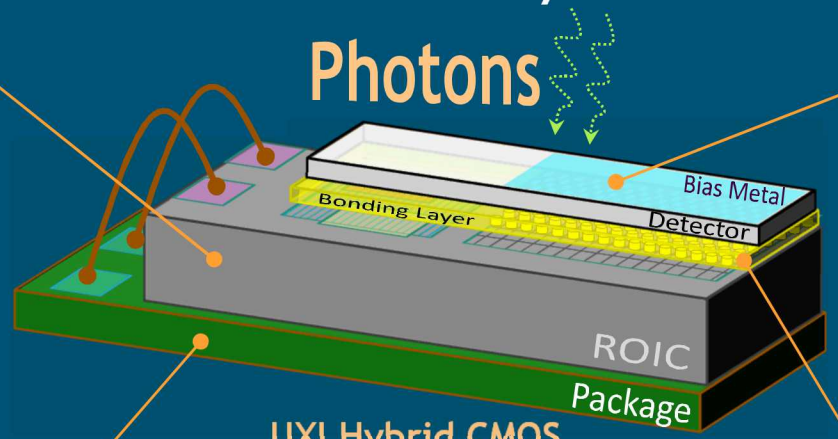


Many parts come together to become a hybrid CMOS UXI camera

Read Out Integrated Circuit (ROIC) Suite

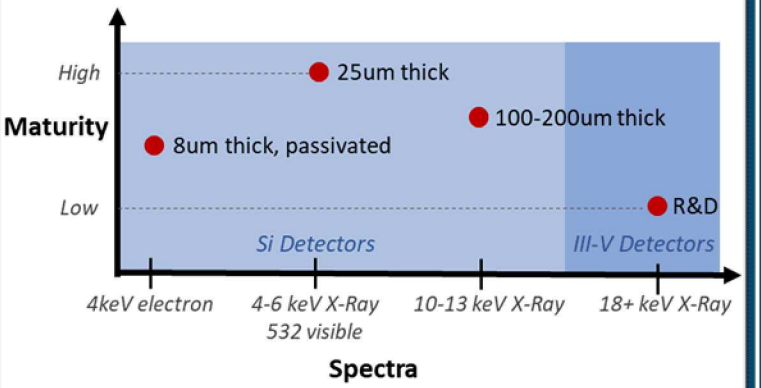


- Fabricated in SNL's 6" CMOS7 0.35 µm technology
- 1-2ns min shutter, 2-8 frames
- 1024x512, 25umx25um pixels
- Adjustable shutter timing



UXI Hybrid CMOS Sensor

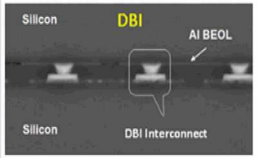
Photo Diode Array



Sensor Package

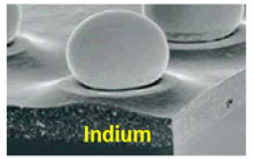
Integration

- Direct Bond Interconnect (DBI)



- External supplier used to date
- DBI process is being stood-up

- Indium bump bonding

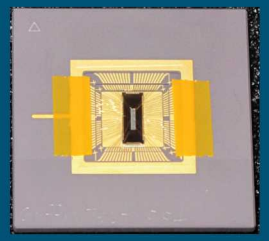


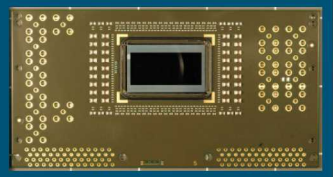
- 5-15um In balls on 10-30um pitch
- 524k connections

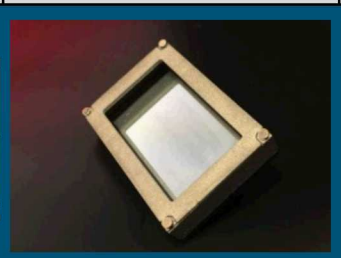
Camera System Development for Facility Specific Needs (Z-machine/NIF)

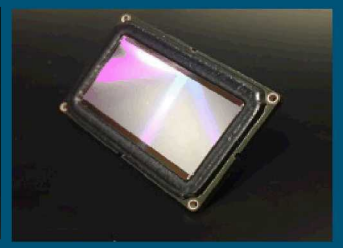
Fielded Sensor History

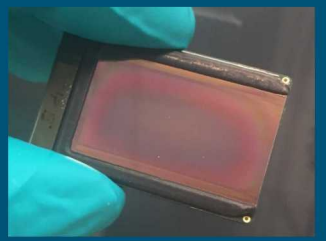
	In Use			In Test
	Furi	Hippogriff	Icarus	Daedalus
Year	FY14	FY15	FY16	FY18
Min Integration time	~1.5 ns	~2 ns	~1.5 ns	~1.0 ns
Frames	2	2 (full resolution) 4 or 8 (Row interlaced)	*4 (full resolution) *8 (L/R interlaced)	3 (full resolution) 6+ (Row/L/R interlacing)
Tiling Option	No	No	No	One Side
CMOS Process	350 nm (SNL)	350 nm (SNL)	350 nm (SNL)	350 nm (SNL)
Pixels	448 x 1024	448 x 1024	512 x 1024	512 x 1024
Pixel Size	25 μm x 25 μm	25 μm x 25 μm	25 μm x 25 μm	25 μm x 25 μm
Capacitor Full Well	1.5 million e^-	1.5 million e^-	0.5 million e^-	1.5 million e^-









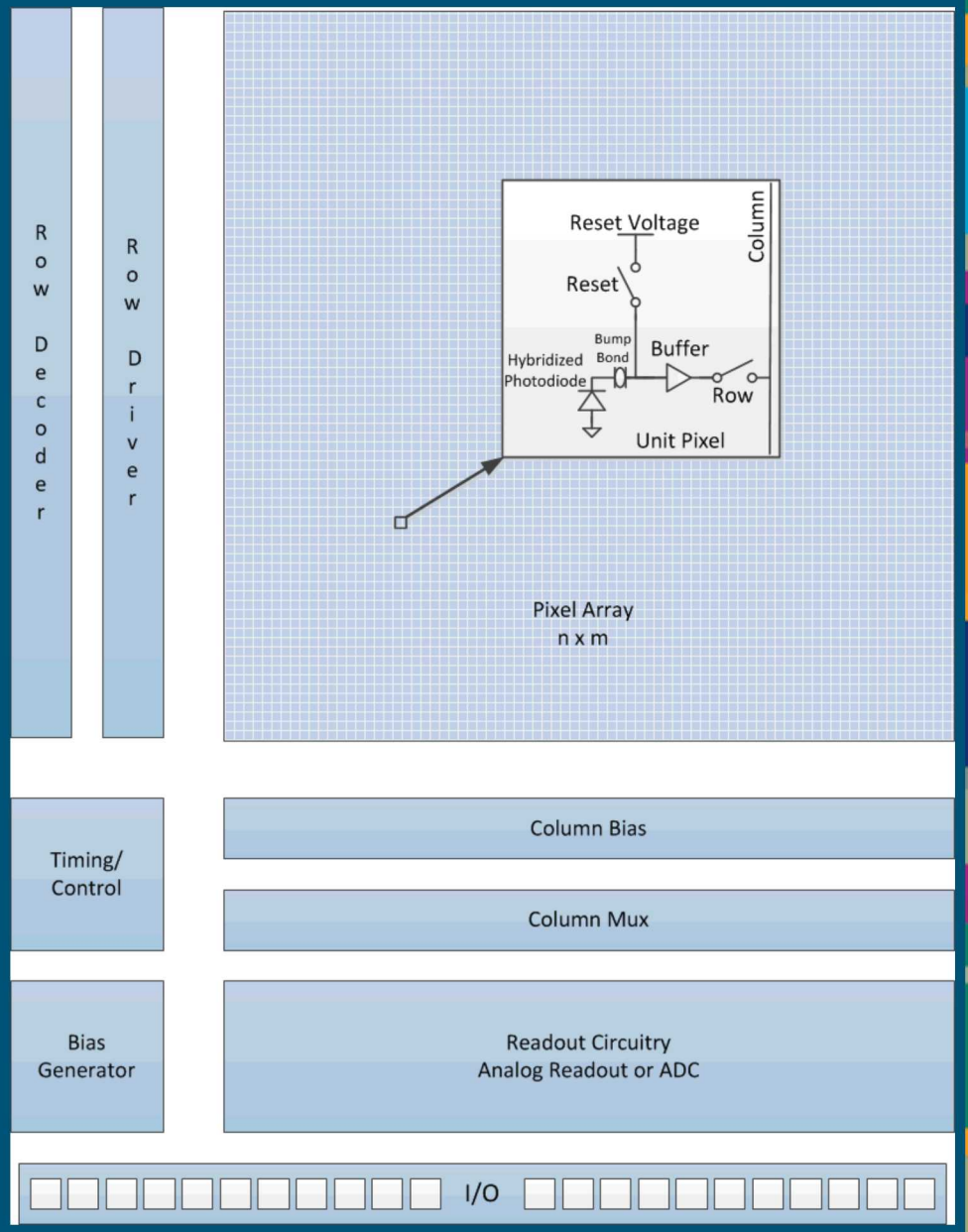


Traditional CMOS camera architecture serves as the base concept for burst mode imager development

A photodiode acts as the photon-to-electron transducer

Pixel circuitry converts this electron charge (Q) to a voltage or current

Support circuitry facilitates decode and readout of the pixel array



ICF facilities operate on a very slow rep rate so burst mode imagers fit the application well

Burst mode cameras store each frame of image data in-situ for high speed operation

- Multiplexes multiple pixels into one
- A transistor switch acts as an electronic “shutter” for each frame

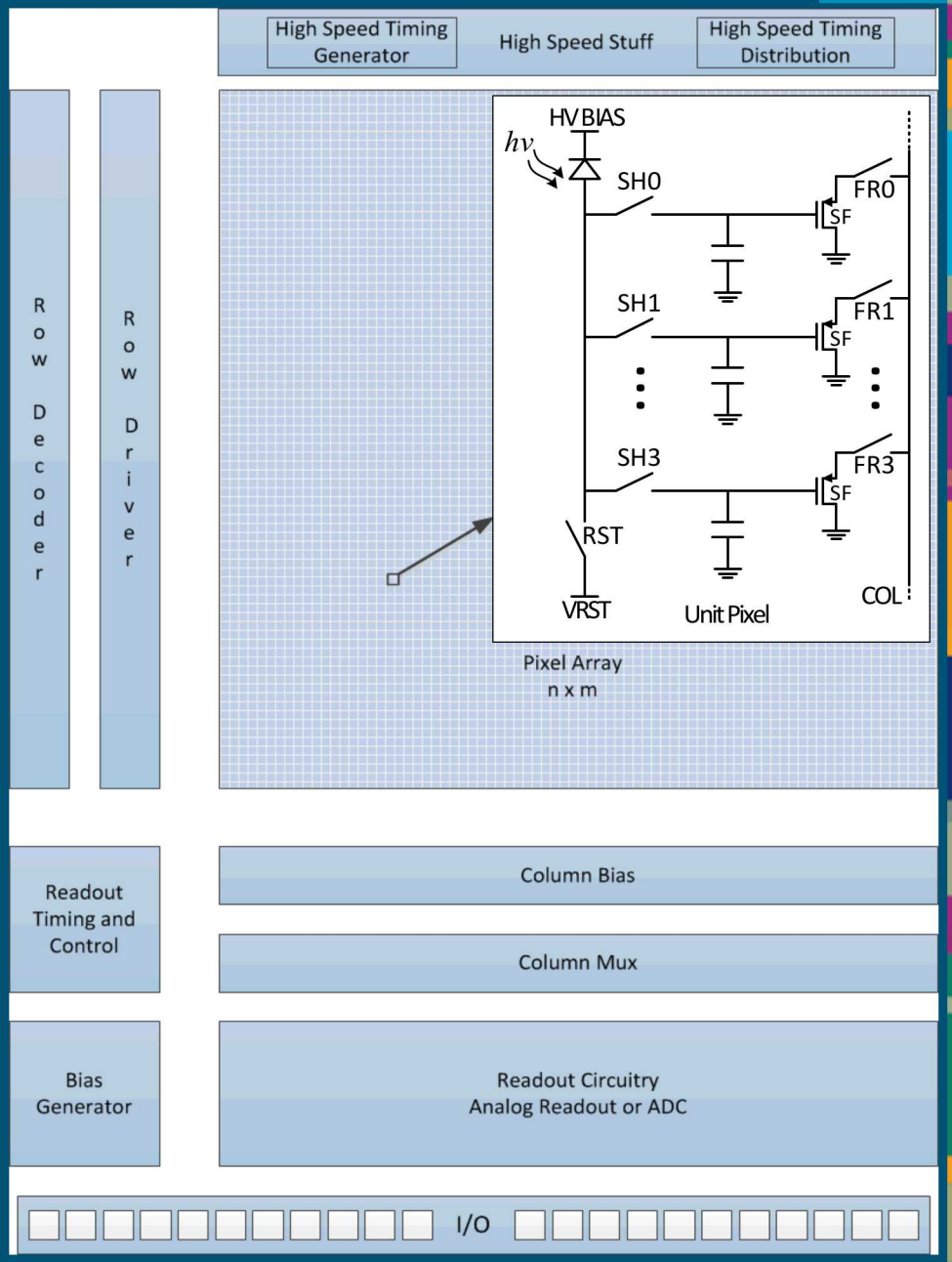
In-pixel storage introduces conflict between

- Pixel spatial resolution
- Full well capacity
- Number of frames
- Capacitive density is a critical design element

Configure the part prior to the experiment

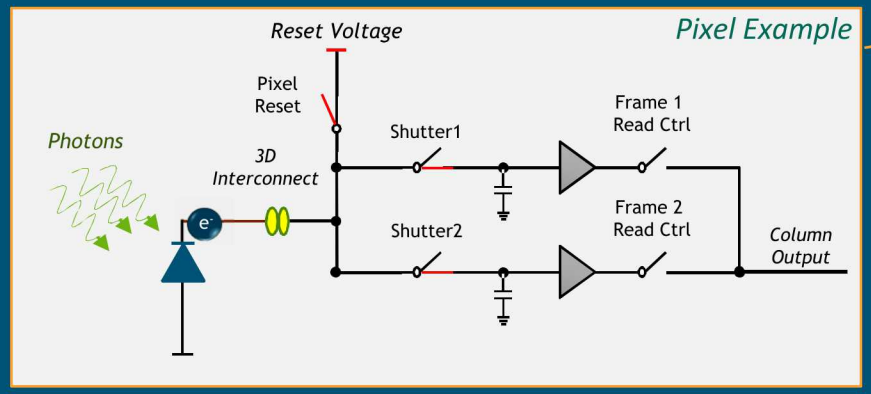
Trigger and capture images on a high speed (ns) timescale

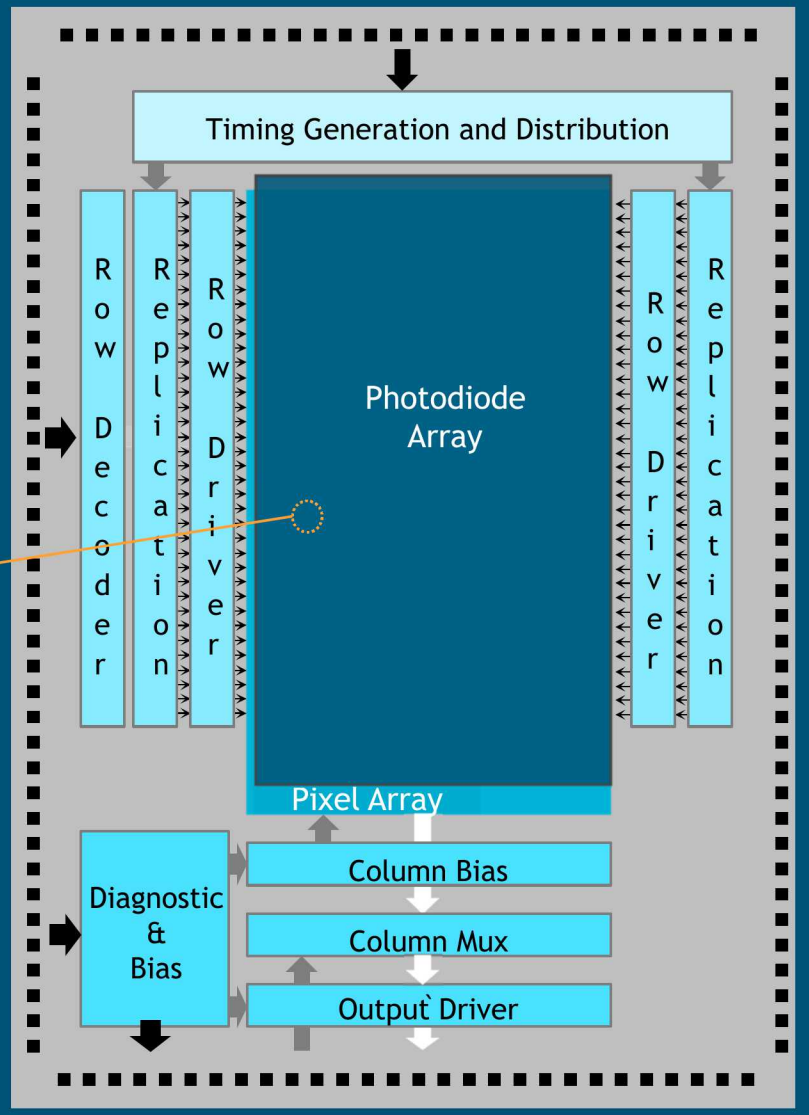
Read off information stored in-pixel on a slow (µs-ms) timescale



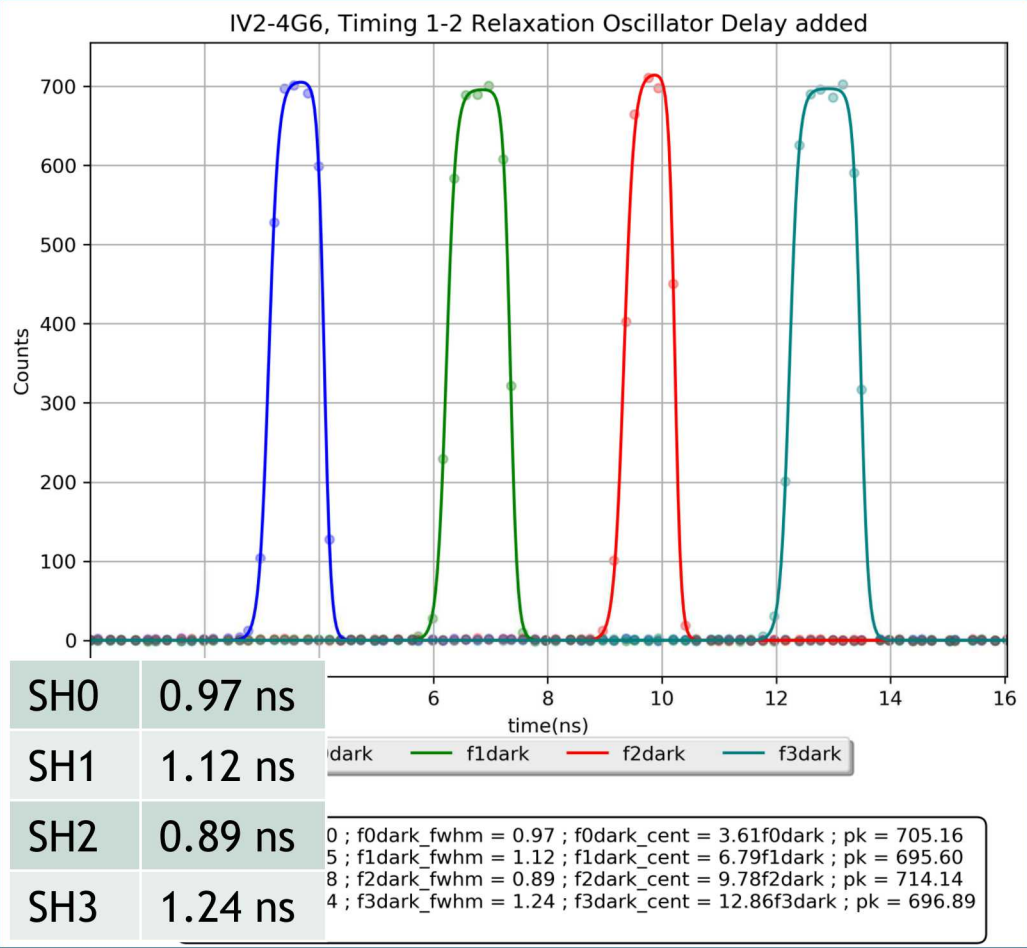
Sandia hCMOS have three distinct operational phases when capturing an image

1. Configuration Phase
   - Shutter profile is entered
2. Triggered Image Capture
   - Pixel array and diagnostics are reset
   - High speed shutters generated/distributed
   - Images captured and stored
3. Readout
   - Random access readout of images



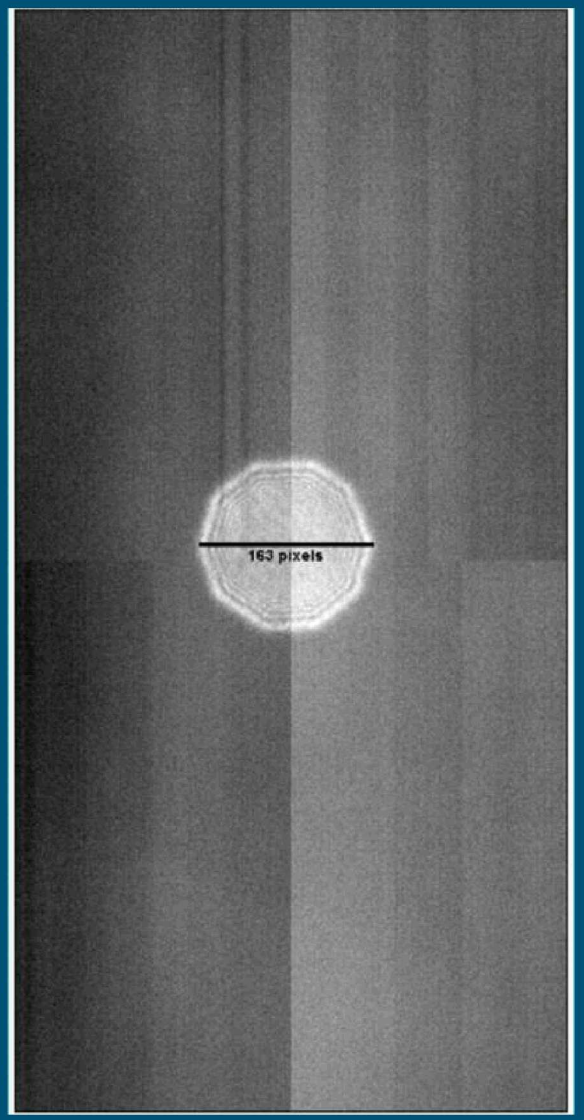


Global effects and photodiode speed dominate fastest integration time currently achievable with Icarus



SH0	0.97 ns
SH1	1.12 ns
SH2	0.89 ns
SH3	1.24 ns

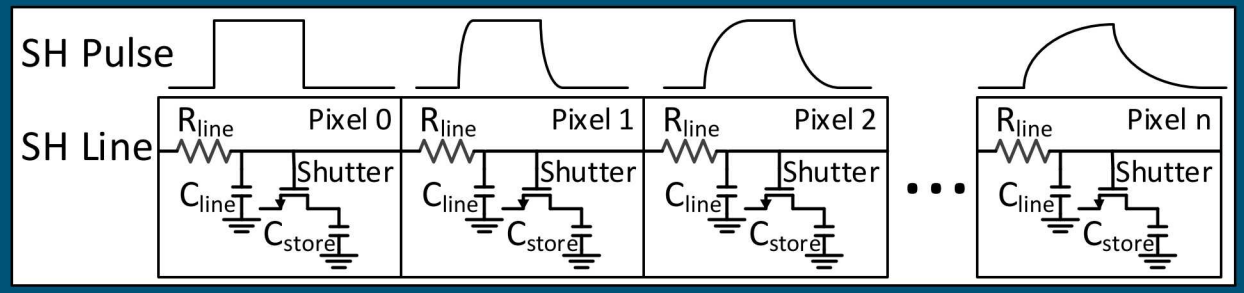
1 ns timing shutter profile, aperture exposing ~4 % of the array, 5.6% full well illumination, 8 µm thick photodiode



Aperture shutter profile

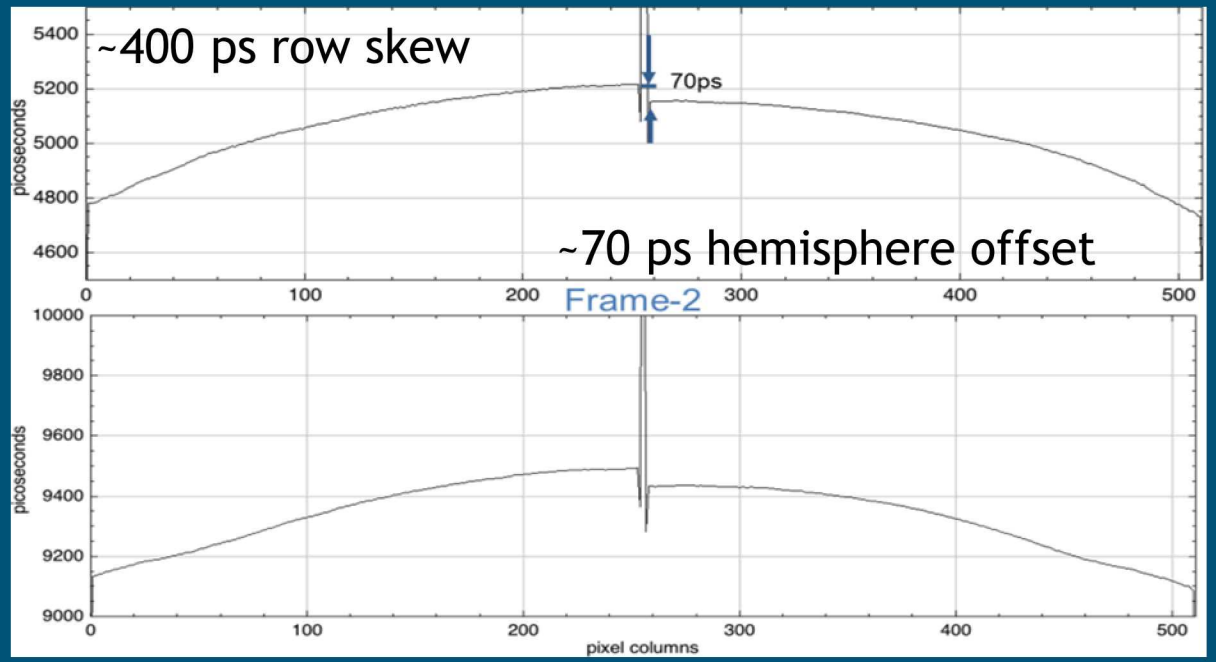
Row-wise timing skew is also an issue with current UXI camera implementations

Driving the distributed RC load of many pixels introduces a timing skew from the outermost pixel columns to the innermost pixel columns

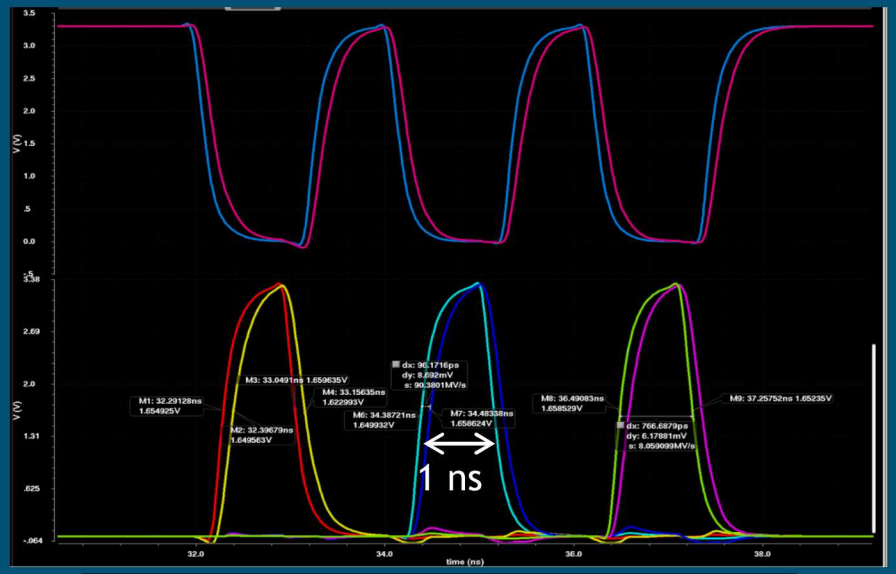


Icarus exhibited slightly worse timing skew (400 ps) than past camera due to increasing the pixel row length from 224 to 256

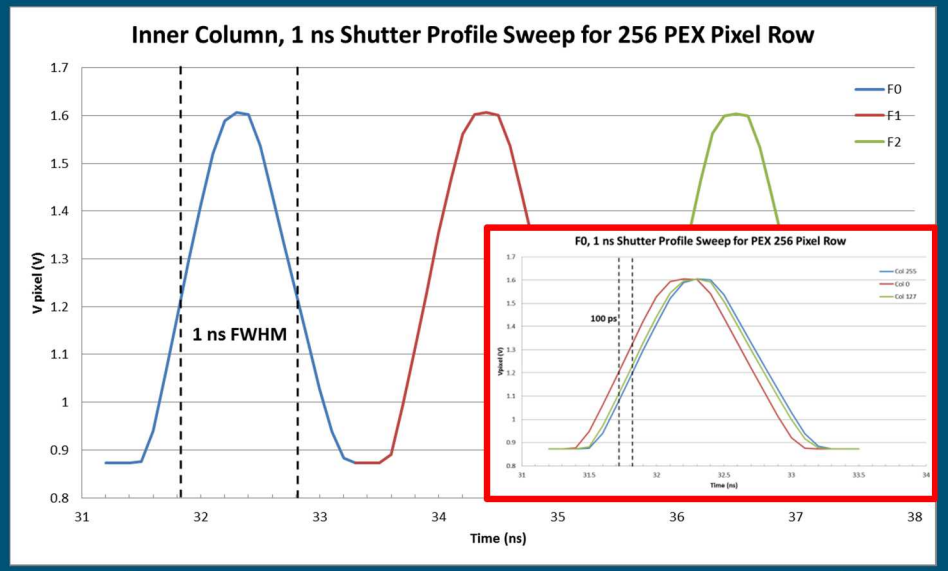
- Hemisphere offset tuned to 70 ps



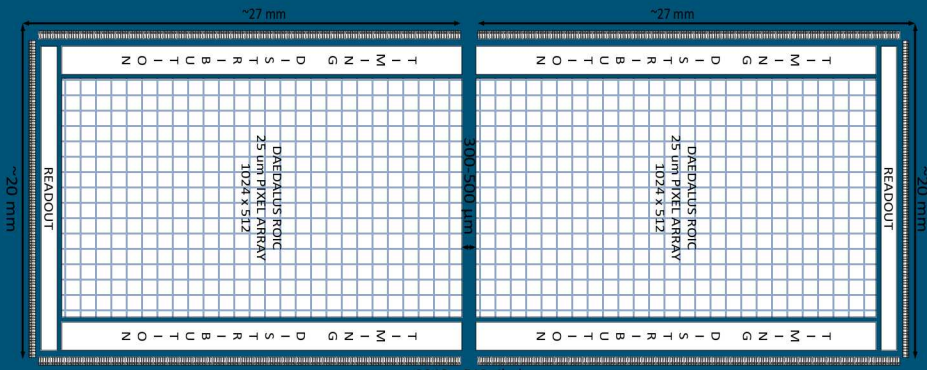
Daedalus is functional electrically and is currently undergoing packaging



1 ns row shutter timing parasitic sim

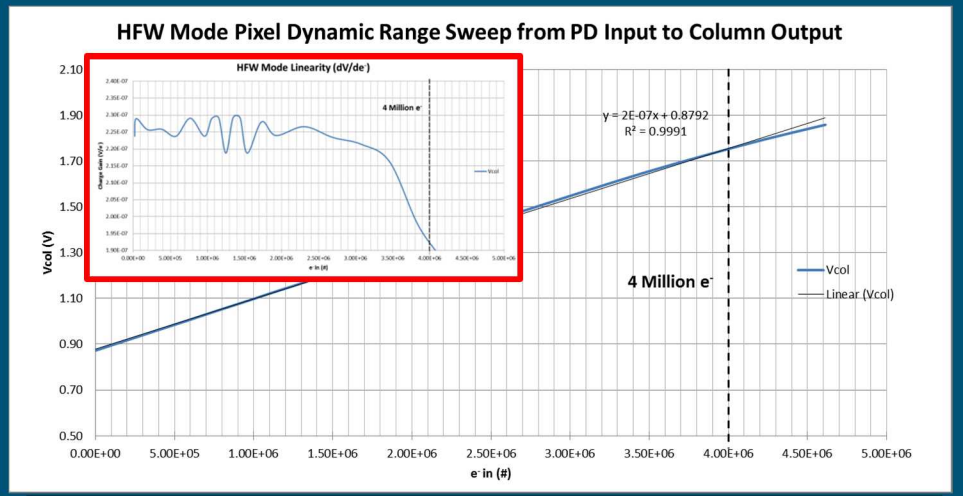


1 ns simulated shutter profile



2 tiled imager concept

Active array size: 12.8 mm x 51.2 mm

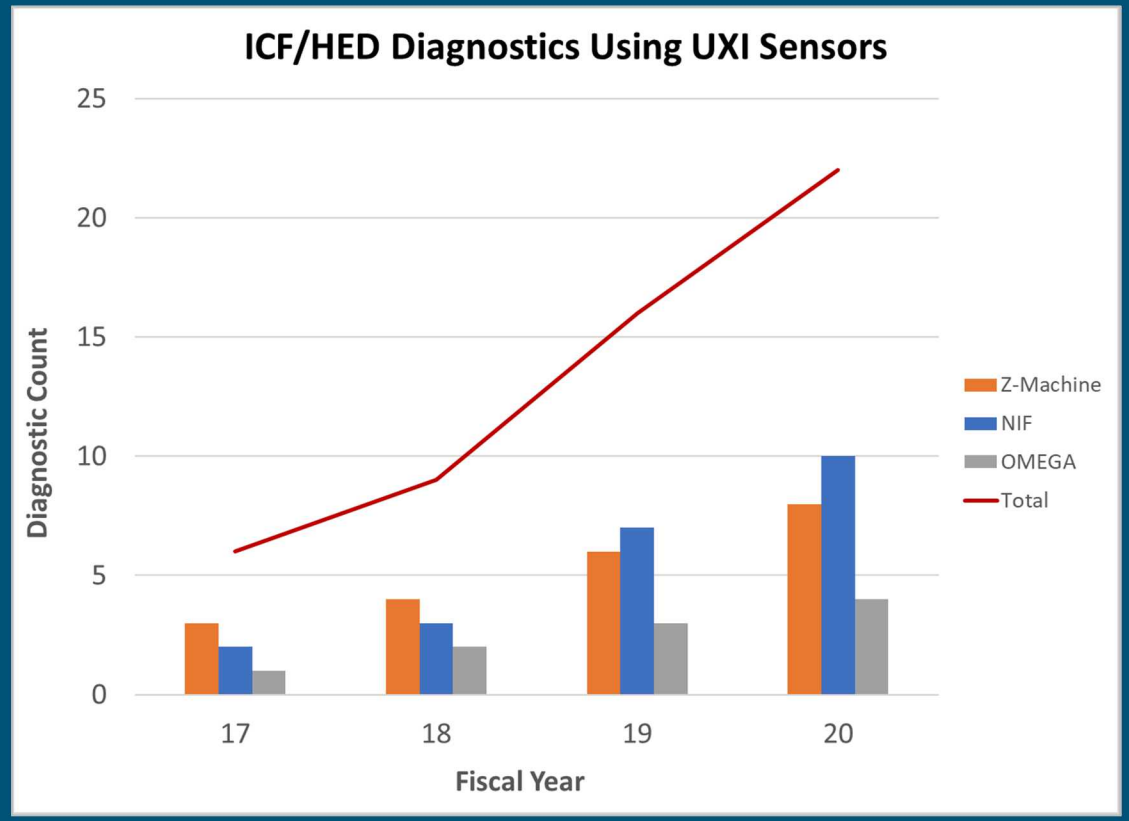


High Full-Well mode DR simulation > 4 million e-

Future work and applications are expanding the scope of the UXI program

Multiple additional facilities are fielding or plan to field UXI sensors

- 19 additional diagnostics are planned for ICF diagnostics utilizing UXI sensors
  - Stanford Linear Accelerator (SLAC)
  - French CEA, Laser Mega Joule
- Other DOD/NW applications



Is there a path to 2D, sub 100 ps imagers?

Etoh, Takeharu Goji et al. “The Theoretical Highest Frame Rate of Silicon Image Sensors.” Ed. Vittorio M. N. Passaro. *Sensors (Basel, Switzerland)* 17.3 (2017): 483. *PMC*. Web. 2 May 2018.