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Comparing Circuit Connectivity Between All-Metal GDS Layouts

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***Abstract*—We present a methodology to compare the connectivity of all-metal layouts using new methods supported by functions existing in commercial tools. Industrial design tools such as Mentor Graphics Calibre and KLayout contain some of the necessary layout manipulation and comparison methods. However, microscope-derived GDS2 does not contain the semiconductor devices which design tools presume to exist. Accordingly, we augment and extend the commercial methods to accommodate our requirements. Our extensions for all-metal GDS2 comparisons create three complementary connectivity measures. Two are created by providing the necessary conditions for Calibre's layout-versus-schematic (LVS) and parasitic extraction (PEX) analyses, both with new post-processing. The third uses KLayout functions to identify opens and shorts in a microscope-derived GDS2 compared to a design GDS2.**

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I. Introduction

Research and development funded by IARPA's RAVEN program seeks to create microscope technologies for supply-chain verification of microcircuits. Methods used during microscopic examination, data collection, and processing are imperfect and can erroneously affect the layout of the microcircuit under examination. Layout comparison can be used as a means to understand the consequence of cumulative imperfections and estimations made to the original layout. Layout comparison can therefore assess the quality of the applied microscopic examination methods. In order to perform layout comparison, an efficient method to compare design GDS2 to microscope-derived GDS2 must be implemented.

Industrial design tools such as Calibre and KLayout contain some of the necessary layout manipulation and comparison methods. However, microscope-derived GDS2 does not contain the semiconductor devices which design tools presume to exist. Thus, the layout comparison functions in design tools cannot be used as they are applied in microcircuit fabrication. Accordingly, we augmented and extended the commercial methods to accommodate our requirements. Our extensions for all-metal GDS2 comparisons create three complementary connectivity measures. Two are created by providing the necessary conditions for Calibre's layout-versus-schematic (LVS) and parasitic extraction (PEX) analyses, both with new post-processing. The third uses KLayout functions to identify opens and shorts in a microscope-derived GDS2 compared to a design GDS2.

The paper is organized as follows. Section II provides background information on microscopic investigation, KLayout, and Calibre. Section III presents the problems that occur when attempting to use the tools as-is to compare circuit connectivity of microscope-derived GDS2. Section IV introduces our augmentations and extensions to these tools. Section V describes a series of verification, validation, and sensitivity tests to measure our extensions. We demonstrate the improvements made when using our extensions for particular edge cases and summarize the capabilities of each method. Section VI discusses areas of our solution which would benefit from further work.

II. Background

A. Microscopic investigation techniques

The process of obtaining the design GDS2 and microscope-derived GDS2 is as follows. A chip is designed using a layout editor tool and assembled using standard manufacturing methods. The design GDS2 is the layout used during the chip manufacture process. A separate GDS2 layout is extracted using a microscopic investigation method. The microscope-derived GDS2 layout, also called the observed or scanned GDS2, is the layout extracted from this method. The scanned GDS2 is compared to the design GDS2 used to manufacture the chip. In this way, the quality of the microscopic investigation method is gauged. In some cases, post-processing of the design GDS2 file is required to merge common layers which have different GDS numbers and/or purpose numbers. For example, in multi-patterned technologies such as advanced FinFET nodes, there may be two GDS layers with the same GDS numbers, but with different purpose numbers (Metal-1, for example) [9]. In these cases, the different layers are merged into a common GDS layer.

There are various ways to extract the GDS layout from a chip via microscopic investigation. One method is to surface-scan the chip one layer at a time by incrementally removing layers of material from the chip until every layer is scanned [3][5]. The layers from the scan are stitched together via post-processing. Another method involves scanning multiple layers at once using non-destructive X-ray microscopy [4]. The sections scanned are then stitched together via post-processing.

These and other microscopic investigation methods have the potential to introduce a variety of deformities into the GDS2 that were not present on the manufactured device. In some cases, these deformities are harmless, but in other cases they affect circuit connectivity and must be accounted for.

B. Microscopic investigation phenomena

Deformities that microscopic investigation methods may introduce are as follows. *Dilation* occurs when the border of a metal feature is magnified, causing the edges to balloon outward. *Erosion* causes the opposite effect; all edges of a metal feature shrink inwards. *Displacement* occurs when metal traces in a layer shift due to imprecise scanning. *Scaling* occurs when the units of the design GDS2 do not match the units of the scanned GDS2. *Patching* occurs when only particular portions of the GDS2 file are scanned. *Additive noise* introduces extra metal into a layer, for example caused by particulates encountered during investigation. *Subtractive noise* produces the opposite effect and removes metal from the scanned GDS2.

These deformities combine to produce more complex phenomena. *Fusion* occurs when two metal features overlap during scanning and become a single object in the resulting GDS2. *Bridging* is the fusion of nearby metal traces. *Mouse biting* causes small sections to be removed from the edges of metal. *Splitting* occurs when erosion causes thin metal features to disjoin from one another. *Resolution errors* are introduced when processing converts curved pieces of metal into rasterized right-angled features. *Warping* is caused by nonlinear translational errors during the investigation process which warps the coordinates of scanned objects. *Stitching errors* occur when two portions of a layout are scanned separately, stitched back together, and phenomena produced by the investigation method create imperfect layout alignment.

C. Calibre

Calibre is an industrial tool capable of performing LVS and PEX to isolate connectivity errors between two GDS files [6]. The tool performs LVS by first generating a circuit netlist from the design GDS2. The tool is then given the observed GDS2 and tasked to compare this layout to the prior netlist. In order to perform this comparison, Calibre generates a circuit netlist of the observed layout and compares the two netlists using graph analysis techniques.

Calibre is optimized to handle large GDS files. Since Calibre compresses the circuit representation into a netlist representation, the resulting netlists are easy to work with and present no bottleneck to software performance. However, the compression removes location information from the files. Location information is necessary when there are many similar connection patterns within the layout that must be distinguished.

D. KLayout

KLayout is an open source, high performance layout viewer and editor capable of operating on objects within a GDS2 layout via Design Rule Checks (DRCs) [10]. DRCs are fundamental logic operations performed on the features in the GDS2. For example, if the AND DRC were performed on two features then the resulting features represent their intersection. Connectivity analysis techniques can be performed using KLayout's built-in software along with DRC scripts. The software also uses a connectivity tool capable of determining all objects connected to one another through adjoining layers of metal.

Although KLayout is capable of powerful analysis using these built-in techniques, the tool is limited in terms of performance. It is not portable to graphics processing units (GPUs), which makes the sequence of DRC scripts incapable of being quickly performed when working with large-scale layouts. The connectivity analysis tool also requires all objects to be loaded into memory, bottlenecking large GDS2 files and limiting the breadth of connectivity coverage that the tool can provide.

III. Motivation

Both Calibre and KLayout are both capable of performing connectivity analysis for a comprehensive variety of circuit verification problems. However, their connectivity metrics make hard assumptions on the data provided. If the scanned GDS2 does not lie within the operational envelope of the tools, then their connectivity metrics begin to break down. In this section we explore the assumptions made by Calibre and KLayout and observe that these assumptions may not always be upheld when performing connectivity analysis of layouts produced via microscopic investigation techniques.

A. LVS assumptions

The Calibre and KLayout tools use LVS techniques to locate differences in connectivity between two layouts. If the two layouts represent different circuit designs, there is no merit comparing them. It is therefore assumed that the two layouts are already very similar in structure. This assumption could easily be violated during microscopic investigation if a large-scale inaccuracy introduces significant errors in the scanned layout or if the scanned layout is missing large metal regions. Regardless of the appearance of the scanned GDS2, the connectivity differences must be accurately quantified with respect to the design GDS2.

LVS is typically performed when an engineer aims to verify whether a GDS2 layout generated from software or modified by hand matches the circuit design. The CAD tools are therefore tasked to locate minute discrepancies and notify them to the engineer. The tool was not intended to quantify the extent of large-scale discrepancies [7]. To elaborate, take for example a short circuit that has connected many pins together. Modern tools would classify the anomaly as a single short circuit, however the short circuit impacts many places of the netlist and is considerably more complex than a short between only two pins. Since the objective is to quantify the level of connectivity in the scanned GDS2, we require a method to measure the extent of shorts and opens not found in contemporary LVS techniques.

Modern tools also make assumptions about circuit patterns found inside the GDS2 layouts. It is reasonable to assume that a circuit contains devices, however microscopic investigation methods cannot always extract these devices. Therefore, some layouts may only contain a large network of wire routing with no devices completing the logical function of the circuit. We assume the worst case scenario in this work and remove all devices from the layouts. Devices are used by netlist solvers as landmarks to distinguish between similar circuit patterns [8]. When they are removed, networks can become ambiguous and the netlist solver is more likely to come across areas which it cannot distinguish with certainty.

Furthermore, if all of the devices are removed from a complex circuit, then the circuit becomes compartmentalized into a set of small disjointed circuits. Assumptions can be made about the structure of embedded circuits to aid graph matching netlist solvers [1]. These assumptions are no longer true if the circuit within the chip is separated into many smaller nets. As more of the circuit is compartmentalized, each portion of the netlist encompasses less structure [8].

B. *Patch assumptions*

As was discussed in Section II, KLayout is not capable of handling large GDS2 layouts. When the entire circuit cannot be loaded into memory, the layout must be broken up into smaller pieces. LVS can then be performed on each section, given a correspondence between the layout and netlist.

Problems arise when patches are extracted from a scanned layout. It is not guaranteed that a patch taken from the scanned GDS2 corresponds to a co-located patch from the design GDS2. Stitching errors and warping can produce a patch that is very different from the design GDS2. Although the patch may appear different, the connectivity within the layout is preserved by such phenomena. For example, a minute horizontal shift in a layer due to stitching errors does not affect the connectivity of a circuit until the shift causes a metal contact to disconnect from a via. Contact points are typically padded, giving a high tolerance to investigation phenomena. However, sampling a patch from a layout reduces tolerance. If the stitching error removes a portion of metal from the patch that is present in the design, then LVS will mistake the missing metal as an open circuit regardless of whether the circuit remains connected. Patches are therefore more sensitive to perturbations present in the scanned layout, and methods for registering two patches to one another must be used in order to increase the tolerance of patches from investigation phenomena.

IV. METHODS

In order to overcome the shortfalls presented in Section III, we provide new methods of analyzing GDS connectivity using Calibre and KLayout. We first establish the methods used to extract GDS patches. We then observe that by enriching the Calibre tool's functionality and combining the results with a new KLayout connectivity analysis method, we achieve a comprehensive connectivity metric capable of handling most of the phenomena produced during microscopic investigation.

A. *Patch method*

Since KLayout is not able to process large layouts, we perform the connectivity analysis on cross section patches sampled from the GDS. A cross section patch is a rectangular column with arbitrary bounds taken in the same location for every layer. To provide the best possible comparison, each layer in the cross section of the scanned layout is aligned using the layer from the design patch. This alignment is performed separately for each patch.

B. *Enriching Calibre LVS*

In order to produce an accurate and representative measure using Calibre's LVS techniques, devices must be included in the netlist. We present the Calibre LVS method that performs LVS with devices added to the GDS2 files manually. We also present the Calibre PEX method that performs PEX to automate this process.

1) Manual device placement: In order to achieve a device placement that is tolerant to investigation phenomena, we perform LVS on patches described from Section IV.A. Devices are inserted onto every exposed metal edge around the perimeter of the patch. Fig. 1 demonstrates how the extra material is inserted into the layout. The original patch is shown in gray and devices are specified by red rectangular features with an exclusive purpose number recognized by Calibre LVS as resistive elements. Every device is also given a unique label mandated by Calibre LVS.

Manually adding devices and labels to both layouts increases the possibility for label mismatch. Label mismatch could occur, for example, if the scanned layout has additive noise along the edge of a patch. Particulates along that edge would be given a unique label which should have been given to a metal feature instead. To prevent label mismatch, we connect all devices together with a wire bordering the patch and give the wire a unique label. Fig. 2 shows this correction; the original patch is shown in gray, device markers are shown in red, and metal

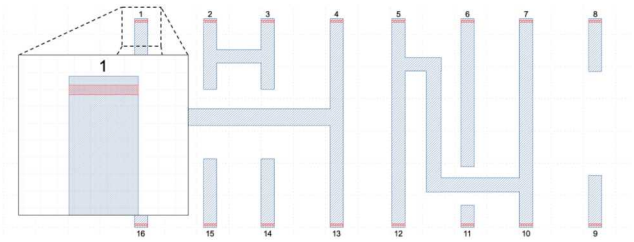

Fig. 1. Manual device insertion

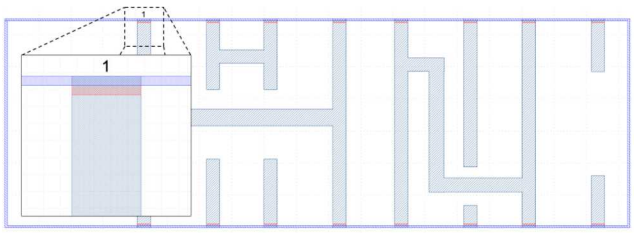

Fig. 2. Label mismatch prevention technique

connecting the perimeter is shown in blue. The resulting Calibre LVS method is able to analyze the connectivity of a patch, granted the additional overhead of manually connecting the metal features along the edge of the patch and adding device markers.

Through the LVS process, resistors are added where resistive elements were placed. A visualization of the Calibre LVS method is shown in Fig. 3. The visualization includes a netlist overlaid on top of the patch, showing the connections made by the LVS method. Resistors added by the method are boxed in orange, and connections between the resistors are illustrated in dark red.

2) Automatic device placement: Devices can also be placed automatically by using Calibre's PEX capabilities. Instead of producing a labeled set of devices along the perimeter of the patch, PEX places devices incrementally along all pieces of metal in the patch, according to the resistance and capacitance properties of the metal features. We use Calibre's maximum resistance and capacitance reduction settings during PEX to achieve minimal device placement. After the devices are inserted into Calibre, the edges are connected together and labeled with a unique character as before. Fig. 4 shows the result of PEX after device reduction and label mismatch prevention. Capacitive elements are removed for demonstration purposes.

Note the extra devices in Fig. 4 not present in Fig. 3. Devices placed using PEX are also placed internally. For the case in Fig. 4, such device placements would help distinguish connectivity differences. However, when mouse bites, additive noise, or resolution errors are introduced, PEX cannot simplify its device placement which results in a hypersensitive connectivity measurement. The results from these cases are presented in Section V.

C. KLayout Flow method

The Calibre LVS method introduced in the previous section enables LVS to provide a connectivity difference measurement for the scanned layout. The method provides the layouts with devices and bandages the disjoint circuits into a whole, but the method never overcomes the fact that LVS is a verification technique not intended to quantify the extent of shorts and opens in the layout. A method designed to quantify the extent of shorts and opens is established using KLayout.

In order to design this method, we make an observation about the edges of a patch taken from the microscope-derived GDS2. Each edge represents a piece of metal in the circuit, connecting metal from outside the patch to metal inside the

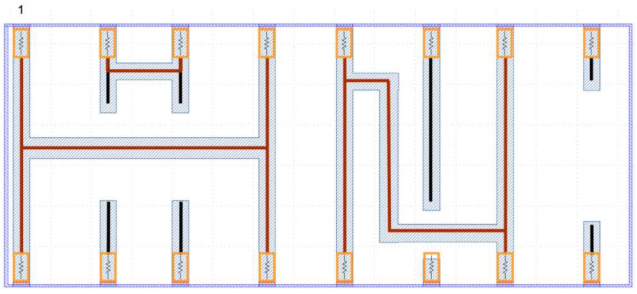

Fig. 3. Manual resistor insertion and reduction

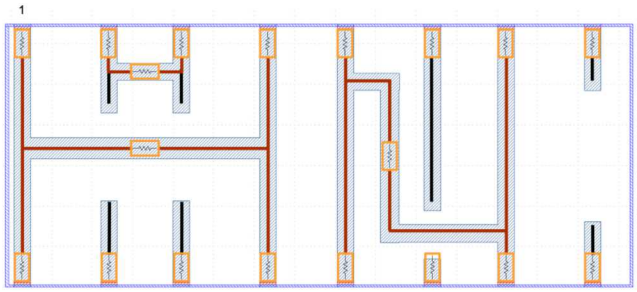

Fig. 4. Automatic resistor insertion and reduction

patch. If we follow the connections from inside the patch, we eventually reach other edges of the patch where the connection continues beyond its boundaries. Essentially, the connectivity of the patch flows in from one edge and out none, one, or many other edges of the patch. If each edge is followed in this way, we observe a recognizable connection pattern unique to the patch. The pattern from the design patch can be compared to the pattern from the scanned patch and provide a measure of the connectivity difference between the two layouts. We will refer to this measurement method as the KLayout Flow method.

We call the entry point from a patch the *input*, and the exit points from the patch the *outputs* for that input. Short or open circuits within a patch are noticed by finding extra or missing outputs for every input, respectively. Short and open circuits can also be combined in complex patterns, and accounted for using the same search method.

A benefit to using this method is that location information of each edge is preserved in the representation. Given the patches are correctly registered to one another, this location information reduces ambiguity between identical connection patterns.

In Fig. 5, an open circuit is present in a patch and highlighted by a red box. Each of the four inputs in the GDS2 are used to detect the open circuit. The Flow method iterates over the available inputs. It detects one missing output from input 1, and two missing outputs from input 2. The missing connections are highlighted in red. The other missing outputs are patterns already covered by input 1 and input 2 and are therefore ignored. The ignored discrepancies are illustrated in dark red. By counting the missing outputs, we observe the open circuit affected three unique connections within the patch.

Similarly another open circuit is presented and highlighted by a red box in Fig. 6. The open circuit affects more of the patch than before, bisecting a four-way junction. The four inputs are again used to measure the extent of the open. Input 1 detects two missing outputs, input 2 detects one missing output, and input 3 detects one additional missing output. By adding the missing outputs, we observe the open circuit causes four unique discrepancies. As expected, this open circuit is determined to be more extensive than the open circuit presented in Fig. 5.

The sensitivity of the Flow method provides valuable new insight into the connectivity difference between two GDS2 files. Modern tools reduce opens and shorts as much as possible, leading to an unquantifiable measurement. For example, if a short circuit were to occur between a series of parallel wires, it would be observed as a single short circuit by modern tools. In the Flow method, the short circuit is valued by how many new

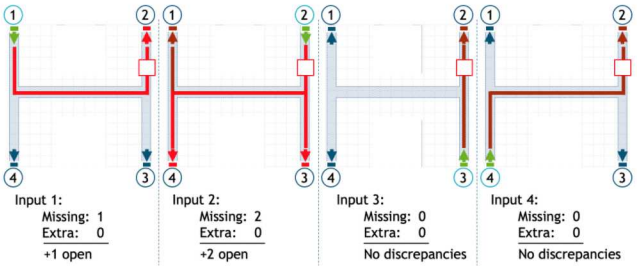

Fig. 5. KLayout Flow minor open circuit demonstration

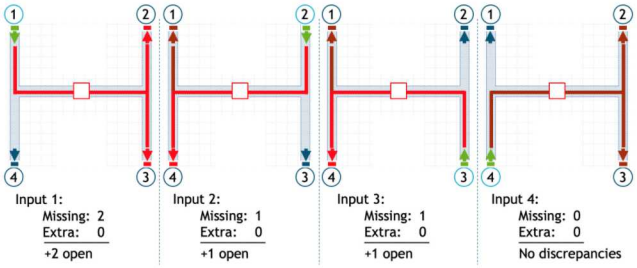

Fig. 6. KLayout Flow extensive open circuit demonstration

connections the short circuit introduced. Modern tools can mimic the sensitivity of the Flow method through methods such as PEX, however these methods quickly become too sensitive for our purposes. We will compare the capabilities of each method in the following section.

V. Results

Verification, validation, and sensitivity tests were performed to measure the capabilities of the Calibre and KLayout methods. Calibre test results were determined by running the LVS method and manually interpreting the results. KLayout test results were determined by performing the Flow method and using the metrics directly to measure connectivity differences. For the verification and validation tests, a 4-layer patch of size 12 µm x 48 µm was taken from a rudimentary circuit design. For the sensitivity tests, a 22-layer patch of size 30 µm x 78 µm was taken from a custom ASIC design providing typical circuit connections that pass Global Foundries design rule checks.

A. Verification tests

Seven verification tests were performed using the Calibre LVS method and the KLayout Flow method to detect connectivity differences. These tests contain very simple differences that should be easily detected. Both methods successfully detected all connectivity differences. The tests were as follows.

1) Design: No difference between either layout.

2) Internal metal: Removed metal internal to the patch that was not connected to the inputs of the patch. This test simulated benign noise in the scanned layout that did not change the circuit connectivity.

3) Floating metal: A portion of metal internal to the patch was removed. The metal was not connected to anything and its removal did not change the circuit connectivity.

4) Two shorts: Metal was shorted in the surface layer, creating two new connections.

5) Futile short: Metal was shorted in the bottom layer, however the metal was already connected in the surface layer.

6) Single open: Metal was opened along one extremity.

7) Multiple open: Metal along a three-way junction was opened, introducing two opens into the circuit.

B. Validation tests

Five validation tests were performed using the Calibre LVS method and the KLayout Flow method to detect connectivity differences. These tests were more complex than the verification test cases. They highlight the benefits to using one method over the other for particular cases. Table I shows whether each method passed or failed the validation test. The tests were as follows.

1) Short and open: One short and one open are combined in the surface layer. The KLayout Flow method detects the combination, but the Calibre LVS method does not detect the difference.

2) Missing input: An input is removed from the patch extremities. Internal connections are kept intact. Both methods detect the missing input.

3) Missing input and open: A missing input is combined with an open circuit. The Flow method detects the combination, but the LVS method only detects the missed input.

4) Missing input and short: A missing input is combined with a short circuit. Both methods detect the missing input and short circuit.

5) Duplicated input: One input along the edge of the patch is forked to result in two inputs. The Flow method fails to simplify this example into a single input, whereas the LVS method makes the connection.

C. Sensitivity tests

Two tests are presented for the Calibre PEX method. These tests are particular cases used to demonstrate the sensitivity of the PEX method. Table II shows the number of discrepancies produced by this method. The tests were as follows.

1) Hole in wire: The layouts are identical, however a hole is introduced into a section of wire in the scanned layout. The hole is in a location free of contact with other metal. If devices are not reduced after PEX, over 22,000 extra connectivity discrepancies are observed. This technique can be used as a very sensitive measure if all other methods detect no connectivity differences.

TABLE I. VALIDATION TEST RESULTS

Test #	Calibre LVS method	KLayout Flow method
1	Failed	Passed
2	Passed	Passed
3	Failed	Passed
4	Passed	Passed
5	Passed	Failed

TABLE II. CALIBRE PEX METHOD DISCREPANCIES

Test #	Without Reduction Step	With Reduction Step
1	22,725	0
2	461	13

2) Split via: The layouts are identical however a via becomes split in half, connecting the metal layers in two places instead of one. We perform this test to show that, although the connectivity of the circuit did not change, there were connection discrepancies present after maximal device reduction. Thirteen discrepancies remained after maximal reduction. The PEX method is therefore too sensitive to use in every situation.

D. Capability summary

The verification, validation, and sensitivity tests are categorized by capability and presented in Table III to give a summary of the capabilities of the Calibre and KLayout methods presented in this study. Both methods are capable of detecting simple differences in connectivity. The KLayout Flow method lacks the pattern-matching techniques that Calibre uses, whereas the LVS method cannot identify complex combinations of shorts and opens. The KLayout Flow method measures the extent of opens and shorts, whereas the LVS method does not.

The LVS and Flow methods can be used in tandem to improve the accuracy of connectivity difference measurements. The LVS method can be used when the patch inputs and outputs do not align and when there are forks in the inputs. The Flow method can be used when discrepancies are combined in complex ways and to give a measure of the extent of the present discrepancies.

The PEX method's hypersensitivity suggests it is capable of being used to measure the connectivity difference when the LVS and Flow methods detect no disparity. Its use of resistive and capacitive elements also suggests that PEX can be used to measure connectivity differences impacting areas of a circuit sensitive to electrostatic noise and interference.

VI. FUTURE WORK

The disparities of both the Flow method and LVS method presented in Section V.D can be improved. The Flow method can use circuit reduction techniques to recognize when there are extraneous inputs in the scanned layout, and use pattern recognition techniques to distinguish between inputs when they do not overlap the design layout. The LVS method would benefit from improved post-processing to provide a measure of the extent of opens and shorts in the layout.

TABLE III. CAPABILITY SUMMARY

Capability	Calibre LVS	KLayout Flow
Finds minute shorts and opens and basic differences in GDS	Yes	Yes
Measures extra inputs and outputs	Yes	Yes
Matches inputs/outputs that do not overlap each other	Yes	No
Simplifies discrepancies with input nodes	Yes	No
Supports 22-layer patch area greater than 4500 μm^2	Yes	No
Detects opens and shorts in complex scenarios	No	Yes
Measures the extent of opens and shorts	No	Yes

The tests performed in this work were designed to validate the methods introduced. They were not intended to characterize the methods in terms of performance. Further tests must be performed in order to determine the tradeoffs between either method. The circuit designs used were treated as arbitrary entities, however tests should be performed with a variety of circuit designs in the future.

GPU acceleration can be added to the KLayout software in order to boost performance. With improved memory management, the KLayout Flow method may be able to support a much larger circuit patch.

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