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Electro-thermal Simulation and Performance Comparison of 1.2 kV, 10 A Vertical GaN MOSFETs

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***Abstract*—With an increased interest in electric vehicles, significant effort has gone into the design of power electronic systems that are capable of handling large blocking voltages and high-power operation in smaller form factors. Because of its high electron mobility and large breakdown field, GaN has great potential to meet the demanding requirements of next generation electric vehicles. In this work, we perform electro-thermal simulations of two potential vertical metal-oxide-semiconductor field-effect transistor (MOSFET) device architectures that can achieve 1200 V blocking voltage and 10 A on-state operation. Results show that a planar device geometry exhibits reduced peak electric fields in the gate oxide allowing for design optimization to reduce device on-resistance, leading to lower power dissipation.**

Keywords—vertical GaN MOSFET; power devices; electro-thermal simulations

I. Introduction

Presently, commercially available gallium nitride (GaN) based power switching transistors are lateral high electron mobility transistor (HEMT) devices. Most of the commercial devices have targeted a voltage rating of 600-650 V, but recently devices with a breakdown rating of 900 V have become available [1]. While significant progress has been made to enable lateral devices capable of 900 V, there are still limitations in the lateral architecture. These limitations have primarily been due to the epitaxial growth of GaN on non-native substrates such as Si, which results in a high defect density, as well as non-uniform electric field distribution inherent in a lateral device layout. Furthermore, reliability concerns based on the quality of the GaN material and the lattice mismatched buffer layers needed to control strain in the device structure have caused manufacturers to de-rate device voltage capabilities significantly.

While bulk GaN substrates remain expensive, their commercial maturity is improving, and several groups are researching the development of fully vertical GaN transistors. Current devices are based on similar designs in more mature materials such as Si and SiC and aim to allow for increased blocking voltage and power handling capability in a reduced form factor. Two types of metal-oxide-semiconductor field-effect transistors (MOSFETs) that have been proposed for vertical GaN structures are the double-well MOSFET (D-MOSFET) and the trench-gate MOSFET (T-MOSFET).

In this work, we have performed electro-thermal simulations of both types of vertical structures using Silvaco ATLAS. Both devices are designed for 10 A forward current capacity with a blocking voltage of 1.2 kV. The impact of the gate dielectric material on electrical performance and design is evaluated for SiO_2, Al_2O_3, AlN, and SiN. We then set an electric field limit in the dielectric and compare the blocking voltage capabilities of both devices. We then look at the on-state operation and compare the thermal/electrical performance of each device while in DC operation at 10 A. Finally, the reduction in electrical current for each device is explored as a function of the junction-to-case thermal resistance in order to provide insight into potential device designs capable of achieving robust thermal performance while simultaneously maintaining desired electrical operation.

II. Device Design and Simulation Model

Device design and optimization for MOSFETs has been studied extensively in the literature [2-4]. Currently available commercial SiC power MOSFETs incorporate either the D-MOSFET or T-MOSFET design with each type having distinct advantages/disadvantages and manufacturing challenges. One of the primary concerns in either device is that of electric field management [5]. It is imperative to design a MOSFET such that it can obtain a high avalanche breakdown voltage without exceeding the breakdown strength of the dielectric between the gate and semiconductor material. Additionally, an elevated electrical resistance during the on-state will lead to unwanted power loss and device heating. Because of this, the reduction of the specific on-state resistance ($R_{on\text{-}spec}$) is also a primary design goal [6].

When designing a vertical GaN MOSFET, similar processes and goals as those for SiC MOSFETs can be incorporated. Figure 1 shows the simulated device layouts with relevant dimensions. Device dimensions were chosen based on a minimum lithography feature size of 2 μm, as will be used during the device development. Doping in the D-MOSFET was prescribed to be $5x10^{18}$ cm^{-3} in the N^+-source, $1x10^{18}$ cm^{-3} in the P-base, and $1x10^{16}$ cm^{-3} in the N-epilayer. The T-MOSFET had doping prescribed as $5x10^{18}$ cm^{-3} in the N^+-source, $1x10^{18}$ cm^{-3} in the P-base, and $8x10^{15}$ cm^{-3} in the N-epilayer. Looking at the gate dielectric, SiC devices have the distinct advantage of thermally grown SiO_2 layers that provide an excellent interface and electrical isolation. While there are still concerns about the oxide reliability due to large electric fields, it remains as the choice dielectric for SiC devices [7, 8]. GaN devices, however,

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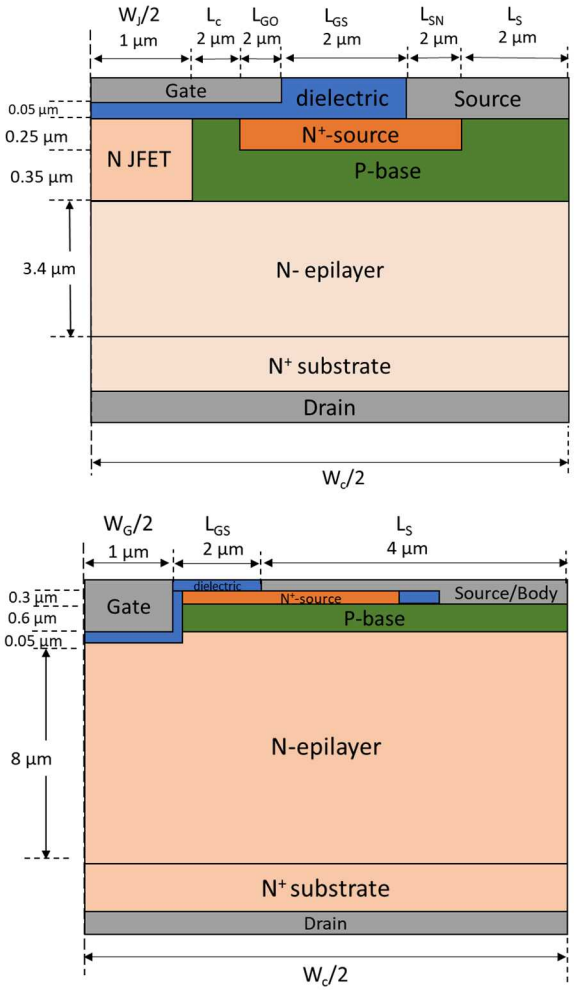

Figure 1: (Top) Half-cell of simulated D-MOSFET design. (Bottom) Half-cell of simulated T-MOSFET design.

must have a dielectric layer deposited, typically using a method of chemical vapor deposition (CVD) or an atomic layer deposition (ALD) process. GaN trench MOSFET devices found in literature have employed either metal-organic chemical vapor deposition (MOCVD) of Al_2O_3, or an SiO_2 ALD process [9, 10]. Four dielectric materials (SiN, SiO_2, Al_2O_3, and AlN) were considered for the initial device design. As shown in Figure 2, the dielectric constant has a large impact on both the threshold voltage and the electric field present in the dielectric. As expected, both the threshold voltage and electric field were inversely proportional to the dielectric constant [11]. In line with our previous work and capabilities [12], SiN was our chosen dielectric due to its relatively large relative permittivity (7.5) and high dielectric breakdown strength (10 MV/cm) [13]. A safety factor of 2.5 for dielectric breakdown was prescribed to ensure device reliability. For this reason, we considered device operational parameters such as gate voltage (V_G) and breakdown voltage (V_{BR}) to be limited such that the electric field in the SiN dielectric does not exceed 4 MV/cm.

Simulations were performed with Silvaco TCAD to determine the required epilayer doping and thickness to achieve a 1200 V breakdown condition in both devices. A coupled lattice heating model allowed for the examination of device thermal performance and power requirements necessary to achieve a 10 A on-state operational current. Relevant simulation values and parameters as developed in our previous work [14, 15] are given in Table 1.

TABLE 1
GAN SIMULATION PARAMETERS AND VALUES

Symbol	Quantity	Value
E_g	Bandgap	3.44 eV
ε_s	Relative Permittivity	9.7
T	Temperature	300 K
μ_p	Hole Mobility	11 cm^2/Vs
μ_n	Electron Mobility	1200 cm^2/Vs
k	Thermal Conductivity	$1.3\left(\frac{T}{300K}\right)^{-0.28}\frac{W}{cm\cdot K}$
R_{J-C}	Junction-to-Case Thermal Resistance	5 °C/W

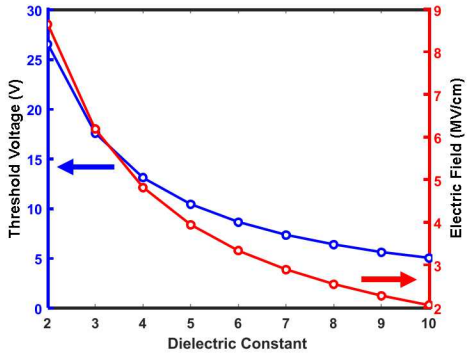

Figure 2: Threshold voltage and electric field as a function of the gate dielectric constant for a 50 nm thick layer. Electric field in the dielectric is estimated at 1200 V for a D-MOSFET device.

III. RESULTS

Both devices were successfully designed to achieve a 1200 V breakdown as shown in Figure 3. However, the D-MOSFET was able to sustain up to 1600 V without reaching the SiN E-

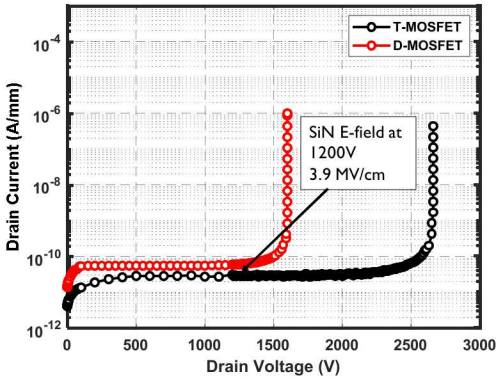

Figure 3: Comparison of device breakdown. The D-MOSFET was able to achieve 1600 V without exceeding the dielectric E-field limit, while the T-MOSFET exceeed the E-field limit at 1200 V.

field limit, while the T-MOSFET experienced significant field crowding at the trench corner. The D-MOSFET did show current crowding in the GaN material itself at the junction of the JFET, drift region, and p-base area. For a non punch-through design, this would lead to a large amount of impact ionization and create an avalanche breakdown condition in the device. The T-MOSFET had to be designed with a thicker epi-layer and lower epi-doping to sustain 1200 V blocking performance, while simultaneously not exceeding the 4 MV/cm E-field limit in the dielectric. Methods to control this field crowding in SiC devices, such as ion implantation to form a p-type layer underneath the gate oxide at the bottom of the trench, are not easily achieved in GaN, so they were not included in these simulations [16].

In forward operation, the field crowding also impacted the gate drive voltage. The peak electric field in the SiN dielectric is located at the corner of the trench in Figure 4. Because of the enhanced electric field crowding present in the trench device, the gate drive voltage was limited to 15 V such that the 4 MV/cm electric field requirement in the dielectric was not exceeded. Because the D-MOSFET is a planar device, the electric field in the on-state is a simple linear function of voltage and thickness and takes on a relatively uniform distribution as shown in Figure 5. For our chosen dielectric thickness of 50 nm this allows for the SiN to sustain a 20 V gate drive before exceeding the E-field dielectric limit. Figure 6 shows how the electric field in each of the devices scaled as a function of the gate drive voltage.

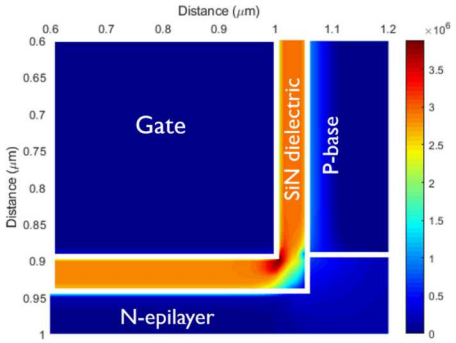

Figure 4: Electric field in T-MOSFET at the corner of the gate dielectric with a 15 V gate bias (V_{DS} = 1 V). Current crowding at the corner of the gate limits the gate drive potential. Colorbar is [V/cm].

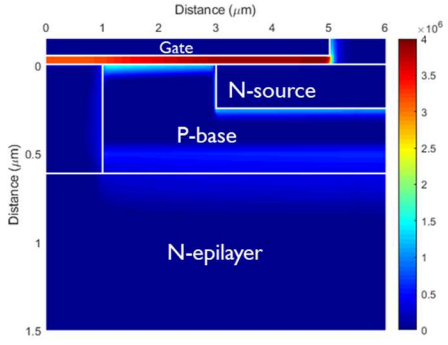

Figure 5: Electric field in D-MOSFET with a 20 V gate bias (V_{DS} = 1 V). The planar device exhibits a uniform electric field in the dielectric. Colorbar is [V/cm].

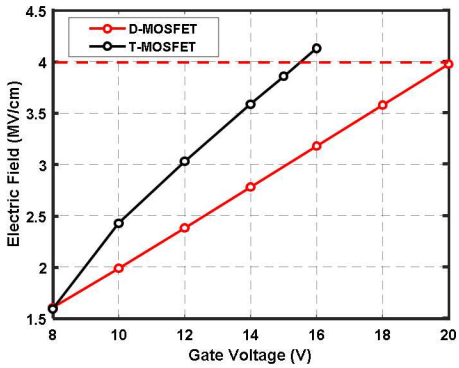

Figure 6: Comparions of device gate voltages as limited by the electric field in the SiN dielectric. Field crowding at the corner of the T-MOSFET limited the gate voltage to only 15 V as compared to 20 V in the D-MOSFET.

The appropriate gate width to achieve 10 A operation in the on-state was investigated. It was found that for both devices, a 10 cm gate width was sufficient to sustain the 10 A current in the linear region of device operation. This is in line with previous reports. Gupta *et al.* reported on a vertical GaN T-MOSFET in which a 14 cm gate would be required to achieve 10 A operation [17]. Additional trench devices as reported by Oka *et al.* demonstrate 10 A operation and 1.2 kV blocking voltages for a chip area of 1.5 mm x 1.5 mm, however, they do not impose any restrictions on the electric field in their dielectric and operate the gate drive voltage up to 40 V. In this current work, the T-MOSFET device had twice the power dissipation and therefore almost twice the temperature rise for the same current capacity as the D-MOSFET design. Figure 7 shows IV curves for both devices considering a 10 cm gate width and a 20 V and 15 V gate drive for the D-MOSFET and T-MOSFET, respectively.

As the power density of electronic devices continues to increase, it becomes increasingly important to implement thermal/electrical co-design requirements from the device inception. Here we have included a coupled electrical/thermal model in the device design in order to observe the impact of thermal resistance on device self-heating and reduction in carrier mobility. All previous results reported in this work considered a 5 °C/W thermal resistance prescribed at the base of the simulation. This value is on the high end of what has been

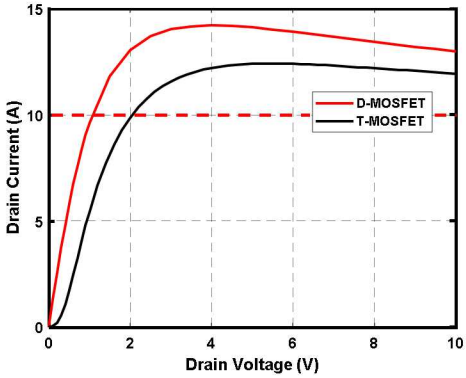

Figure 7: IV curves for both devices with a 10 cm gate width.

reported in literature for a junction-to-case thermal resistance [18]. It was found that in order to achieve a 10 A operation the D-MOSFET required 10 W power dissipation resulting in a 48 °C temperature rise, while the T-MOSFET required twice the power dissipation at 20 W, resulting in a 92 °C temperature rise. This considers a situation where the case of the device can maintain the ambient temperature. In practical applications, the devices will incur additional thermal resistances beyond the case that will extend to the ambient environment or to an active cooling solution (Fig. 8).

From a design standpoint, thermal operating limitations are placed on a device such that the device temperature does not exceed a specified value, typically 150 °C. If a 25 °C operating environment is assumed, the additional case-to-ambient thermal resistance that is acceptable in order to maintain the temperature requirement can be estimated by examining the relationship between temperature, power, and thermal resistance. As shown in Figure 9, the D-MOSFET device, which has a 10 W power dissipation at 10 A, is able to sustain an additional thermal resistance of 7.5 °C/W before exceeding the 150 °C limit, where the T-MOSFET device, with a power dissipation of 20 W at 10 A, can only sustain an additional 1 °C/W thermal resistance. In these cases, the T-MOSFET would require a much more sophisticated cooling solution, most likely requiring an active cooling loop to maintain temperature operation.

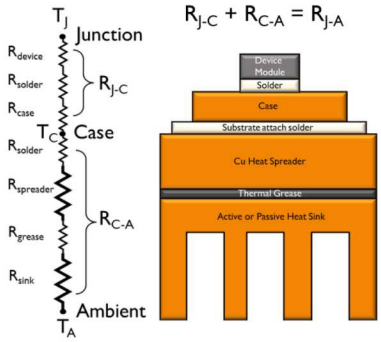

Figure 8: Schematic of typical thermal resistances found in device stacks from device to final thermal solution.

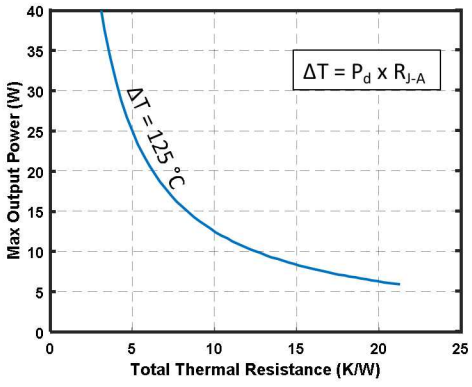

Figure 9: Maximum power output vs. total thermal resistance considering an ambient environment of 25 °C and temperature operating limit of 150 °C .

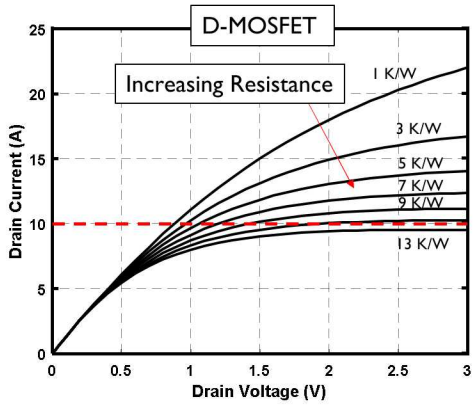

Figure 10: D-MOSFET IV characteristics with increasing thermal resistance.

Additionally, it was found that an iterative approach was necessary to fully understand thermal limitations. This was due to the increased temperature rise impacting carrier mobility and scattering mechanisms, thereby resulting in a reduced current carrying capability. Figure 10 demonstrates how an increase in thermal resistance can cause a significant reduction in the device's current capacity.

IV. Conclusions

It was found that both device designs could achieve the off and on-state requirements of 1.2 kV blocking voltage and 10 A current capability, however, the T-MOSFET design experienced electric field crowding at the corner of the trench, resulting in a thicker drift region and lower doping to maintain the specified 4 MV/cm electric field requirement in the dielectric. Additionally, the field crowding limited the gate drive voltage to 15 V in the T-MOSFET as compared to 20 V in the D-MOSFET. For the same gate width of 10 cm in each device, this resulted in a power dissipation at 10A of 10 W and 20 W for the D-MOSFET and T-MOSFET, respectively. The additional power dissipation in the T-MOSFET design was shown to greatly restrict the package design due to 7x less thermal resistance allowed in order to maintain an operating temperature of 150 °C as compared to the D-MOSFET design. These initial simulation results will help to guide the design of actual devices from both an electrical and thermal perspective, such that the fabricated devices can best meet the design requirements with reliable operation.

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