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LIQUID-COOLED HEAT SINK OPTIMIZATION FOR THERMAL IMBALANCE MITIGATION IN WIDE-BANDGAP POWER MODULES

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ABSTRACT

Power semiconductor die layout in substrates used in power modules is generally optimized for minimum electrical parasitics (e.g., stray inductance) by considering the minimum spacing between dies for thermal decoupling. The layout assumes sufficient heat spreading and transfer from dies to the cooling structure. For module designs using a direct substrate cooling method, the base plate is removed, leading to a steady-state thermal asymmetry in the power module due to insufficient heat spreading/transfer. This causes significant temperature differences among the devices. Such unintentional thermal asymmetries can lead to undesirable asymmetries in power conversion among semiconductor devices, which impact reliability. This article proposes a thermal imbalance mitigation method that uses evolutionary optimized liquid-cooled heat sinks to improve the thermal loading among devices.

NOMENCLATURE

FE finite element
GA genetic algorithm
GaN gallium nitride
IMS insulated metal substrate
SiC silicon carbide
TPG thermal pyrolytic graphite
WBG wide-bandbap

INTRODUCTION

In high–power density automotive applications, thermal management of the power module is provided by liquid-cooled heat sinks to ensure manufacturer-specified operation of the semiconductor devices [1, 2]. In the process of continuous improvements in transportation electrification, the potential for power conversion density increment in power modules is being widely studied for highly integrated drivetrain development [2, 3]. Wide-bandgap (WBG) semiconductor devices, such as silicon-carbide (SiC) metal oxide semiconductor field effect transistors (MOSFETs) and gallium-nitride (GaN) high–electron-mobility transistors, offer efficient power conversion compared with their Silicon counterparts. They help improve the efficiency of the system, thereby allowing increased power conversion density. However, WBG devices still exhibit power losses and excess heat in small volumes, leading to bottlenecks in reducing the module volume [2,3]. Hence volume reduction and optimization of the cooling system is necessary; and optimization-based design methods have been proposed in the literature, including gradient/hessian as well as evolutionary optimization-based methods [4–9].

While advances in power conversion density are desired, it is also important to have the semiconductor devices in the power module operate uniformly with respect to one another [2, 3]. One aspect of uniformity is the observed thermal impedance by semiconductor chips in a module. In the absence of sufficient heat spreading or transfer in advanced power module packaging schemes, individual semiconductor devices experience differences in the thermal impedance offered by the cooling system [3]. For steady-state operation, such thermal impedance imbalances lead to significant temperature differences among the devices [3].

Various heat sink designs have been adopted for liquid-cooled heat sinks in which the heat sink is immersed in the coolant for efficient heat transfer from the substrate to the coolant. Some conventional designs used in commercial heat sinks are pin-fin and straight-fin [10, 11]. These conventional designs are tailored for uniform and high heat transfer performance across the contact surface with minimum pressure drop across the coolant. However, these designs do not account for thermal imbalances occurring in the power semiconductor dies. Semiconductor device properties are closely related to their operating temperatures. Imbalances in thermal resistance or steady-state temperature lead to asymmetry in power conversion among devices; that is, a few devices will provide more power conversion than others. This power conversion asymmetry may lead to reliability issues or underutilization of semiconductor devices to avoid thermal issues [12]. Hence, unconventional heat sink designs are required which not only allow for balanced thermal operation of the semiconductor devices but also maximize the power conversion density.

For such designs, this paper proposes a thermal imbalance mitigation method that uses evolutionary optimization algorithms for designing liquid-cooled heat sinks. The heat sink structure is optimized for the targeted substrate so that the steady-state temperature imbalance among devices is minimized as the power conversion density of the module is maximized. To accomplish this, the optimization engine uses a Fourier-series–based heat sink representation scheme to consider unconventional heat sink structures that are not available in the literature. The optimization procedure then uses population-based evolutionary algorithms to optimize the geometry for specified objectives while satisfying imposed constraints. The optimization-based design process for the proposed method is shown in Figure 1.

HEAT SINK GEOMETRICAL REPRESENTATION

To optimize the heat sink geometry, first, it is necessary to be able to mathematically represent the geometry. The optimization engine will therefore use a mathematical representation to determine the best possible design/s that fulfill its requirements. In this paper, it is assumed that the heat sink geometry does not change along the direction of coolant flow. Thus, the geometry needs to represented for the 2D cross-section in the optimization engine and will be extended along its length for computational finite element (FE) analysis.

In the available heat sink geometry representations [9,13], in this article, the heat sink coolant contact surface was considered to be composed of Fourier-series terms as [13]

$$F_{hs}(x) = H_0 + \sum_{n=1}^{N_{hs}} \left(A_h[n] \cos\left(\frac{2\pi}{\lambda_x} h[n]x + \phi_h[n] \right) \right), x \in [0, W_x] \tag{1}$$

where $F_{hs}(x)$ is the height of the heat sink fin at each position x with respect to axis $F_{hs}(x) = 0$ (x varying between 0 and width W_x); H_0 is a constant (DC) shift; λ_x is the wavelength (which is also equal to W_x); $h[n]$ is the harmonic order and $A_h[n]$ and $\phi_h[n]$ are its corresponding amplitude and phase shift, respectively; and N_{hs} is the total number of harmonics considered. For example, consider the heat sink shown in Figure 2 located between $x = 0$ and 1. The structure is composed of $H_0 = 0.5$, harmonic orders $h = [4,\ 10]$ with their respective $A_h = [0.1,\ 0.2]$ and $\phi_h = [\pi/2,\ \pi/3]$.

For the optimization engine, the variables in Eq. (1) constitute the design space of the heat sink geometry and are optimized for the best solution/s. In the next section, a thermal imbalance

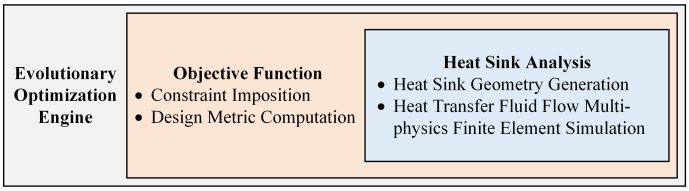

FIGURE 1. OPTIMIZATION-BASED DESIGN PROCESS

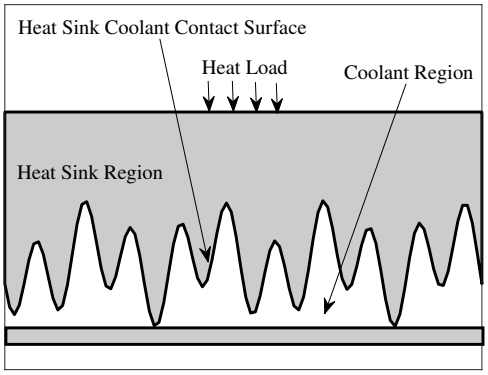

FIGURE 2. EXAMPLE HEAT SINK FOR $H_0 = 0.5$, $h = [4,30]$, $A_h = [0.1,0.2]$, $\phi_h = [\pi/2,\pi/3]$.

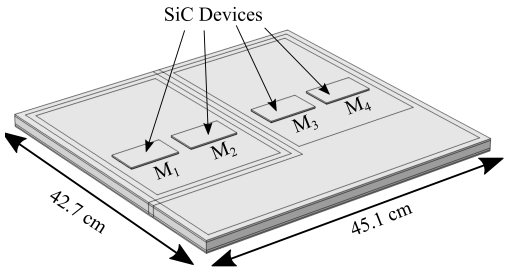

FIGURE 3. SiC-BASED WBG HALF-BRIDGE POWER MODULE

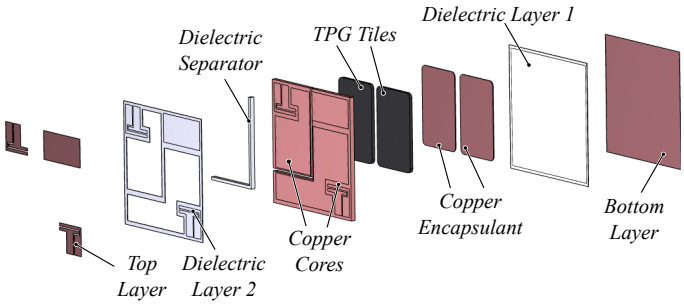

FIGURE 4. EXPANDED VIEW OF THE SUBSTRATE [14]

problem is described which will require this heat sink representation for its optimization.

STEADY-STATE THERMAL IMBALANCE

The power module substrate structure considered is shown in Figure 3 and an expanded view of its substrate in Figure 4 [14]. As shown in Figure 3, four SiC devices are placed on a graphite-embedded insulated metal substrate (IMS) to create the half-bridge module shown in Figure 5. The graphite-embedded structure proposed in ref. [14] can provide up to a 17% improvement in steady-state thermal resistance and 40% improvement in transient impedance compared with a conventional AlN-based direct-bonded copper (DBC) substrate. The IMS incorporated a 152 μm thick dielectric for isolation of the graphite-embedded copper cores from the heat sink. The SiC MOSFET dies were placed on individual copper cores, separated by the dielectric separator, to form the half-bridge circuit presented in Figure 5. An additional top layer, separated by a 152 μm thick dielectric material, was used to accommodate gate-source terminals and a DC terminal. SiC MOSFET dies from CREE CPM3-1200-0013A rated at 1200 V 13 mΩ were used. The power loss in each die at 71 A is approximately 87 W for a 140 A RMS current rating at the output of the substrate.

The steady-state thermal performance of the considered power module was simulated using 3D FE simulations at the considered power level. To represent conventional cold-plate performance, a uniform heat-transfer coefficient of 5000 W/m^2/K was

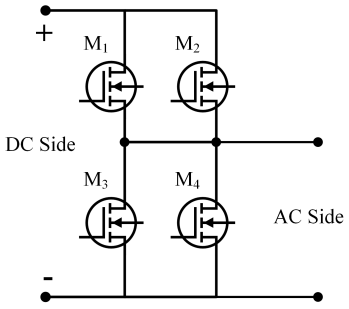

FIGURE 5. POWER MODULE ELECTRICAL CIRCUIT

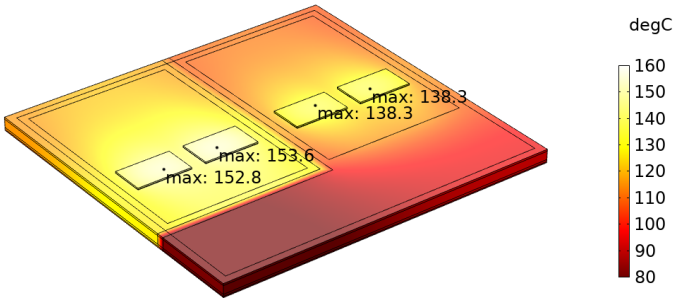

FIGURE 6. 3D FEA SURFACE TEMPERATURE SOLUTION

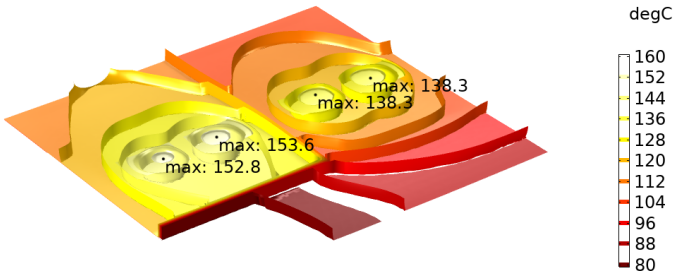

FIGURE 7. ISOTHERMAL CONTOURS IN WBG MODULE

set as the boundary condition at the bottom-most plate of the substrate with a 65°C coolant temperature [3]. The results of the FE simulations are presented in Figures 6 and 7 wherein it can readily be seen that the devices in the upper half of the half-bridge (dies M_1 and M_2) have significantly higher temperatures than those in the lower half (dies M_3 and M_4). The temperature difference is nearly 15°C. Similar conclusions were presented in [3], wherein it was shown that the devices in an IMS-based layout had different thermal impedances as a result of the inherent structure of the module.

To resolve the thermal imbalance, this paper proposes a mitigation scheme in which the cooling system formed by the optimized heat sink and coolant compensates for the difference in

thermal impedance observed by the semiconductor dies. That is, for the heat sink developed by the optimization engine, the steady-state thermal resistances between the die junction and the coolant observed by each die are nearly equal. For such an exercise, a problem statement must first be mathematically defined for the optimization algorithm.

Consider the power module shown in Figure 3 operating at a continuous peak-rated power loading condition with an arbitrarily designed cooling system. At this loading condition, the device temperatures are computed using FE simulations for the applied cooling. Next, the thermal loading of each chip is increased by the factor $\alpha_{hl} > 1$ while the same cooling system is retained, and the new die temperatures are computed. The incremental thermal resistance of each die is then defined as

$$R_{th,inc,\xi} = \frac{T_{j,max,\alpha_{hl},\xi} - T_{j,max,1,\xi}}{(\alpha_{hl}-1)P_{cw,\xi}} \tag{2}$$

where $\xi \in \{\mathrm{M}_1, \mathrm{M}_2, \dots\}$ are the dies on the power module, $T_{j,max,\alpha_{hl},\xi}$ is the maximum die temperature at α_{hl} factor power load, and $P_{cw,\xi}$ is the continuous worst-case rated power loading condition for die ξ. Next, the imbalance in the steady-state thermal resistance $R_{th,im}$ is defined as

$$R_{th,im} = \max_{\xi}(R_{th,inc,\xi}) - \min_{\xi}(R_{th,inc,\xi}) \tag{3}$$

To minimize the steady-state thermal imbalance, an optimization problem is formulated to minimize $R_{th,im}$ over the generated heat sink designs. The optimization engine finds appropriate Fourier-series variables that minimize the difference in thermal impedance. For the execution, an optimization problem is then formulated.

FORMULATION OF OPTIMIZATION PROBLEM

Using the mathematical definition of thermal imbalance, an optimization problem was developed. In this article, heat sink design was carried out for a given power module layout structure for a given maximum current rating or maximum heat loading. In subsequent subsections, first the variables or design space for the problem are defined. Next, some constraints are imposed on the heat sink design to satisfy various properties (e.g., maximum allowed junction temperature). Finally, the design metrics of interest and a fitness function are defined, which can be used by the optimization engine of interest.

Design Space

Recall that in Eq. (1), the heat sink geometry is represented as being composed of a combination of harmonic geometries and a DC constant H_0. For a given current load (or heat load), module layout, coolant parameters, flow rate, and heat sink material parameters, the design variable vector (or geometrical design vector) $\boldsymbol{\theta}_\mathbf{g}$ is given by

$$\boldsymbol{\theta}_\mathbf{g} = [\ \underbrace{H_0}_{\text{DC Shift}}\ \underbrace{h[1]\,h[2]\dots h[N_{hs}]}_{\text{Harmonic Orders}}\ \underbrace{A_h[1]\,A_h[2]\dots A_h[N_{hs}]}_{\text{Harmonic Amplitudes}}\ \underbrace{\phi_h[1]\,\phi_h[2]\dots\phi_h[N_{hs}]}_{\text{Harmonic Phase Angles}}\ ] \tag{4}$$

The length of the $\boldsymbol{\theta}_\mathbf{g}$ vector is $(3N_{hs}+1)$. The limits on each element in $\boldsymbol{\theta}_\mathbf{g}$ are determined from the limits on the maximum allowed height and volume constraints.

Along with the variable vector, few fixed parameters are stored in vector $\mathbf{D}$ as

$$\mathbf{D} = [\mathbf{M_{fp}} \quad \mathbf{C_{fp}} \quad \mathbf{S_{cp}}], \tag{5}$$

where $\mathbf{M_{fp}}$ contains all the fixed parameters of the power module layout and its current loading; $\mathbf{C_{fp}}$ contains all the fixed parameters of the cooling system such as coolant parameters, flow rate, and material parameters; and $\mathbf{S_{cp}}$ contains all the constraint parameters for the design, such as limits on the maximum junction temperature and maximum coolant temperature rise.

Design Constraints

A few constraints are imposed on the heat sink design to assist the optimization engine in discarding solution search spaces that either do not yield to physically viable designs or fail to fulfill the design criteria.

The first constraint imposed was on the uniqueness of the harmonic selection. That is, the vector h in $\boldsymbol{\theta}_\mathbf{g}$ should contain unique elements

$$h[n_1] \neq h[n_2], \forall (n_1,n_2) \in \{1,2,\dots N_{hs}\}, n_1 \neq n_2. \tag{6}$$

In other words, an inequality constraint can be imposed so that

$$\text{unique}(h) \geq N_{hs}\,, \tag{7}$$

where unique$(\cdot)$ computes the number of unique elements in a vector. Note that in equation (7), unique elements in h will always be less than or equal to N_{hs} because the number of elements in h equals N_{hs}. A greater-than-equal-to inequality was imposed, keeping population-based evolutionary optimization algorithms in mind because they generally face difficulties in convergence

with equality constraints [15]. Next, a constraint on the height of the heat sink H_{hs} was imposed so that

$$H_{hs} = (\max(F_{hs}) - \min(F_{hs})) \leq H_{ht,max}\,, \tag{8}$$

where $H_{ht,max}$ is the maximum allowed heat sink height. For a given module layout, this constraint also limits the maximum value of the allowed volume.

The next set of constraints were imposed on the solution of the heat sink FE simulation. In this formulation, it was assumed that the fluid flow was fully developed laminar to reduce the FE analysis computational time in an optimization environment where thousands of simulations may be carried out. For that assumption, a constraint was imposed so that the Reynolds number of the fluid flow solution $R_{N,hs}$ was below the maximum threshold [7]:

$$R_{N,hs} \leq Re_{max}\,. \tag{9}$$

Next, to limit the semiconductor temperature, a constraint was imposed on the maximum device temperature,

$$\max_{\xi}(T_{sic,\xi}) \leq T_{sic,max}\,, \tag{10}$$

where $T_{sic,\xi}$ is the device temperature ξ and $T_{sic,max}$ is the maximum allowed SiC chip temperature from the manufacturer data sheet. Next, the fluid pressure drop across the heat sink $P_{drop,hs}$ was constrained using

$$P_{drop,hs} \leq P_{drop,max}\,. \tag{11}$$

Finally, the change in coolant inlet and outlet surface average temperature was constrained by

$$\overline{T_{c,out}} - \overline{T_{c,in}} \leq \delta_{T,c,max}\,, \tag{12}$$

where $\overline{T_{c,in}}$ and $\overline{T_{c,out}}$ are the surface average coolant temperatures at the inlet and outlet, respectively, and $\delta_{T,c,max}$ is the maximum allowed change in coolant temperature.

Design Metrics

As discussed, it is desirable to maximize the power density of the module as well as minimize the imbalance in thermal resistance. The maximum allowed current rating of the devices was known before the optimization; hence maximizing power density inherently became an exercise in minimizing the power module volume V_{pm}. Power module volume with a heat sink is computed as

$$V_{pm} = W_{pm} \cdot L_{pm} \cdot (H_{pm} + H_{hs})\,, \tag{13}$$

where H_{pm} is the thickness of the power module layout including the SiC devices and substrate, and W_{pm} and L_{pm} are the width and the length of the power module, respectively. For reference, in Figure 3, $W_{pm} = W_x = 45.1$ mm and $L_{pm} = 42.7$ mm. Next, the thermal resistance metric $R_{th,im}$ was computed using Eqs, (2) and (3) after FE simulation of the module.

Optimization Engine and Design Fitness

Among the available evolutionary optimization algorithms, genetic algorithms (GAs) are widely used and are of interest for topology optimization problems [7–9, 13]. In contrast to a derivative-based optimizer, GAs do not require derivative/hessian computations and are generally immune to converging at nonglobal local extrema [15]. In this work, the GA-based tool GOSET was used as the optimization engine [16].

In accordance with the selected optimization engine, the design fitness functions were defined as [15, 16]

$$\mathrm{f} = \begin{cases} \varepsilon \begin{bmatrix} 1 & 1 \end{bmatrix}^T \left(\dfrac{C_s - N_c}{N_c} \right) & C_s < C_I \\ \left[\dfrac{1}{R_{th,im}} \quad \dfrac{1}{V_{pm}} \right]^T & C_s = C_I \end{cases}, \tag{14}$$

$$C_s = \sum_{i=1}^{N_c} c_i\,, \tag{15}$$

where N_c, C_s, and C_I are the total number of constraints, number of constraints satisfied, and number of constraints imposed during the evaluation of the objective function, respectively; c_i is the i^{th} constraint; and ε is a small positive number of the order 10^{-6}.

Computation of c_i is done such that if it is a less-than-equal-to constraint of form $x \leq x_{mx}$ [15, 16],

$$c_i(x, x_{mx}) = \begin{cases} 1 & x \leq x_{mx} \\ \dfrac{1}{1 + x - x_{mx}} & x > x_{mx} \end{cases}; \tag{16}$$

otherwise, for a greater-than-equal-to constraint of form $x \geq x_{mn}$ [15, 16],

$$c_i(x, x_{mn}) = \begin{cases} 1 & x \geq x_{mn} \\ \dfrac{1}{1 + x_{mn} - x} & x < x_{mn} \end{cases}. \tag{17}$$

If constraint i is satisfied, $c_i = 1$; otherwise, $c_i < 1$. If all the constraints are not satisfied, the objective function will yield a small negative number from Eqs. (14) and (15). Otherwise, the inverse of the design metrics will be calculated in Eq. (14). These forms of constraint and fitness functions are advantageous for optimization-based design, as explained in [15]. Using GOSET, the fitness function defined in (14) is maximized [16].

CASE STUDY AND RESULTS

To demonstrate the application of the developed design paradigm, a case study was developed using the power module structure described in Figure 5, with the same parameters and current load used for simulation in Figures 6 and 7. As discussed, the GA was used for the heat sink design optimization.

The fixed design parameters for this case study are shown in Table 1 [3]. Aluminum was selected as the heat sink material. It was cooled using a 50–50% water–ethylene glycol mixture supplied at a 10/6 l/min flow rate and 65°C temperature [3]. To contain the coolant, it was assumed that plates of 0.5 mm thickness were attached to two sides and the bottom of the heat sink. The variable design space considered for this study is presented in Table 2, wherein the number of harmonics considered N_{hs} equaled 10, $n \in \{1, 2, \ldots N_{hs}\}$, and $h[n]$ was an integer.

COMSOL Multiphysics was used to carry out the FE analysis. It interacts with GOSET in MATLAB to create heat sinks, simulate, and report simulation results. GOSET carried out the GA operations, whereas COMSOL was responsible for computing fluid flow and heat transfer performance. As the maximum temperature rise of the coolant was constrained to be less than 5°C, the fluid flow and heat transfer mechanisms were assumed to be weakly coupled to speed up the computational performance of the FE analysis.

In this case study, GA optimization was carried out using a population of 40 for 40 generations. The results of the constrained multiobjective optimization are shown in Figure 8, wherein red-circled data represent the Pareto-optimal front of the designs and blue stars represent the feasible designs considered by the GA over the course of the optimization. Note that feasibility of the design requires that it satisfy all the imposed constraints. The Pareto-optimal fronts of the designs have a total volume V_{pm} between 12 and 13 cm^3 with thermal imbalance $R_{th,im}$ between 0.008 and 0.044 K/W.

Of the designs on the Pareto-optimal front, a design with 12.65 cm^3 volume and 0.015 K/W $R_{th,im}$ was selected, as shown in Figure 8. The harmonic orders and their amplitudes are shown in Figure 9, wherein "0" is the DC shift and harmonics orders greater than 0 represent the composition of the fin structure immersed in the coolant liquid. The cross-sectional structure of the selected heat sink is shown in Figure 10. The total height of the heat sink is 4.27 mm. As can be seen, the DC shift is nearly one fourth of the total heat sink height. The majority of the fin harmonics lie between orders 50 and 60, with small first and 17$^{\text{th}}$ orders.

TABLE 1. FIXED DESIGN PARAMETERS

Parameter	Value	Parameter	Value
W_{pm}	45.1 mm	L_{pm}	42.7 mm
H_{pm}	1.76 mm	$H_{ht,max}$	14 mm
$P_{drop,max}$	13 kPa	Flow rate	(10/6) l/min
Re_{max}	1900	α_{hl}	1.1
$P_{cw,\xi}$	87 W	$T_{sic,max}$	130°C
$\overline{T_{c,in}}$	65°C	$\delta_{T,c,max}$	5°C
Heat sink	Aluminium	N_{hs}	10
Coolant	Water-glycol 50%	N_c	6

TABLE 2. DESIGN SPACE

Parameter	Description	Min.	Max.
H_0	Constant DC shift	0.5 mm	5 mm
$h[n]$	n^{th} harmonic order	1	100
$A_h[n]$	n^{th} harmonic amplitude	0 mm	$H_{ht,max}$
$\phi_h[n]$	n^{th} harmonic phase angle	0	2π

As a result of this harmonic combination, the fin height in the left half of the optimized heat sink cross-section is higher than that in the right half, as presented in Figure 10. As shown earlier in Figure 6, the semiconductor dies in the left half of the substrate have higher thermal resistance because of the layout structure. Hence, the GA optimized the heat sink to provide higher heat transfer for devices M_1 and M_2 compared with M_3 and M_4.

To demonstrate this effect, the FE analysis results for the selected heat sink design are shown in Figures 11, 12, and 13. As presented in Figures 11 and 12, the optimized heat sink significantly reduced the steady-state imbalance between the die temperatures while keeping the junction temperature below 125°C. Comparing the isothermal contour results in Figures 7 and 12, the optimized heat sink provides uniform heat spreading for both sections (upper half and lower half) of the power module. Finally, the pressure drop across the coolant in the flow is shown in Figure 13, which shows that it is substantially below the imposed constraint.

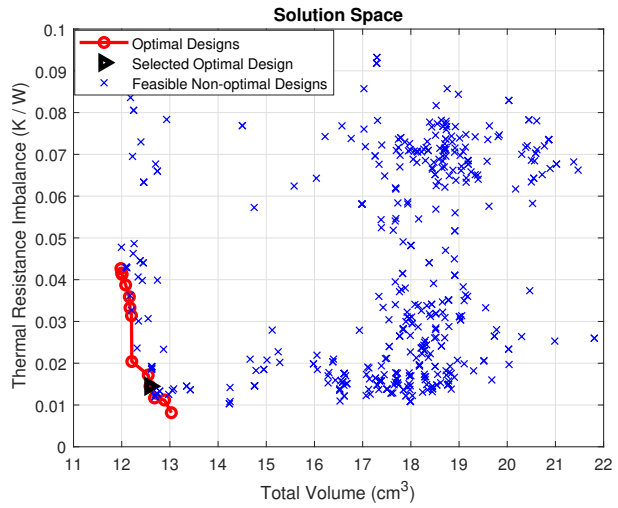

FIGURE 8. DESIGN SOLUTION SPACE

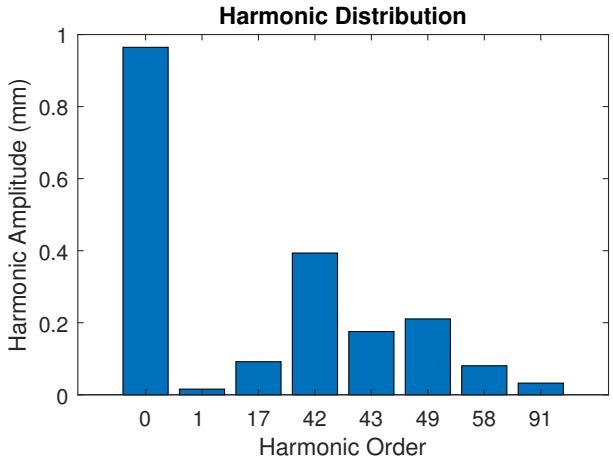

FIGURE 9. SPATIAL HARMONIC DISTRIBUTION IN SELECTED DESIGN

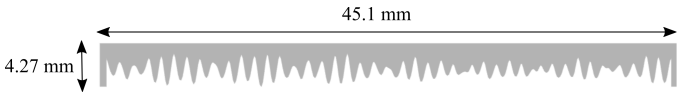

FIGURE 10. SELECTED HEAT SINK DESIGN CROSS-SECTION

CONCLUSIONS AND FUTURE WORK

In this article, an evolutionary algorithm-based topology optimization design paradigm for liquid-cooled heat sinks is presented for application-specific goals and targets. Improvement of the power density of the module and balanced steady-state thermal performance for each die are the two goals of this effort. The article presents a constrained multiobjective optimization-based design method to develop appropriate heat sinks for application.

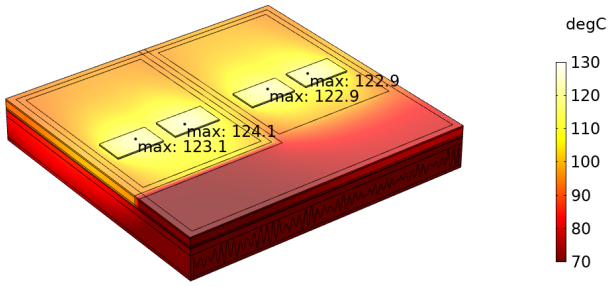

FIGURE 11. SELECTED HEAT SINK SURFACE TEMPERATURE DISTRIBUTION

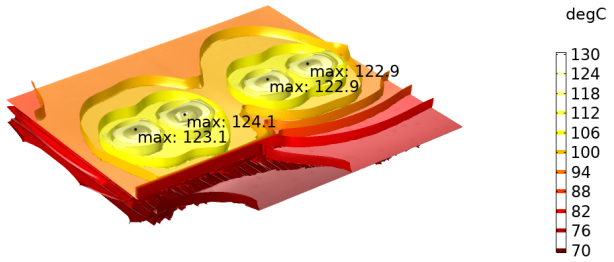

FIGURE 12. SELECTED HEAT SINK ISO-THERMAL CONTOURS

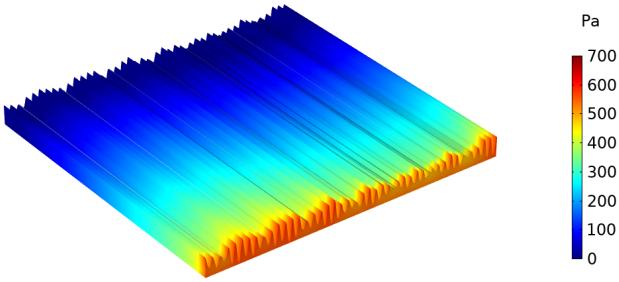

FIGURE 13. SELECTED HEAT SINK COOLANT PRESSURE DROP DISTRIBUTION

It was shown using 3D FE simulations that the GA-designed heat sink indeed mitigates unwanted thermal imbalances by creating a suitable heat sink surface as well as reducing the overall volume of the cooling system. Results from the design optimization demonstrate the effectiveness of the proposed approach.

While the article opens up an interesting design paradigm for custom-made, application-specific heat sink designs for maximum power density, some work remains to be done. As an initial step, extensive hardware validation of the proposed heat sink design is planned. Wire electrical discharge machining can create suitable complex geometries without the need to explore additive manufacturing or 3D printing options. The next step will be to

consider the transient thermal characteristics of the heat sinks. Finally, cost-effective, high- volume manufacturing of such heat sink designs will be explored.

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REFERENCES

[1] U.S. DRIVE Electrical and Electronics Technical Team Roadmap. https://www.energy.gov/eere/vehicles/downloads/us-drive-electrical-and-electronics-technical-team-roadmap.

[2] Gurpinar, E., Wiles, R., Ozpineci, B., Raminosoa, T., Zhou, F., Liu, Y., and Dede, E. M., 2018. "Sic mosfet-based power module design and analysis for ev traction systems". In 2018 IEEE Energy Conversion Congress and Exposition (ECCE), pp. 1722–1727.

[3] Gurpinar, E., Ozpineci, B., and Chowdhury, S. "Design, analysis and comparison of insulated metal substrates for high power wide-bandgap power modules". In 2019 ASME InterPACK.

[4] Zeng, S., et al., 2018. "Experimental and numerical investigation of a mini channel forced air heat sink designed by topology optimization". *International Journal of Heat and Mass Transfer,* ***121***, pp. 663–679.

[5] Dede, E. M., et al., 2015. "Topology Optimization, Additive Layer Manufacturing, and Experimental Testing of an Air-Cooled Heat Sink". *Journal of Mechanical Design,* ***137***(11), 10.

[6] Sun, S., Liebersbach, P., and Qian, X., 2019. "Large scale 3d topology optimization of conjugate heat transfer". In 2019 18th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm), pp. 1–6.

[7] Wu, T., et al., 2017. "Design and optimization of 3d printed air-cooled heat sinks based on genetic algorithms". In 2017 ITEC, pp. 650–655.

[8] Ge, Y., et al., 2019. "Optimal shape design of a minichannel heat sink applying multi-objective optimization algorithm and three-dimensional numerical method". *Applied Thermal Engineering,* ***148***, pp. 120–128.

[9] Dokken, C., et al., 2018. "Optimization of 3d printed liquid cooled heat sink designs using a micro-genetic algorithm with bit array representation". *Applied Thermal Engineering,* ***143***.

[10] Suganuma, K., 2018. *Wide Bandgap Power Semiconductor Packaging: Materials, Components, and Reliability*. Woodhead Publishing.

[11] Sakanova, A., and Tseng, K. J., 2018. "Comparison of pin-fin and finned shape heat sink for power electronics in future aircraft". *Applied Thermal Engineering,* ***136***, pp. 364 – 374.

[12] Ma, K., Bahman, A. S., Beczkowski, S., and Blaabjerg, F., 2015. "Complete loss and thermal model of power semiconductors including device rating information". *IEEE Transactions on Power Electronics,* ***30***(5), pp. 2556–2569.

[13] R. Sahu and E. Gurpinar, and B. Ozpineci, 2020. Fourier Analysis-based Evolutionary Optimization of Liquid-cooled Heat Sinks. Accepted for publication in IEEE ECCE 2020, October 11-15.

[14] Gurpinar, E., Chowdhury, S., Ozpineci, B., and Fan, W. "Graphite embedded high performance insulated metal substrate for wide-bandgap power modules". *IEEE Transactions on Power Electronics*. Accepted for publication in IEEE TPEL 2020.

[15] Sudhoff, S. D., 2014. *Power Magnetic Devices: A Multi-Objective Design Approach*. IEEE, ch. Optimization-Based Design, pp. 1–44.

[16] Genetic Optimization System Engineering Toolbox (GOSET), 2019., Dec. https://engineering.purdue.edu/ECE/Research/Areas/PES/genetic-optimization-toolbox-2.6.