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Silicon Germanium Design

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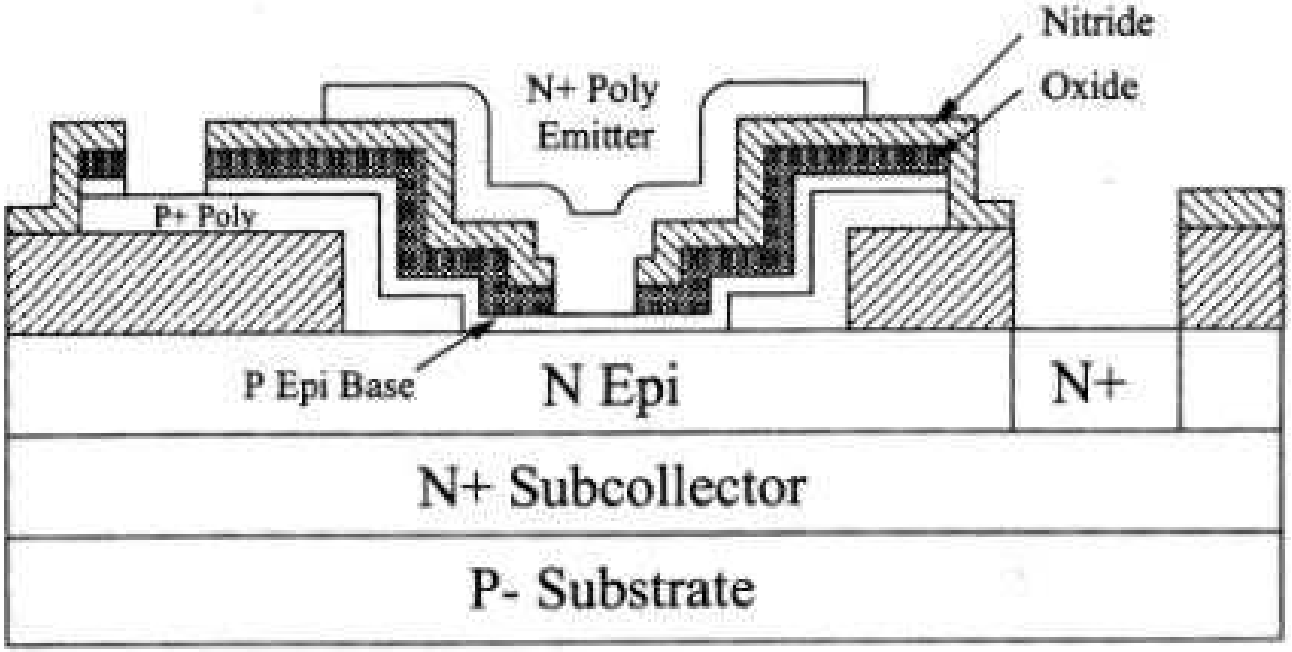
What is Silicon Germanium?

- For the designer, SiGe implies a standard CMOS process with a single device (HBT) added.

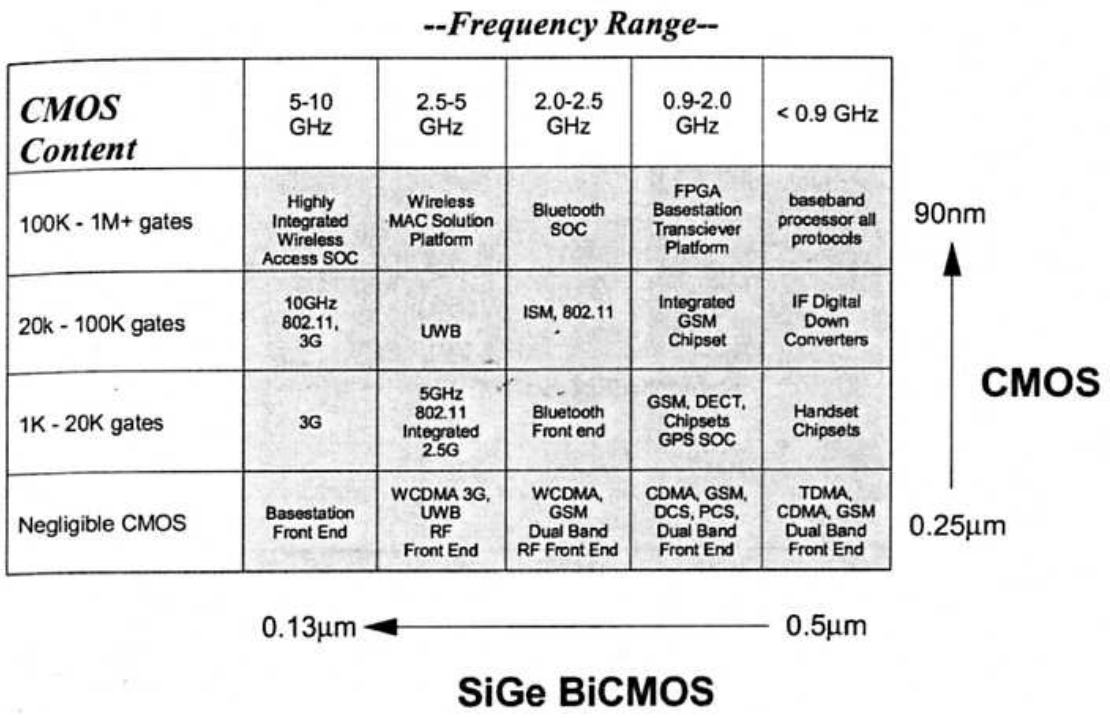


Diagrams from: R.Singh, D.L. Harame, and M.M. Oprysko, Silicon Germanium: Technology, Modeling, and Design, IEEE Press, 2004.

What does SiGe design enable?

- It permits the combination of high performance bipolar circuits with high density CMOS digital logic.

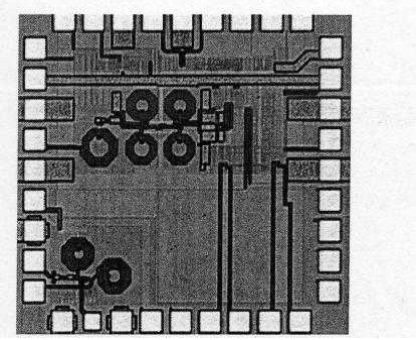
Various wireless application chips fabricated in different SiGe processes. No single process is ideally suited to all applications.



What types of designs can be done in SiGe?

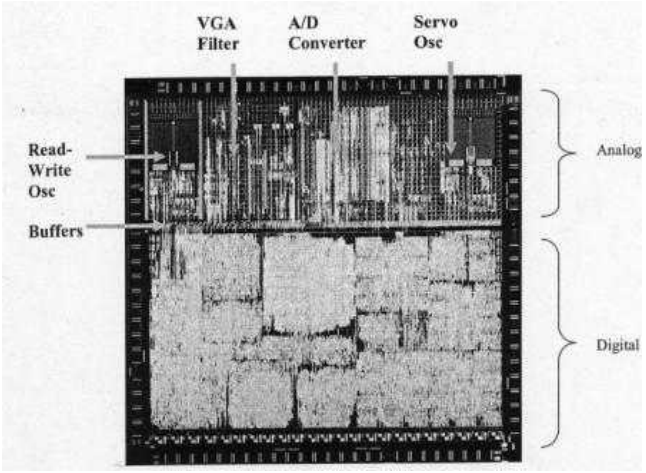
1) Low voltage, low power extremely high speed microwave circuits.

Die photograph is of a 2.07 x 2.07mm downconverter consisting of a LNA and a Gilbert cell mixer. The chip was fabricated in the IBM 6HP process. It operates In the 2110-2170 MHz



2) High density, digital mixed signal designs.

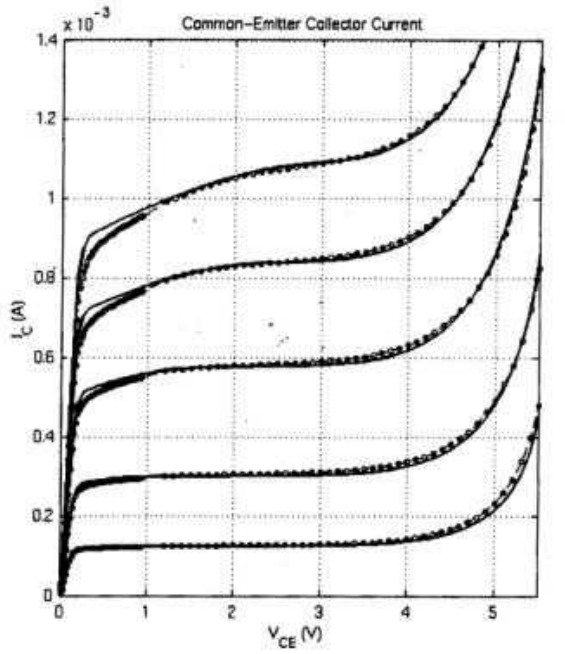
Die photograph is of a high speed PMRL (disk drive) read channel chip fabricated in the IBM 6HP process. Required device propagation times are 175-250 psec.

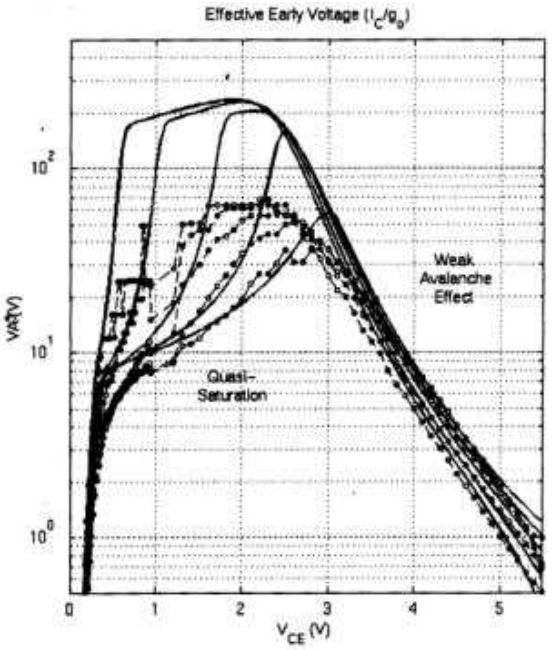


What types of designs can *not* be done in SiGe?

- High frequency power amplifiers

  Vcc=(1/3) x BVceo so P(rms)=(1v) x Icc(rms)





First step in SiGe design process

- Choice of foundry

IBM *	UMC	Texas Instruments
Jazz Semi *	Philips	Intersil
Atmel	STMicroelectronics	
TSMC *	Hitachi	
Maxim	Mitsubishi	
Agere	NEC	
Nortel	Motorola	
Infineon	ON Semi	

(*) Denotes a foundry available to designers outside of that company.

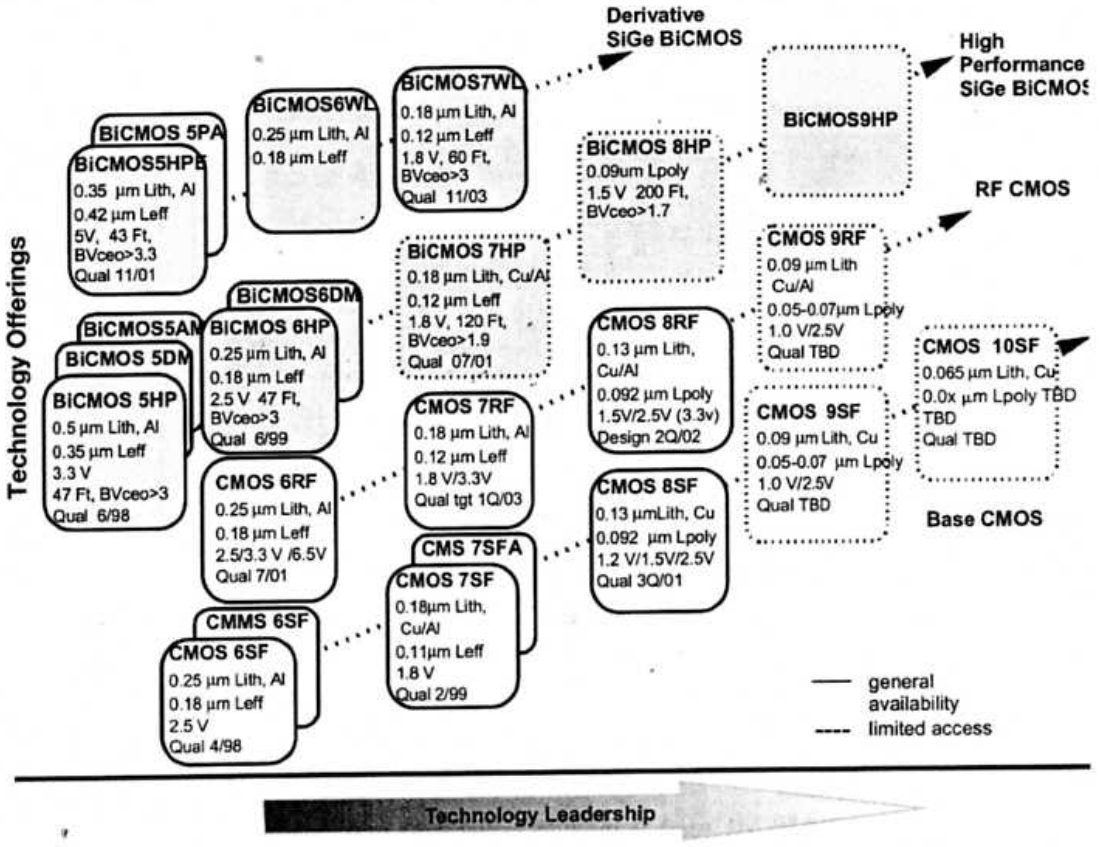
Some characteristics of SiGe designs

- Components and related performance are very foundry specific.
- Microwave portions of the design will be dominated by the physical design (e.g. layout).
- Devices, models, and tools supported are very foundry and process specific.
- All information is proprietary. It is difficult to compare foundries.

Second step in SiGe design process

- Select the correct process based on speed and power requirements:

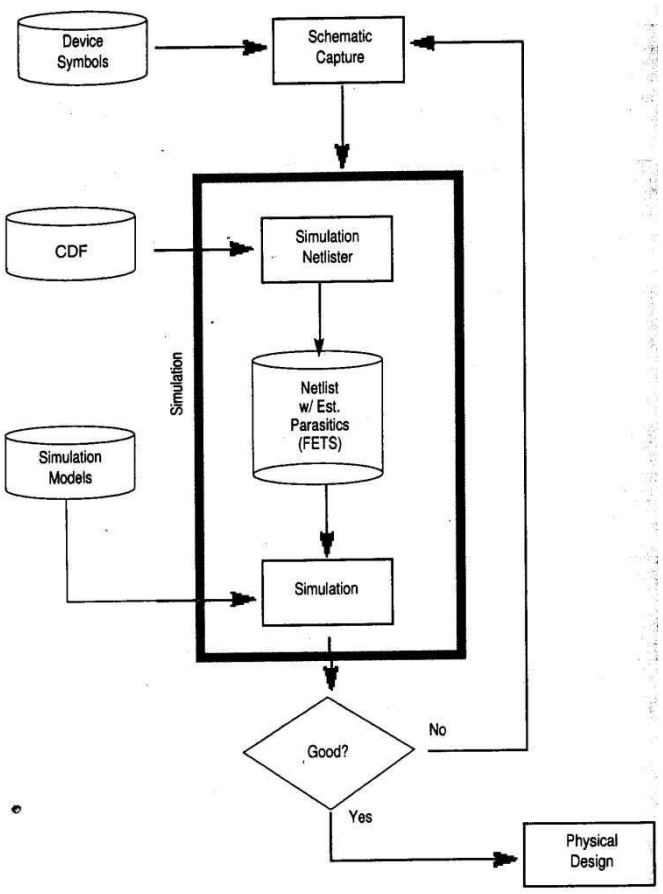
IBM SiGe and advanced CMOS Processes.



Third step in SiGe design process

- Setup of foundry supported models and simulation software.

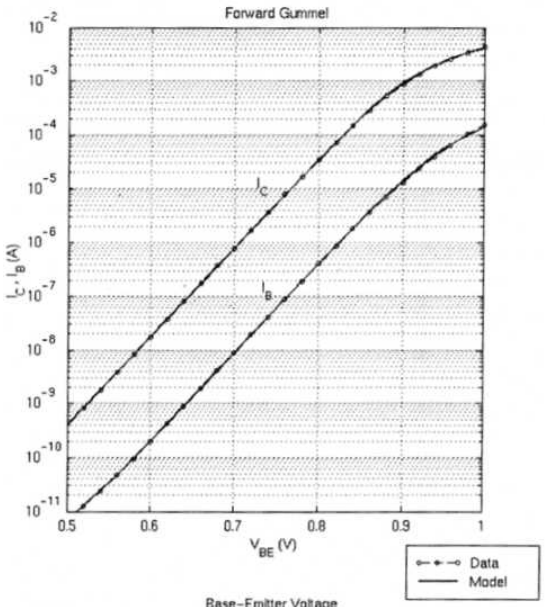
The foundry will supply models and related support software that are written and supported on a particular set of design and layout tools. IBM supports the Cadence Spectre analog design environment, the Cadence Assura physical layout tools, and a variety of other specialty tools. This makes for high entry costs into the SiGe design world. In practice, one will find many low budget operations that design sophisticated SiGe chips without these tools. However, they receive little support from the foundry.

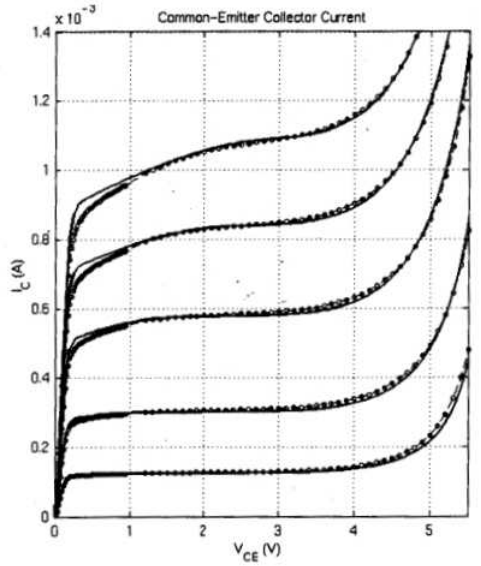


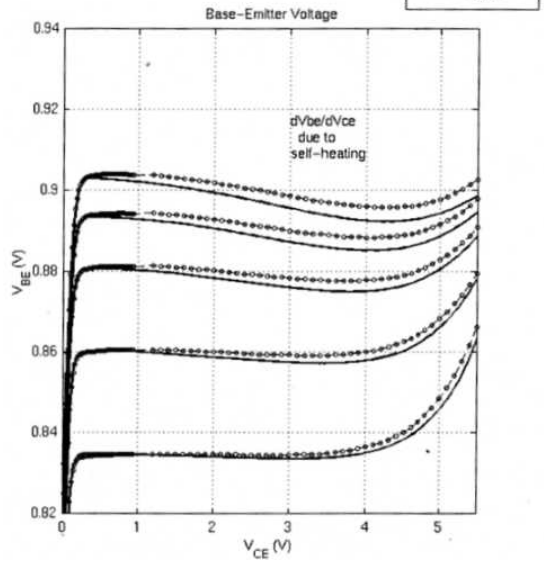
Device Modeling

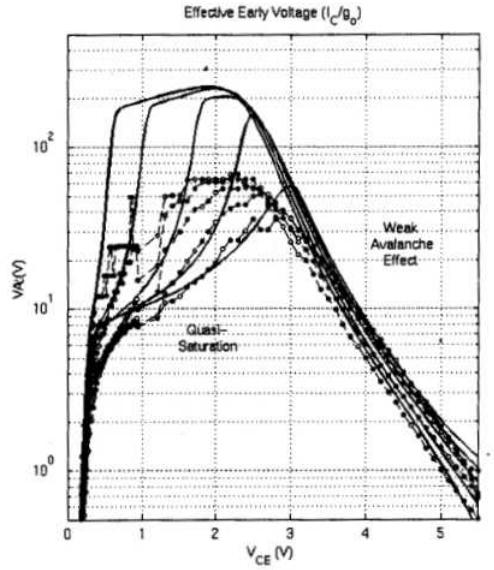
Use of VBIC or MEXTRAM bjt models gives good device level simulation of hitherto negligible parametric effects.

However, these models are cumbersome and can cause problems in full circuit simulations.



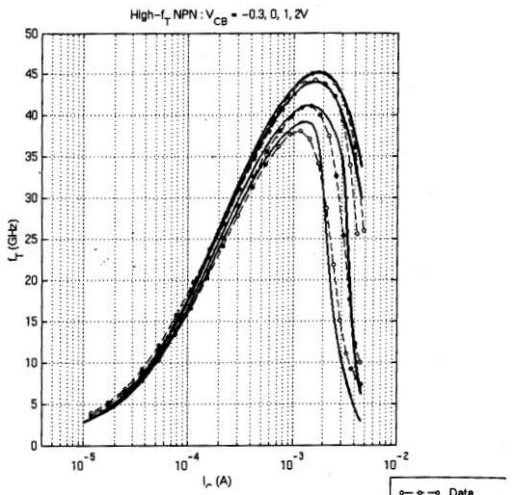


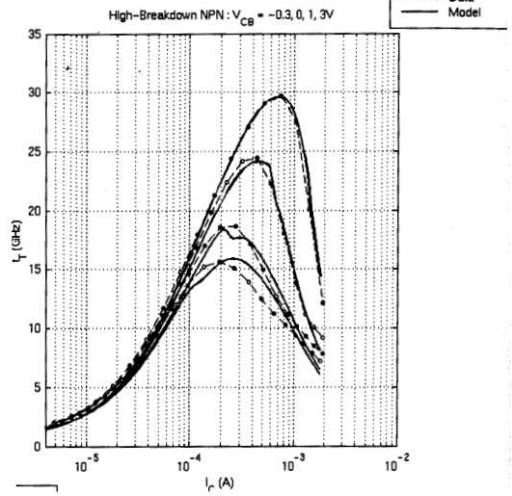


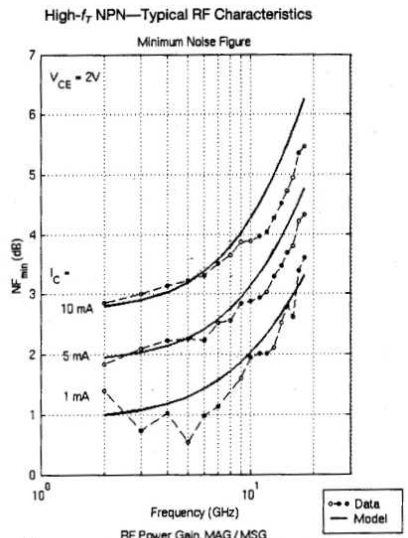


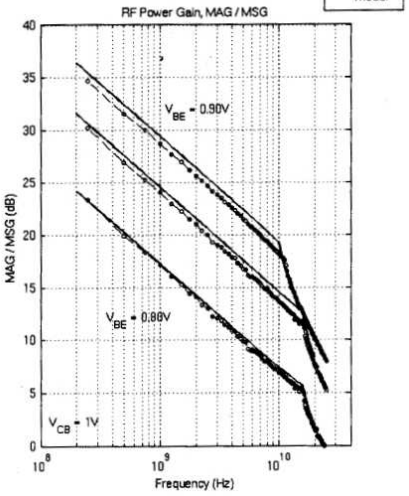
Device Modeling

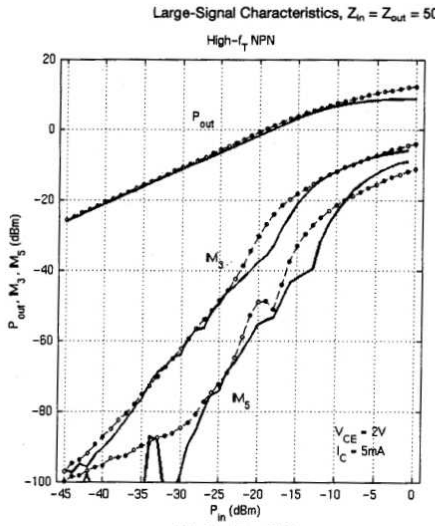
Models provide good device level simulations of gain, F, P1dB, IM3, etc.

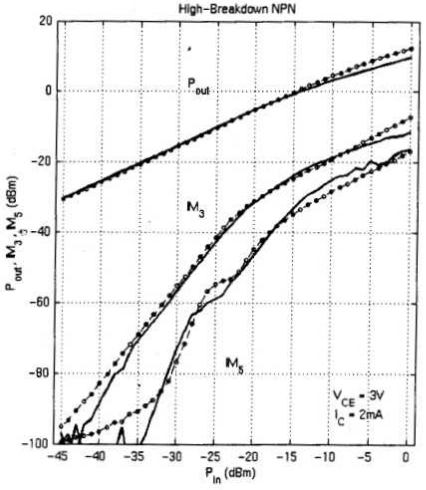








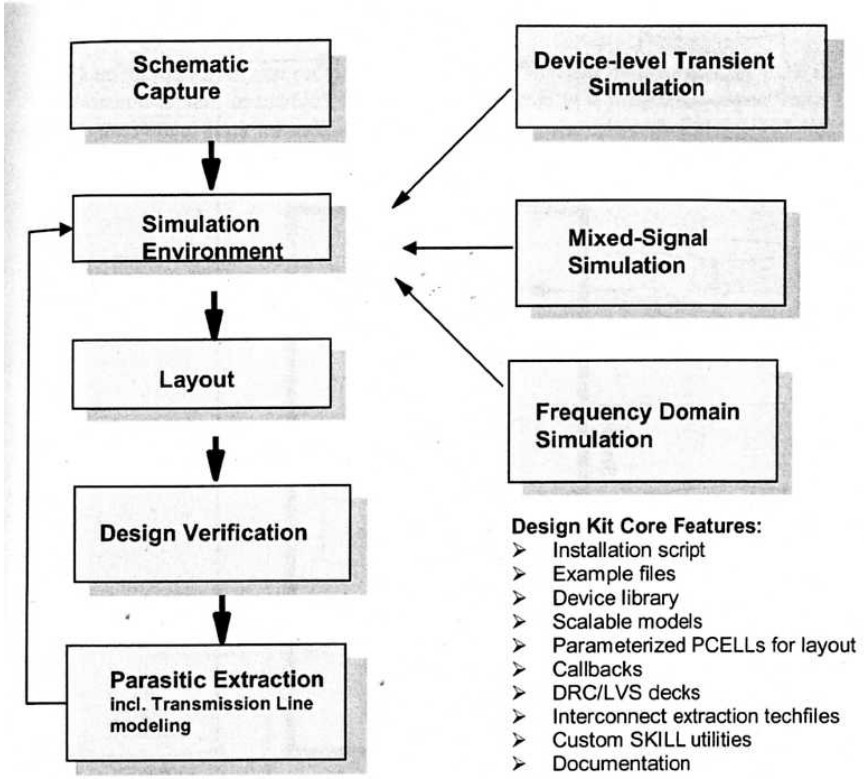




Fourth step in SiGe design process

- Design and iteration of circuit from equation-based process through complete circuit simulation.

The design flow is similar regardless of what design, simulation, or layout tools are used. This design flow was produced by IBM. It skips the most critical step. Before schematic capture can reliably be done, one must perform a basic design analysis using the skills taught in this class. Impedances, matching networks, gains, and bandwidths should be estimated before a simulator is ever started up.



Pitfalls at step four

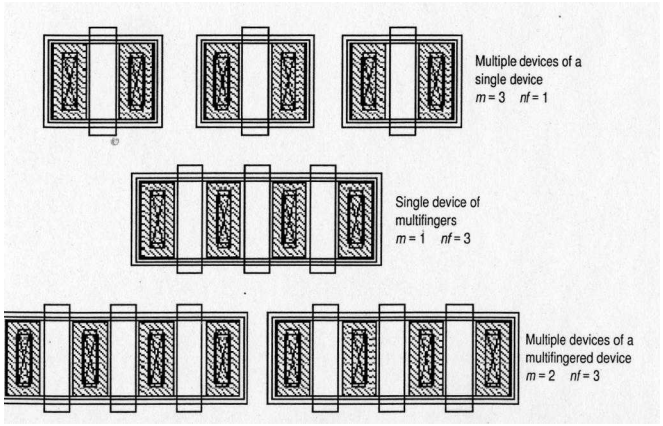
- The design process is increasingly being forced into “black box” software.
- Models and simulation and verification software are complex to a level that no one person can understand entirely what is going on when behavior is erratic.
- Bugs are creeping through at all levels
- Design problems are complex enough that they are only being caught at prototype test phase.
- This is very expensive, as prototype fabrication is $50k (small analog only) to $500k (medium size digital chip). Masks alone for a full wafer 0.13um design cost $1M.
- The only solution is the use of “old fashioned” hand calculations as checks at every stage of the design.

Fifth step in the SiGe design process

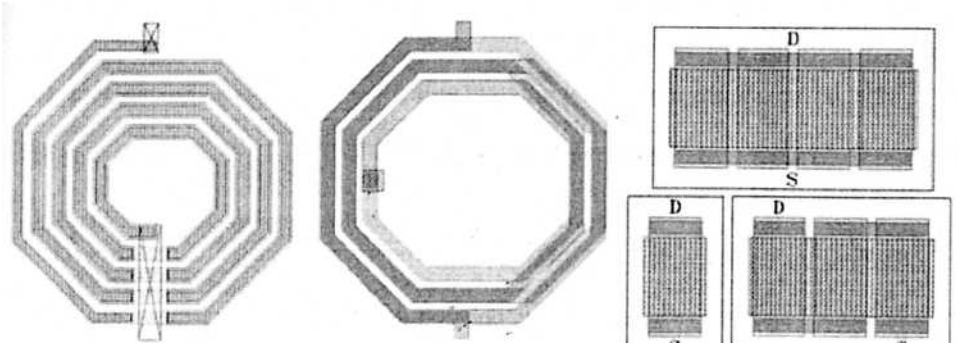
- Layout – cell generation and connection

PCELLS (Parameterized cells) are generated within the layout tools for all elemental devices (FETs, BJTs, capacitors, resistors, and inductors).

These cells are generated by entering the desired device parameters into a form specific to that device. All mask layers for the cell are then created from a proto-cell.



The only problem with this approach is that the generation software and the proto-cells do not always keep pace with rapid changes in the fabrication technology and design rules. Sanity checks must still be performed on cells produced by this process.

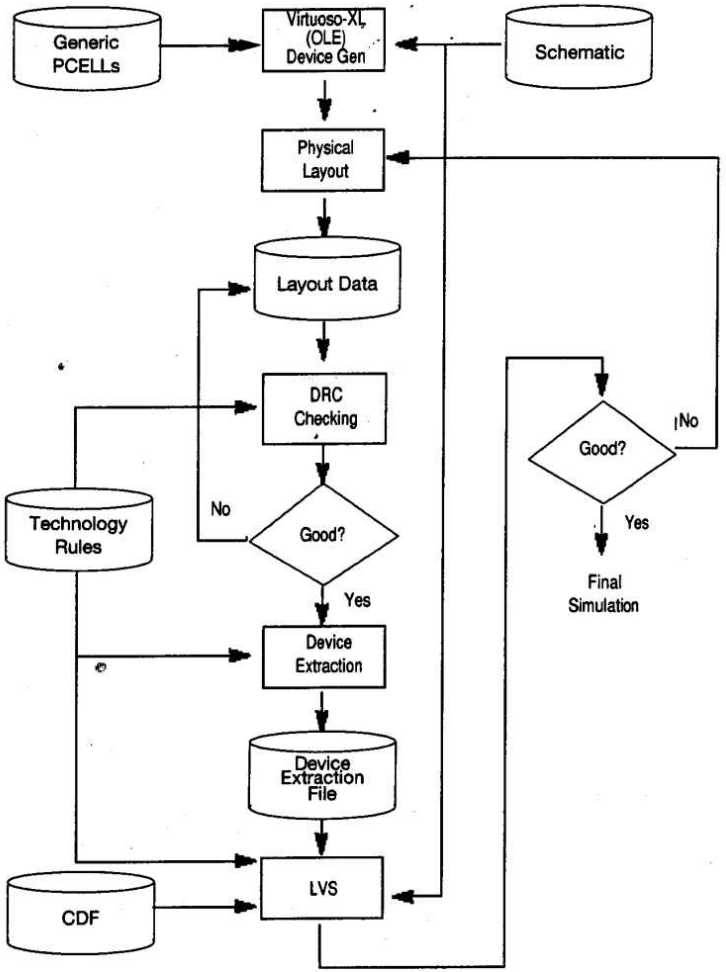


Sixth step in SiGe design process

- Verification – DRC, LVS, parasitic loaded simulation.

Design verification is the most important step of the process. It is the last step and also tends to be the step most cheated of the necessary time to do the job. The process ideally consists of DRC (design rule checking) to look for physical mask rule violations, LVS (layout vs. schematic) to check the resulting circuit against the original schematic, and final simulation of the parasitic-loaded schematic.

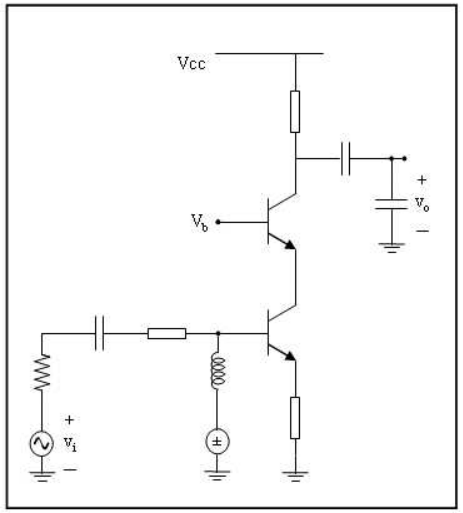
In practice, these steps are often vitiated or skipped entirely.

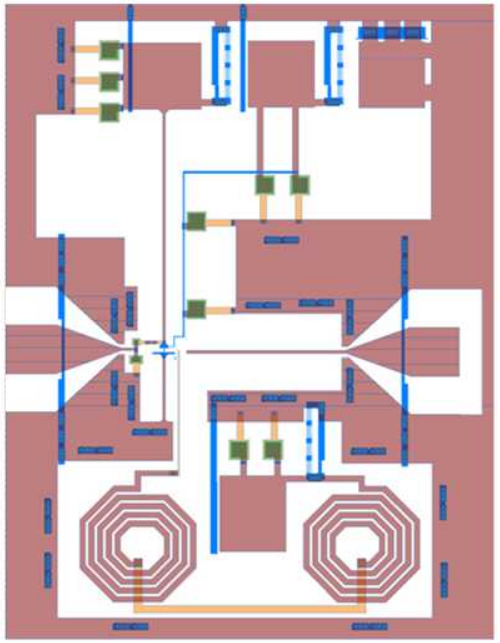


Example Designs: Berkeley Wireless

28 GHz Low Noise Amplifier

Sohrab Emami





Simulation:

I_{core}=6 mA

V_{CC} = 3 V

S_{11}= -30dB S_{22}= -20dB

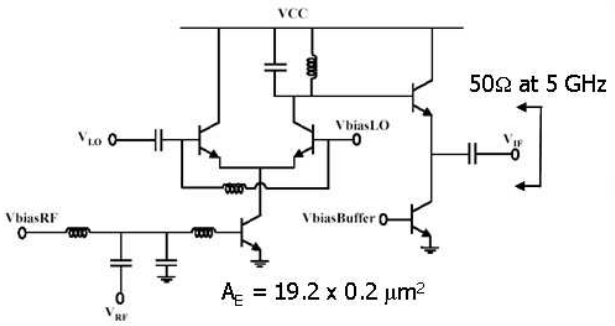
S_{21}= 15.1dB NF= 3.2dB

BWRC

Example Designs: Berkeley Wireless

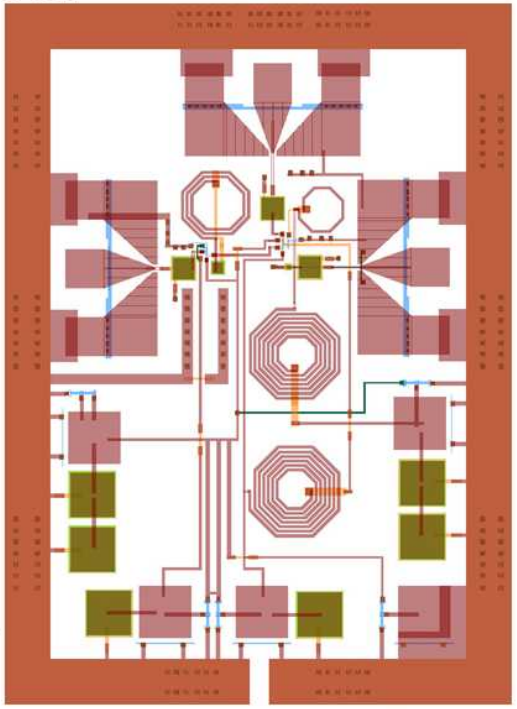
30 GHz to 5 GHz Mixer

Mounir Bohsali



Conversion Gain	11.44 dB
Noise Figure	16.8 dB
Total Power	30 mW
Buffer / Mixer	9 / 21

Simulated Performance



- Traditional microwave mixers are passive and lossy (but linear)
- In this research project we would like to find the upper frequency limits for an active mixer

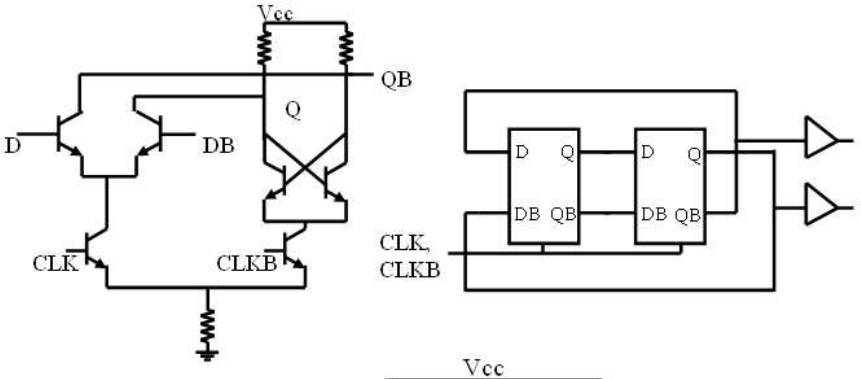
BWRC

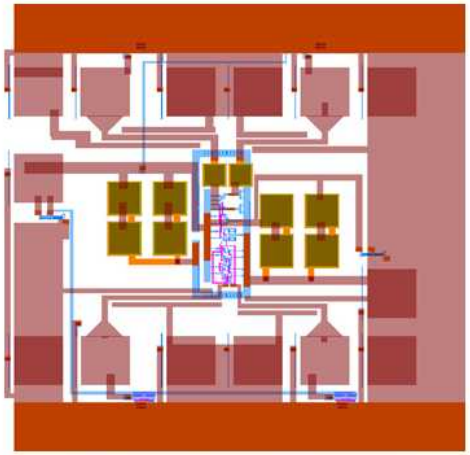
Example Designs: Berkeley Wireless

30GHz SiGe Dividers

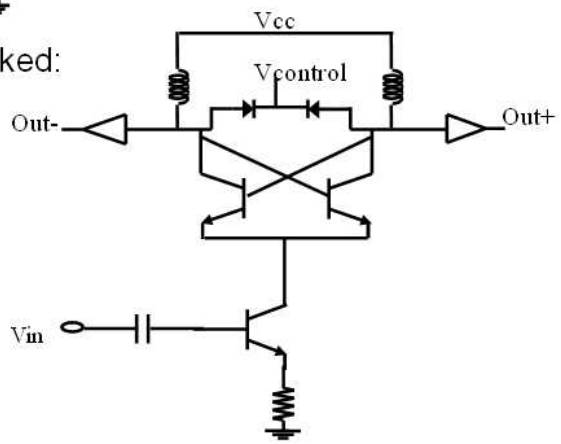
Eddie Ng

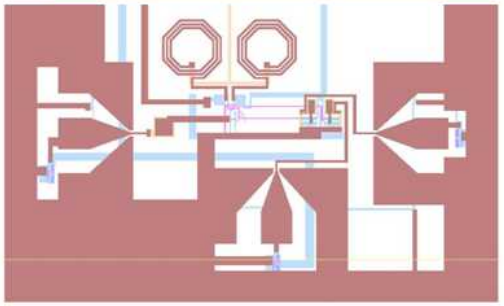
FF-Based:





Injection-locked:





BWRC