CMP
Integration Issues

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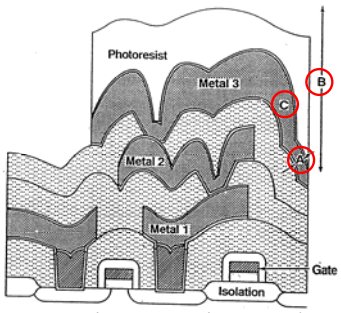
Outline

- Introduction
  - What is CMP?
  - History and Future
  - Brief description of consumables
- CMP processes and applications
  - Glass polishing basics
  - Dielectric CMP
    - ILD, STI
      - Issues related to layout
      - Common STI defects caused by integration
  - Cu CMP
    - Process cycle time issue
    - Layout-generated issues
  - Replacement gates

Driving Forces Behind Planarization



A) Film Deposition
Step coverage

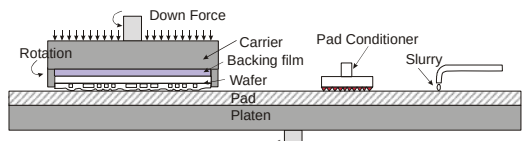
B) Lithography
Depth of focus

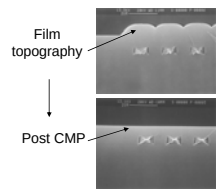
C) Etch
Etch stringers

D) New materials and manufacturing
ex. damascene Cu CMP

Diagram - C. Paumier, SEMICON/Europa 95 Technical Conference

Chemical-Mechanical Polishing (CMP)

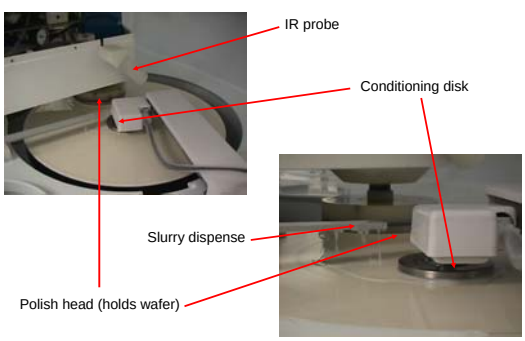




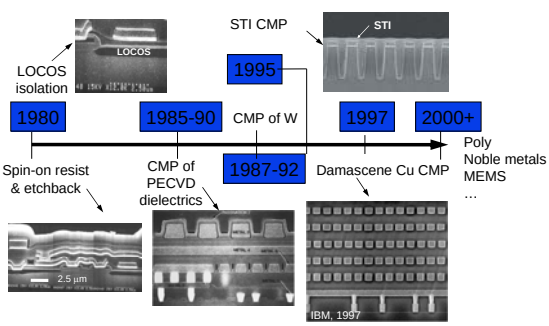
Process Parameters

- Pad and slurry type
- Polishing tool
  - Pressure (carrier/backside)
  - Velocity (carrier/platen)
  - Carrier design
  - Flow rate of slurry
  - Temperature (slurry/pad)
- Pad conditioning

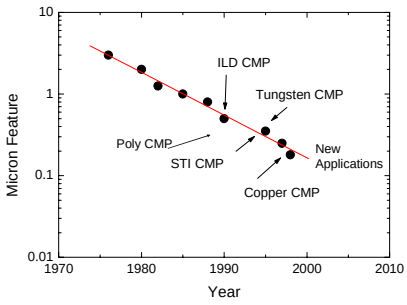
CMP



Technology Enabled by CMP

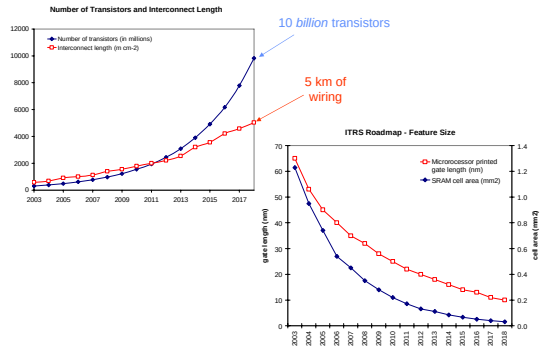


Moore's Law and CMP Applications



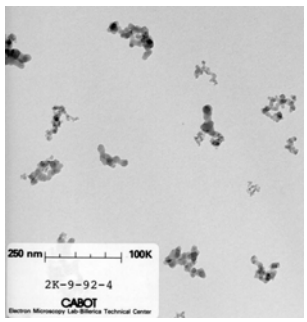
Minimum Feature Size Data: Hetherington, IEDM Short Course, 1999

Where We Are Going



ITRS Roadmap

TEM of Fumed Silica Particles*



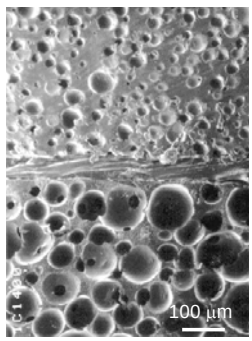
* Courtesy of Cabot Microelectronics

Closed Cell Foam Pads - IC1400 (Class III)

top pad

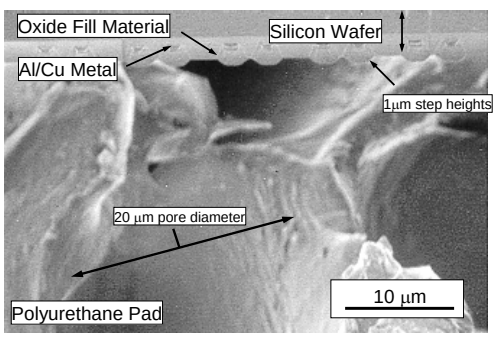
glue layer

bottom sub-pad



IC1400 pad is manufactured by Rohm and Haas.

Relative Scale of Asperities



Dielectric CMP

Preston - Removal rate[1]

- Empirical wear equation

$$PR = k_p \cdot P \cdot v$$

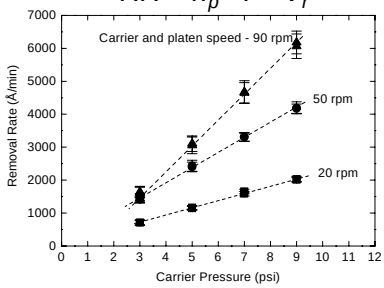
PR - *Glass polish rate*
k_p - *Preston coefficient (process dependent)*
P - *Applied pressure*
v - *Linear velocity*

- Brown[2] and Cook[3] showed derivation $PR = \frac{Pv}{2E}$
  - elastic Hertzian indentation
  - material removed equals indentation cross-sectional area * distance traveled
  - where E = Young's modulus
- Cook[3] noted experimental k_p and $(2E)^{-1}$ don't agree

(1) F. Preston, J. Soc. Glass Tech. 11 (1927) 214.
(2) N. J. Brown, P. C. Baker, and R. T. Maney, *SPIE **306** Contemporary Methods of Optical Fabrication*, 1981, 42.
(3) L. M. Cook, *J. Non-Cryst. Solids* **120**, 1990, 152.

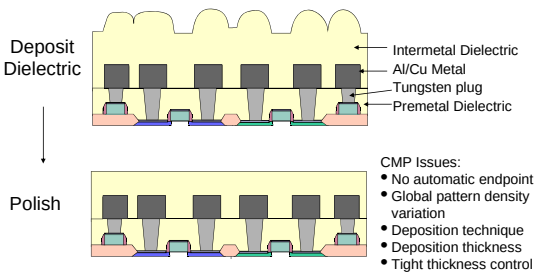
Polishing Kinetics

$$RR = k_p * P * v_r$$



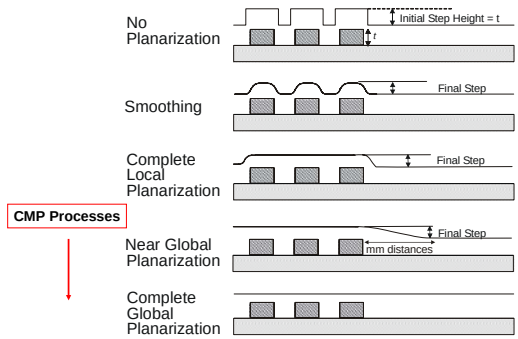
k_p varies with slurry, glass type, etc.

Back End of Line Dielectric CMP

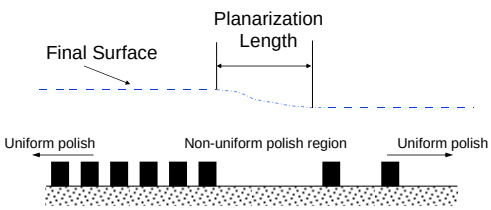


CMP Issues:
- No automatic endpoint
- Global pattern density variation
- Deposition technique
- Deposition thickness
- Tight thickness control

Degrees of Planarization

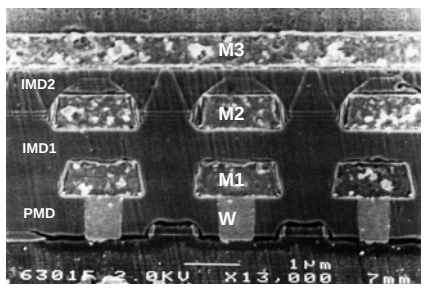


Planarization Length

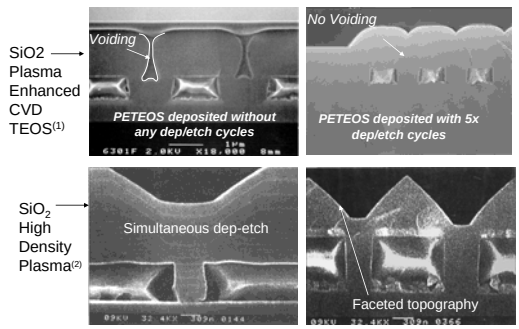


Typical polishing processes result in 3 - 5 mm planarization lengths.

Back-end Dielectric CMP

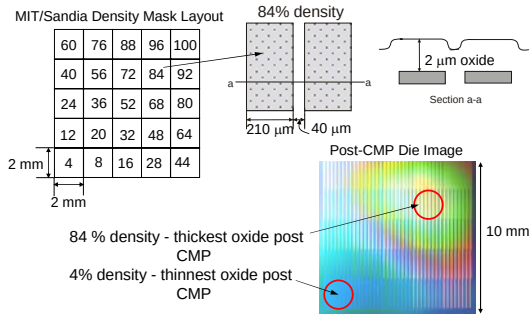


Surface Profile and Gap-fill Technique

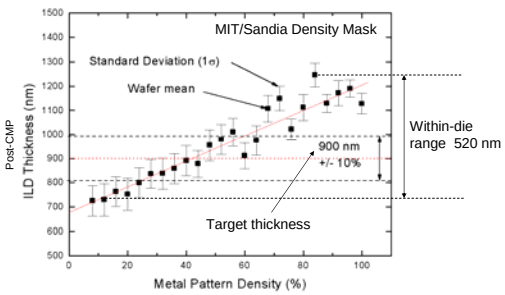


(1) L. Roherty-Osmun, Sandia Labs (2) J. T. Pye et al., Solid St. Tech., Dec. 1995.

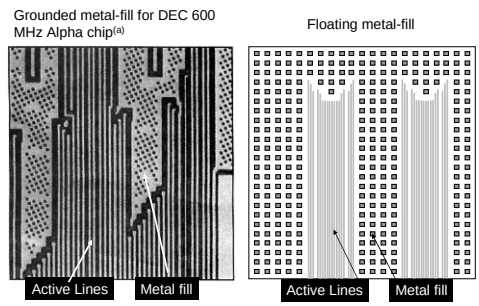
Pattern Density Variations - Measurement



Final Dielectric Thickness Vs. Pattern Density



Examples of Dummy Metal-Fill

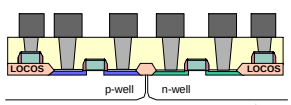


(a) P. Gronowski, et al. IEEE J. Solid-State Circuits, vol. 33, **5**, p. 676, (1998).

Shallow Trench Isolation CMP

Device Isolation Techniques - LOCOS vs. STI

Lateral isolation candidates



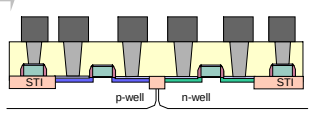
Shallow Trench Isolation with Chemical Mechanical Polishing

+ Small active area pitch possible
+ Denser device packing
+ Superior planarity!

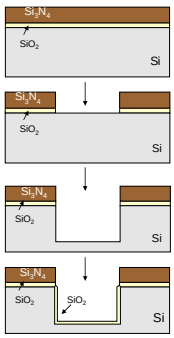
LOCOS-based techniques in 0.25 µm technology

+ Manufacturable, simple, good know-how
- Large 'bird's beak'
- Deep submicron scalability

Further down-scaling



STI Process Flow



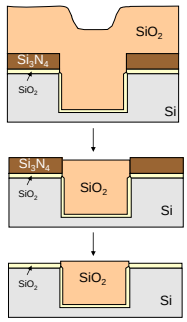
Isolation stack :
Thermal oxide growth (pad oxide)
Active protecting nitride

Pattern and etch of Si_3N_4 and SiO_2

Trench etch into Si

Thermal oxidation of trench sidewall, corner rounding

STI Process Flow

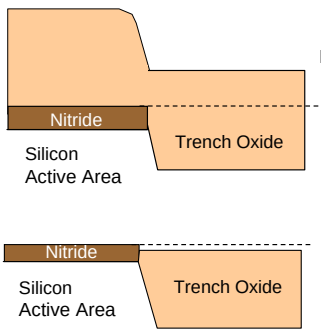


Deposition of trench filling oxide (f.ex. HDP-CVD)

Oxide CMP Polish step with stop on nitride

Removal of nitride layer (wet etch in phosphoric acid)

CMP STI Polishing Regimes



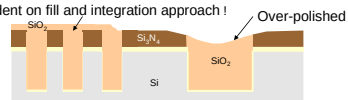
I. Removing step height and oxide over the active area

II. Over-polish to ensure that all oxide is removed over active area everywhere on the die.

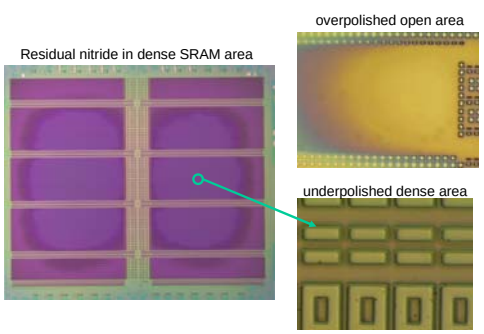
STI-CMP Issues

- Pattern layout effects
  - local removal rate ~ local pressure ~ $\frac{1}{\textit{pattern density}}$
  - variations in the active area to field step height after nitride strip
    - problems at subsequent lithography steps!
  - dishing in large field areas influence on surface planarity!

Incomplete Polish or Erosion?
→ Dependent on fill and integration approach !



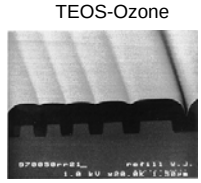
The Problem



Trench Fill Method

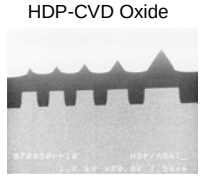
Local planarization as a function of active area width:

TEOS-Ozone



+/- Same oxide thickness everywhere

HDP-CVD Oxide



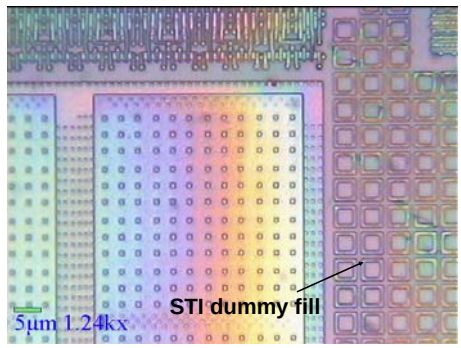
Different pyramids dependent on active area width

→ Difference in CMP behavior!
(pattern density effects)

Use of Dummy Structures

- Dummies widely used in oxide CMP BEOL
  - easiest way to solve pattern density variations
- Similar idea for STI level
  - Large field areas around isolated active areas can be filled up with *dummy active areas*
  - risk of overpolishing is reduced
- Dummies have a lot of design issues
  - designers don't like them
  - mixed signal technologies are especially sensitive to dummy structures
    - –capacitive coupling and noise

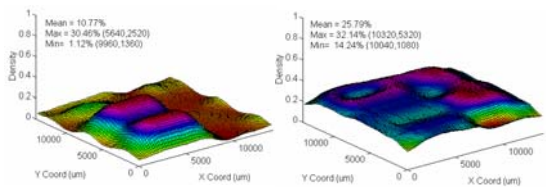
STI Dummy Fill



Courtesy of J. Soden Sandia National Labs

Modifying Existing Layouts

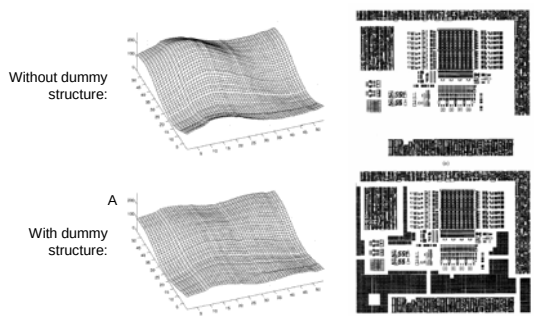
- Requires
  - analysis of within-chip layout density variations
  - dummy fill optimization



Optimized fill structure reduces density variation from 29% to 18%

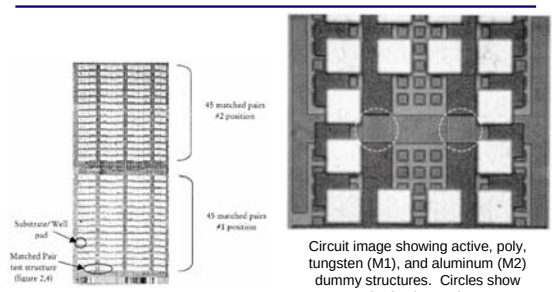
Dummy Fill

Physical process model-based dummy structure design:



R.Tian and X. Tang, IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, VOL. 21, NO. 1, JANUARY 2002

Dummy Structures: Relative Transistor Mismatch

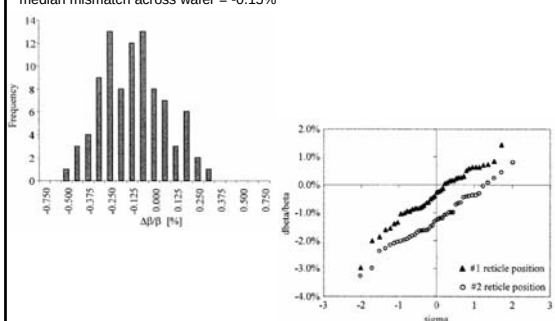


Circuit image showing active, poly, tungsten (M1), and aluminum (M2) dummy structures. Circles show matched pair transistors.

H. Tuinhout and M. Vertregt, *IEEE Transactions on Semiconductor Manufacturing*, 14 **4**, 2001, 302-310.

Test Transistor Layout and Matching Results

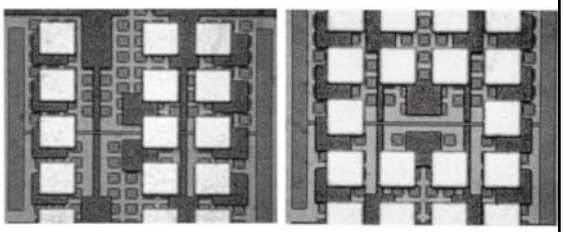
median mismatch across wafer = -0.15%



H. Tuinhout and M. Vertregt, *IEEE Transactions on Semiconductor Manufacturing*, 14 **4**, 2001, 302-310.

Dummy Placement Differences

M2 dummy placement varied between the two positions of matched transistors. The authors attributed variation in dummy placement to variation in mismatch between supposedly matched transistors.



reticle position 1 reticle position 2

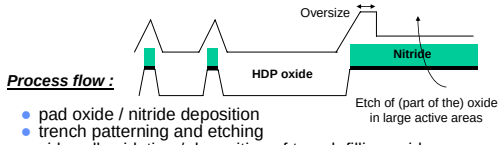
Note that dielectric thickness was not studied.

H. Tuinhout and M. Vertregt, *IEEE Transactions on Semiconductor Manufacturing*, 14 **4**, 2001, 302-310.

Oxide Reverse Etch Approach

Oxide Reverse Etch (ORE), followed by CMP :

Process flow :

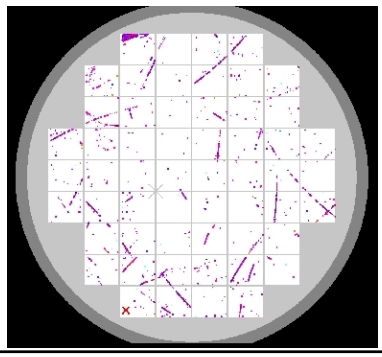


- pad oxide / nitride deposition
- trench patterning and etching
- sidewall oxidation / deposition of trench filling oxide
- *remove (most of) the oxide on large active areas with additional litho and etch step*
- remove remaining oxide from the active areas during the CMP step
- nitride removed during etch step

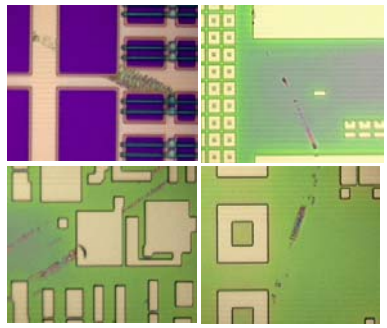
Parameters to be optimized:

- Oversize (litho misalignment)
- Amount of oxide etched back?

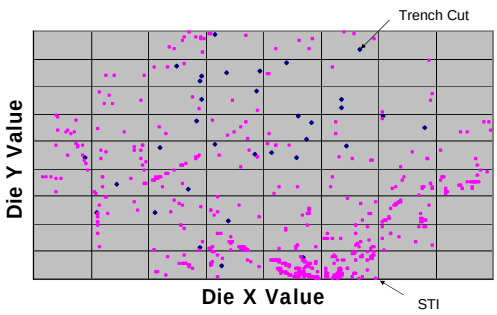
STI Defects



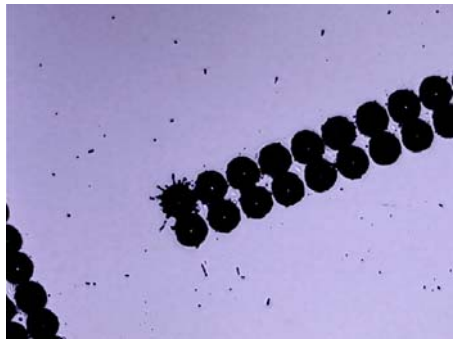
Defects



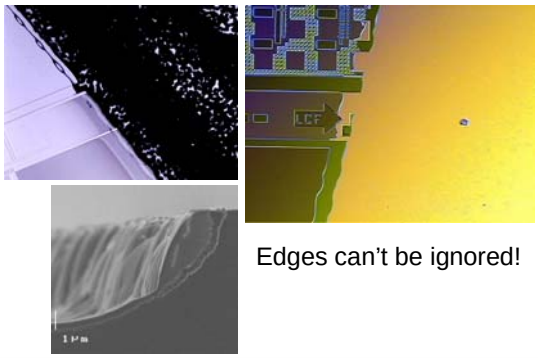
Defect Wafer Map



Defect Source

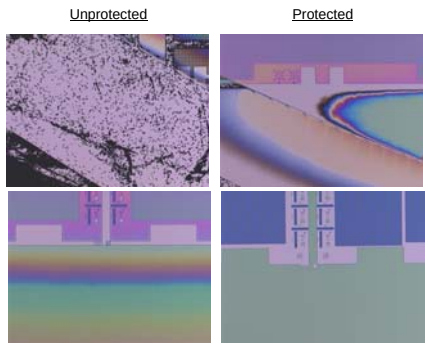


Wafer Edges



Edges can't be ignored!

Edge Comparison

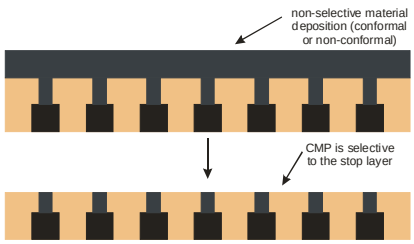


Summary - Dielectric CMP

- Pattern density effects are the key problem to solve for dielectric CMP
- Defectivity is also important
- Slurry and pad engineering is focused on solutions for improving planarity and minimizing defects
- Chip layout can be optimized for CMP process

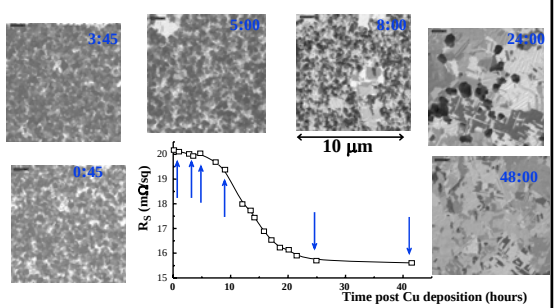
Cu CMP

CMP Removal to Stop Layer



- Material removal and planarization
  - W plugs, copper dual damascene, aluminum (dual) damascene, STI, polysilicon-filled trenches

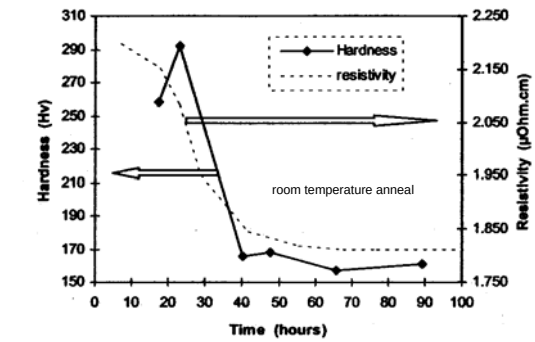
Grain Structure Evolution



Similar time dependence as R_S !

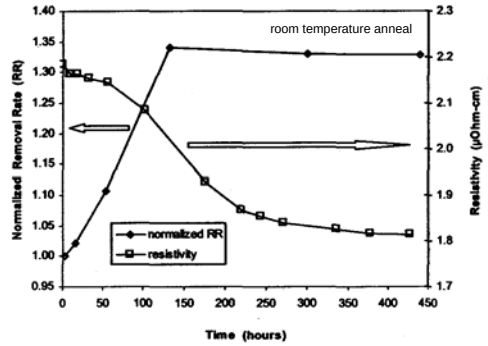
Source: S. Brongersma (Imec)

Hardness and Resistivity vs. Anneal Time



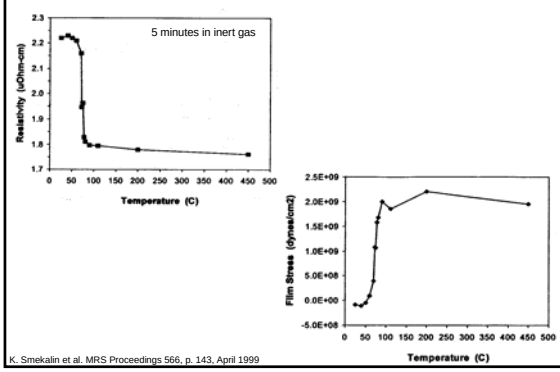
K. Smekalin et al. MRS Proceedings 566, p. 143, April 1999

PR and Resistivity vs. Anneal Time



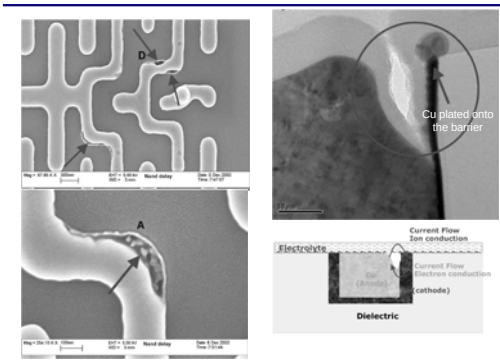
K. Smekalin et al. MRS Proceedings 566, p. 143, April 1999

Elevated Temperature Anneals



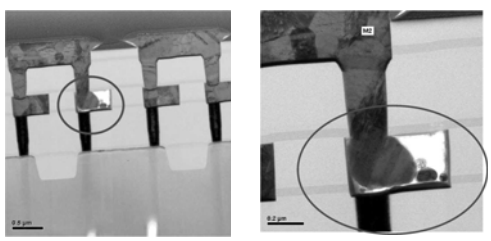
K. Smekalin et al. MRS Proceedings 566, p. 143, April 1999

Galvanic Cu Corrosion



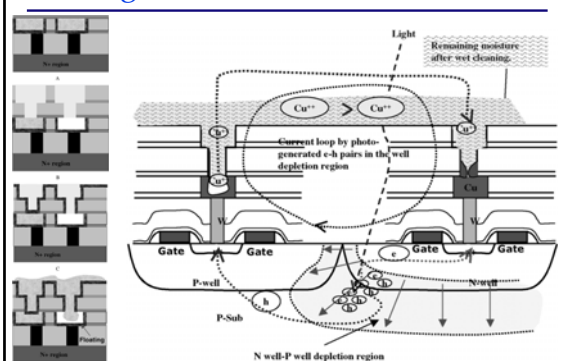
Z. Song et al., IEEE Transactions on Device and Materials Reliability **5** (2), 206, June 2005

Light-assisted Cu Corrosion



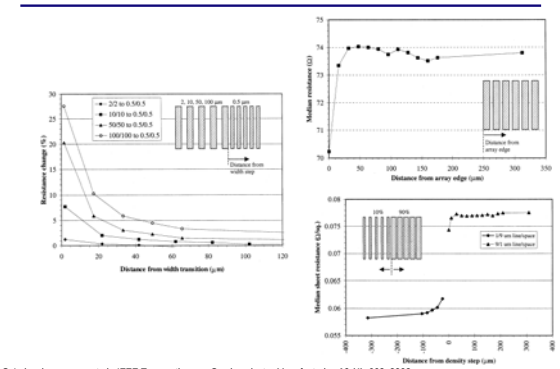
Z. Song et al., IEEE Transactions on Device and Materials Reliability **5** (2), 206, June 2005

Light-assisted Cu Corrosion



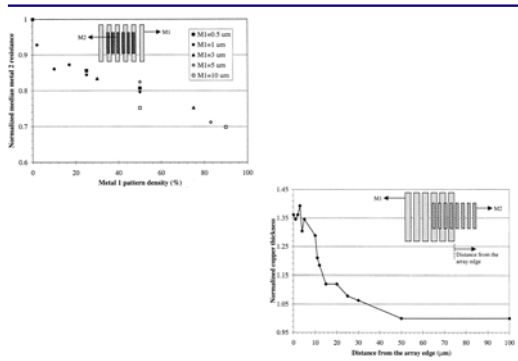
Z. Song et al., IEEE Transactions on Device and Materials Reliability **5** (2), 206, June 2005

Determination of Cu Design Window



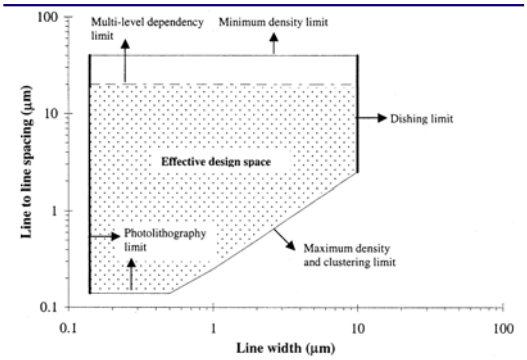
S. Laksminarayanan et al., IEEE Transactions on Semiconductor Manufacturing **16** (4), 668, 2003

Determination of Cu Design Window



S. Laksminarayanan et al., IEEE Transactions on Semiconductor Manufacturing **16** (4), 668, 2003

Determination of Cu Design Window



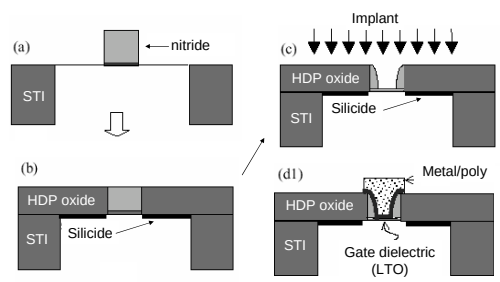
S. Laksminarayanan et al., IEEE Transactions on Semiconductor Manufacturing **16** (4), 668, 2003

Novel Gate Structures

Front End - Replacement Gate Technology

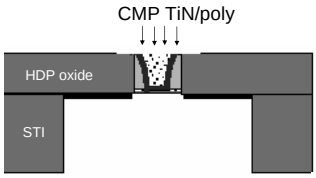
- Oxide CMP stopping on polysilicon (high selectivity required)
- Silicon nitride CMP stopping on oxide (high selectivity required)
- Dishing and erosion issues due to pattern density must be tightly controlled.

Replacement Gate Process for Sub-50 nm CMOS

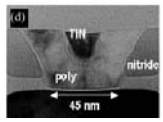


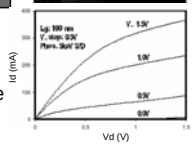
C.P. Chang, et al. *Proc. IEDM*, Dec. 2000.

Replacement Gate Process for Sub-50 nm CMOS



SEM of gate region





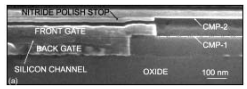
- Front End CMP
  - STI
  - HDP Oxide stopping on nitride
  - TiN/poly gate CMP

C.P. Chang, et al. *Proc. IEDM*, Dec. 2000.

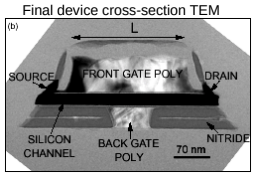
Triple-self-aligned Double-gate Structure

- CMP used for planarization at multiple stages during front-end processing
- High selectivity to nitride polish stop layer
- Planarity to within 5 nm across the wafer

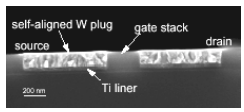
Multiple oxide CMP steps stopping on nitride



Final device cross-section TEM

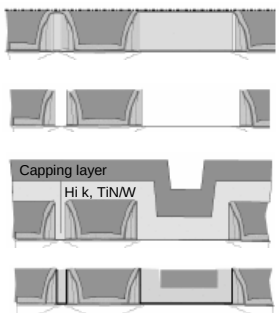


Tungsten plugs formed using CMP



K. W. Guarini, et. al., *IEDM 2001*, p. 425.

75 nm Damascene Metal Gate



Dielectric CMP

Replacement gate removal

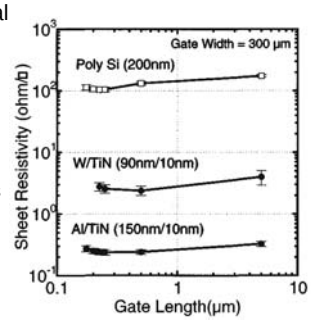
Hi k (HfO_2) , TiN, W, and capping layer deposition.

Capping and metals CMP

B. Guillaumot, et al., *IEDM Tech Digest*, Dec. 2002.

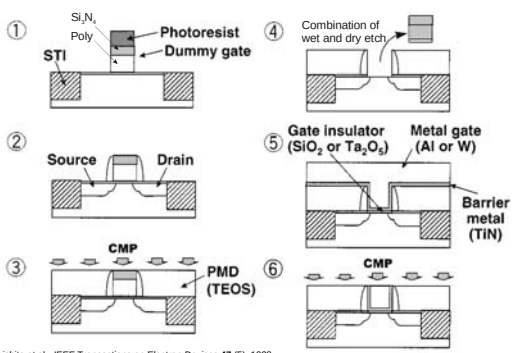
Damascene Metal Gate

- Why damascene metal gates instead of poly?
  - high poly gate resistance limits speed
  - boron penetration from doped poly changes threshold V
  - gate leakage degrades device reliability
  - threshold voltage deviation



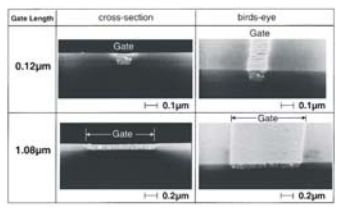
A. Yagishita et al., *IEEE* Transactions on Electron Devices **47** (5), 1028.

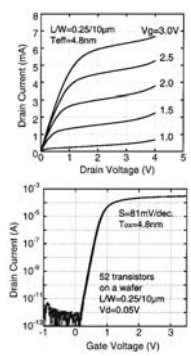
Damascene Metal Gate



A. Yagishita et al., *IEEE* Transactions on Electron Devices **47** (5), 1028.

Damascene Metal Gate

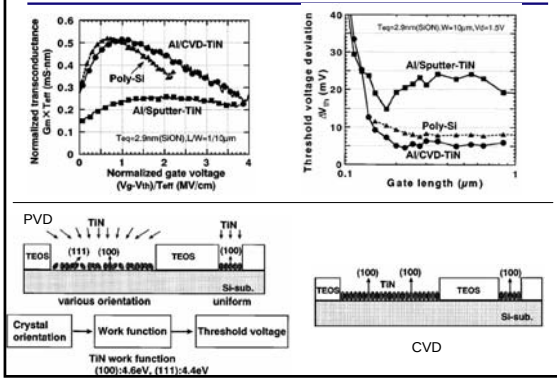




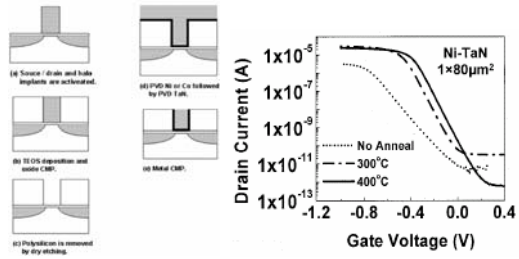
- Damascene metal gates
  - allow for high-K gate dielectrics
  - Minimizes plasma damage
  - complete planarity and high scalability
  - low sheet resistivity thus lower RC time delay
  - no depletion
  - dramatic improvement in GOI

A. Yagishita et al., *IEEE* Transactions on Electron Devices **47** (5), 1028.

Material Issues with Replacement Gates



Ni-TaN Replacement gate



J. Pan et al., *IEEE Transactions on Electron Devices*, 50 **12**, 2003, 2456-2460.

Acknowledgements

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