Solder Interconnection SIP Software for the Windows XP™ Platform

SAND2006-5599P

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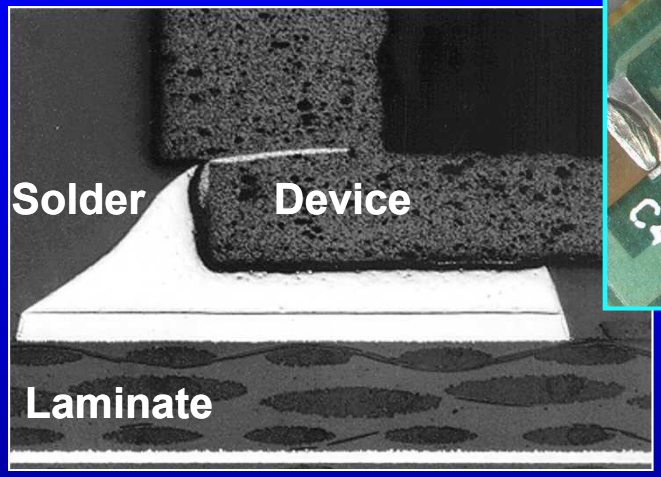
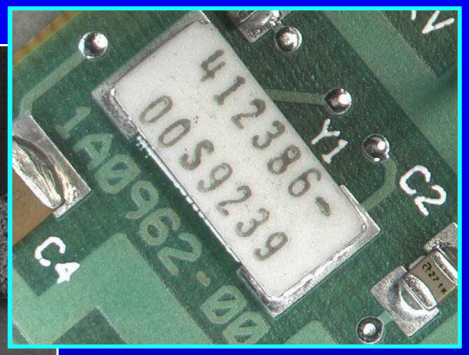
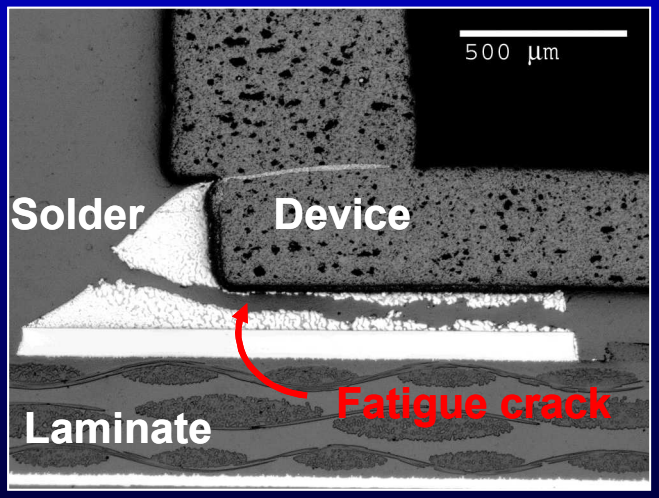
*Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the US Dept. of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.

Thermal mechanical fatigue (TMF) of solder interconnections can degrade the long-term reliability of electronic assemblies.







-55° C / 125° C … 1000 cycles

Two computational approaches have been developed at Sandia for predicting the TMF degradation of solder interconnections

Commercial software package

Solder Reliability Solutions©
ESP, Inc.
(1990)

- Strain energy approach
  $N_f(\Delta W^{\alpha}) = D$
- Library of components, material properties, and thermal histories
- Limited user input
- Statistical prediction

SIP model

CompSIR© code — *1999*

SIP© model ***(LMC/SNL - Shared Vision)***

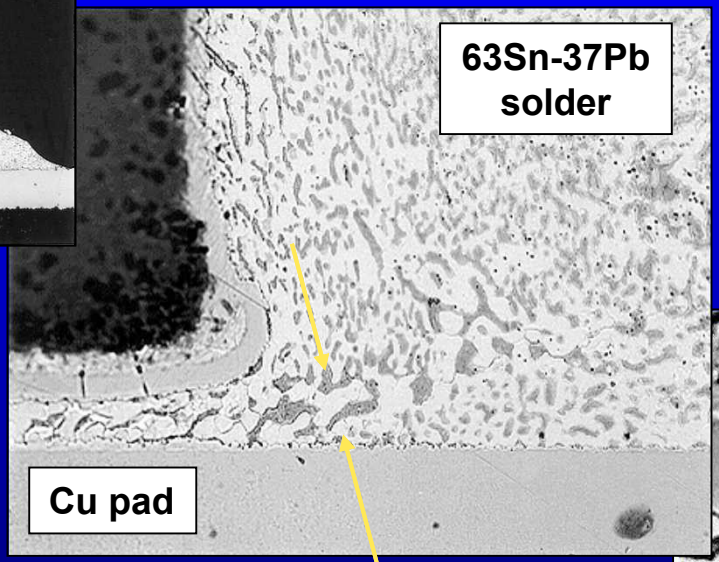
SIP© UNIX™ ***(LMC, SNL, and Strikewire LLC)*** — *2002*

SIP© Windows™ ***(LMC-DTO/Navy, Kansas S. and SNL,)*** — *2007*

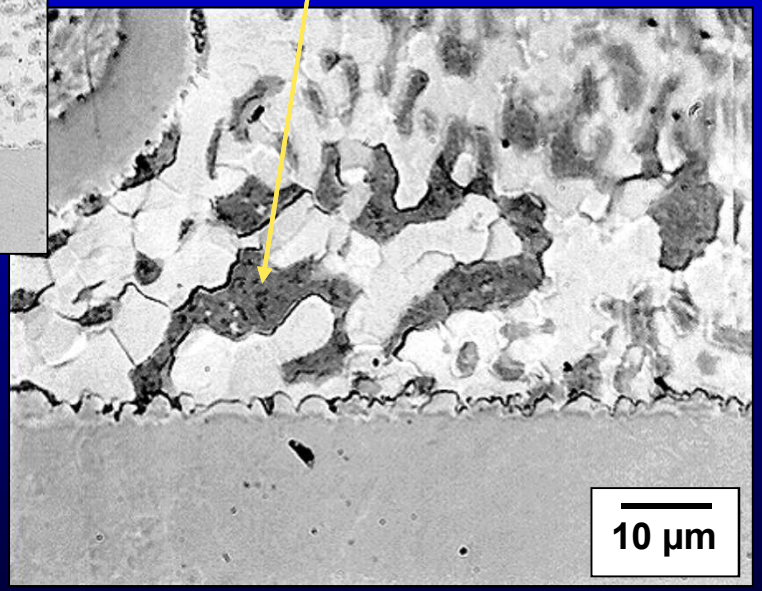
Damage model — *????*

Improved the prediction fidelity by incorporating a "microstructure feedback" variable in the constitutive equation: Pb-rich phase size.

-40° C / 85° C 500 cycles

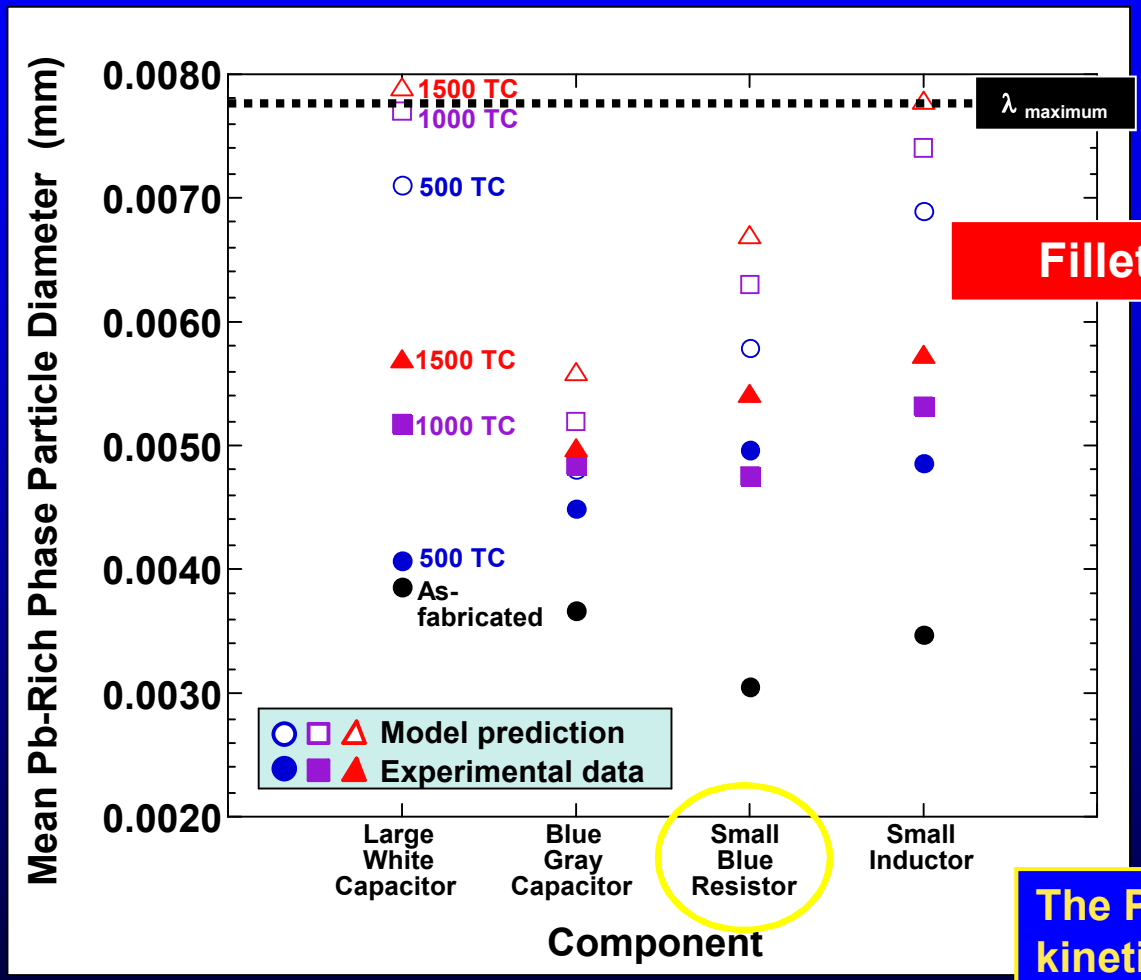


Pb-rich phase coarsening

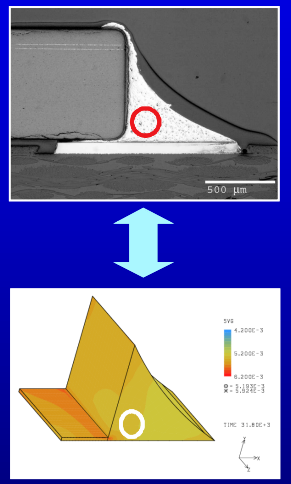


The Pb-rich phase coarsens with exposure to temperature *and* when undergoing deformation.

The predicted, Pb-rich phase sizes were compared very well to experimental measurements in the gap and fillet regions.



Fillet



The Pb-rich phase coarsening kinetics were recently modified to improve the prediction fidelity.

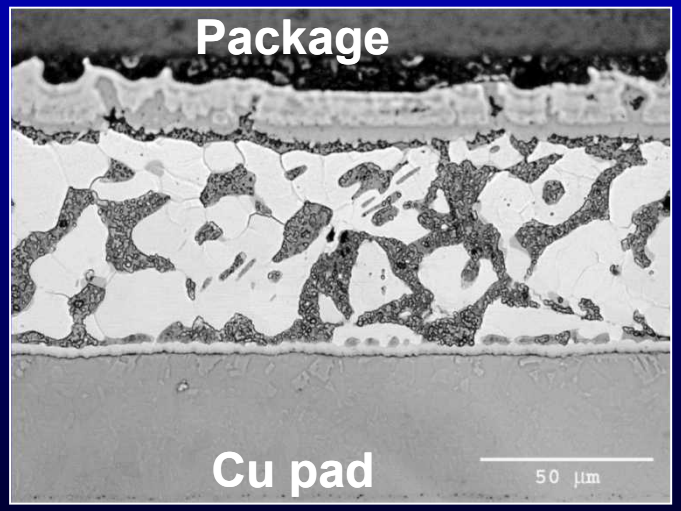
Pb-rich phase particle coarsening will progress towards the initiation of fatigue crack damage in the solder.

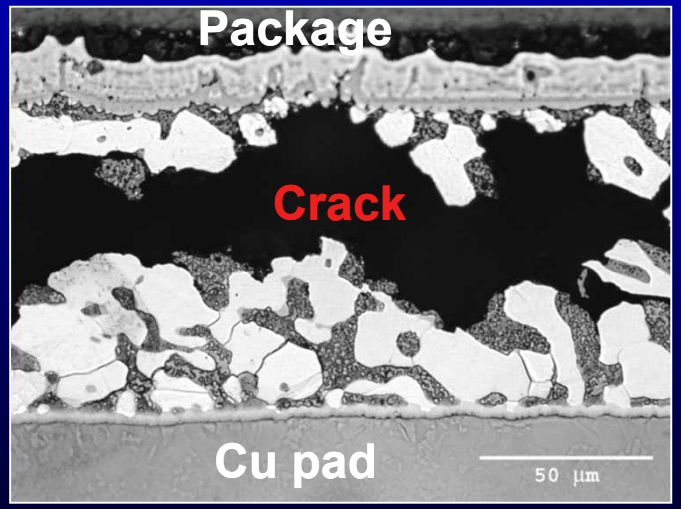
Pb-rich Phase particle coarsening

Maximum Pb-rich phase size λ

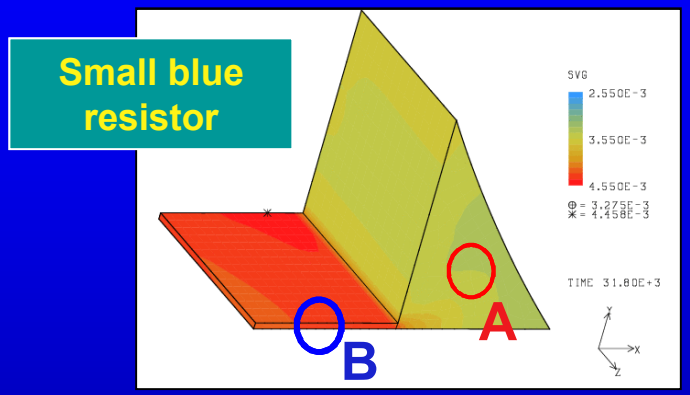
Fatigue crack initiation and growth

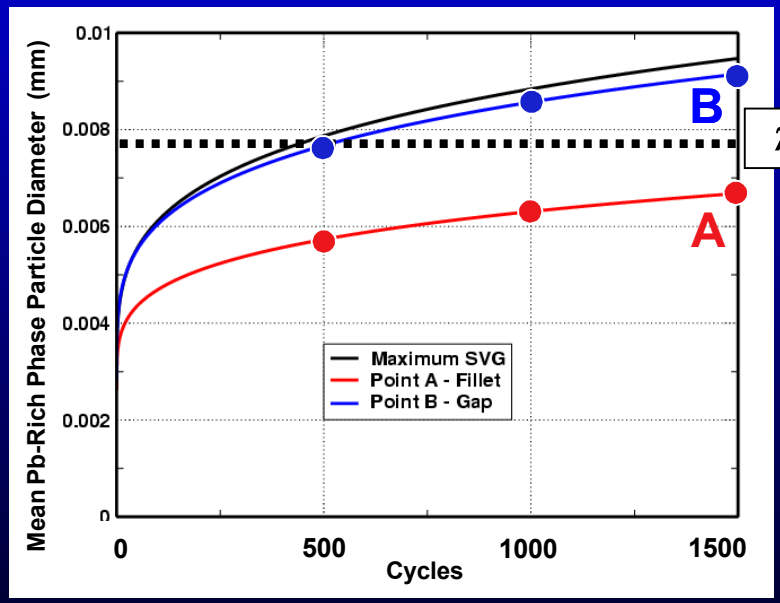
$\lambda_{maximum} = 7.8 \times 10^{-3}$ mm

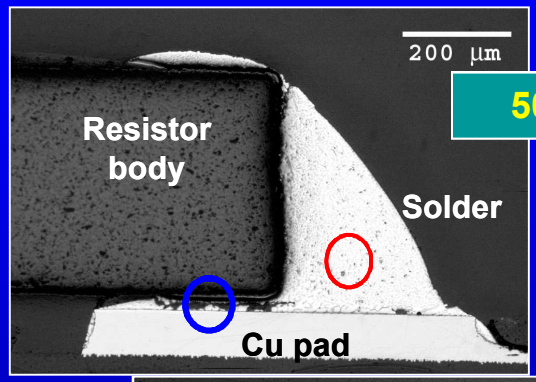


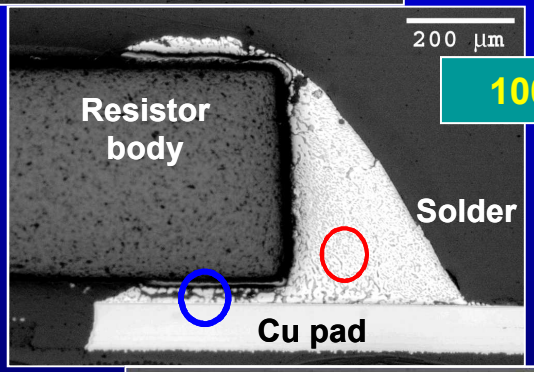


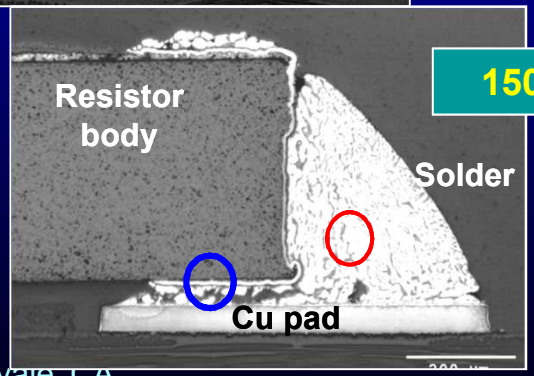
The predicted, limiting Pb-rich phase size - "pseudo damage parameter" - compared favorably to observations of cracks



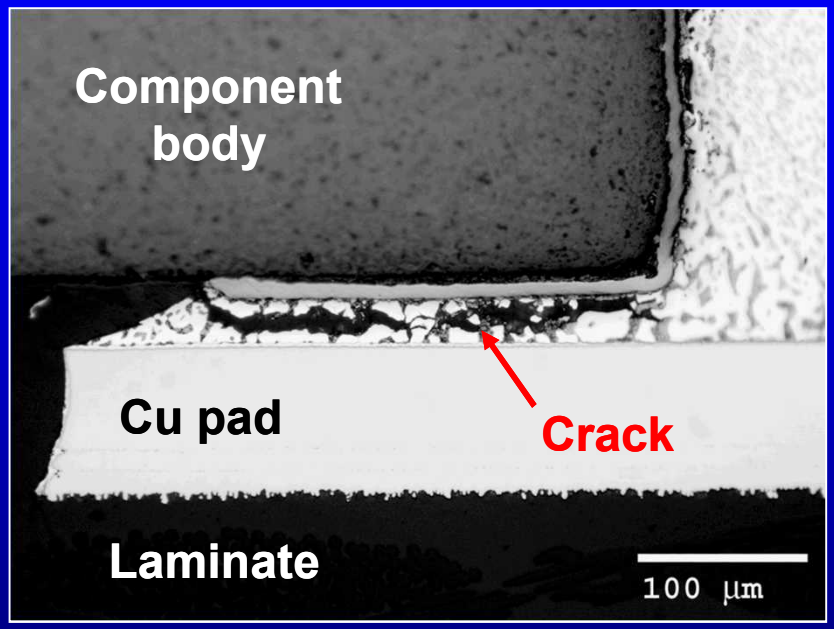


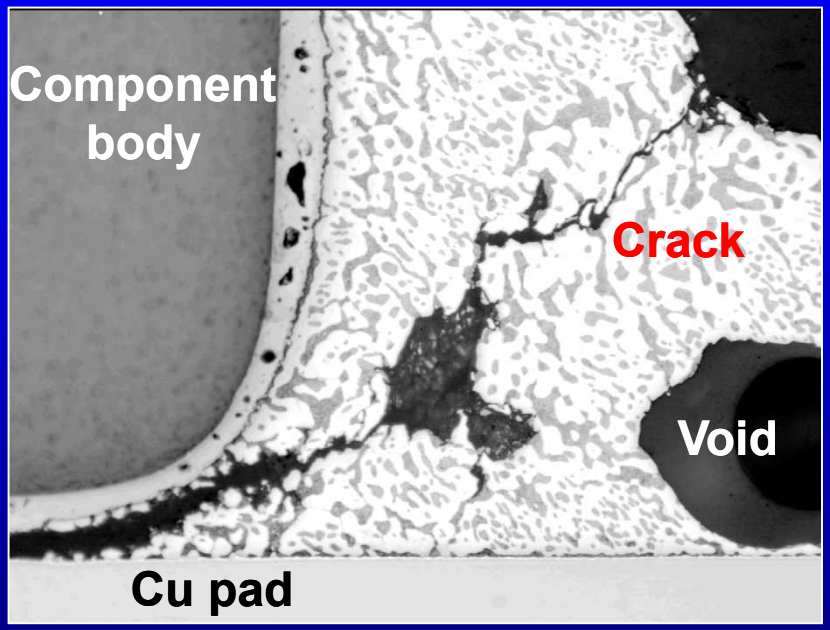






A long-term goal is to incorporate a damage metric into the Sn-Pb model as was done for the Pb-free model.





- The damage metric would be an added parameter in the UCP constitutive model.
- However, developing such a metric will require fatigue testing to establish crack growth behavior.

The UCPD constitutive model will be considered for the Sn-Pb solder.

- The unified creep-plasticity (UCP) constitutive equation was constructed from the stress-strain and creep data:

$$d\varepsilon/dt_{ij} = f_o \sinh^p[\sigma/(\alpha D_\omega)] \exp(\Delta H/RT)$$

- A damage parameter, D_ω, was introduced to track crack development:

$$D_\omega = (1 - \omega)D$$

- The damage metric, "D_ω" will be determined by isothermal fatigue tests performed on ring-in-plug (RIP) samples.

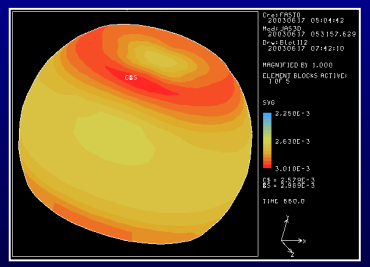
Through the Lockheed Martin/Sandia Shared Vision Program, the CompSIR© model was transformed into the SIP© software

Solder Interconnect Predictor, SIP

GUI Input + CompSIR© Model = GUI Output

- JAS 3-D
- UNIX™ platform
- PC or workstation

- Package geometries
- Interconnection materials
- Material properties



Geometric distribution of deformation represented by (Pb-rich phase size)

The Solder Interconnect Predictor (SIP)© software was developed under contract with Strikewire Technologies, LLC (Louisville,CO)

The format described below for the SIP© UNIX™ version is being used to develop the SIP© Windows ™ version

- **Package geometries**
  - Ball grid array (BGA)
  - Chip scale package (CSP)
  - Gull wing packages (e.g., SOICs, SOTs, QFPs, etc.)
  - J-leaded packages
  - Flip chip (FC) package
  - Diodes
  - Passive chip devices (e.g., resistors, capacitors, etc.)
  - Leadless ceramic chip carriers (LCCC)

The Solder Interconnect Predictor (SIP)© software

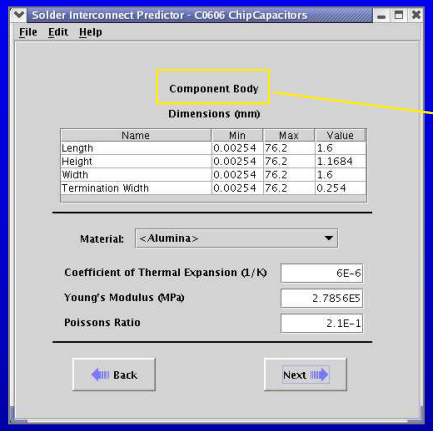
- **Interconnection materials**

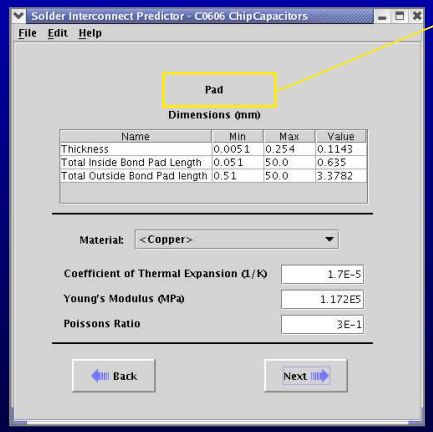
Component	Alumina (resistors and LCCCs), titanate (capacitors), glass (diodes) overmolding (PEMS), interposer (area array), and Si (die for FC)
Substrate	Epoxy-glass (FR-4), BT epoxy-glass, polyimide-glass, polyimide-quartz, epoxy-aramid, polyimide-aramid, and alumina (HMCs)
Pad	Cu, AuPtPd (hybrid microcircuits)
Leads	Cu, Fe-Ni-Co alloy
Underfill	

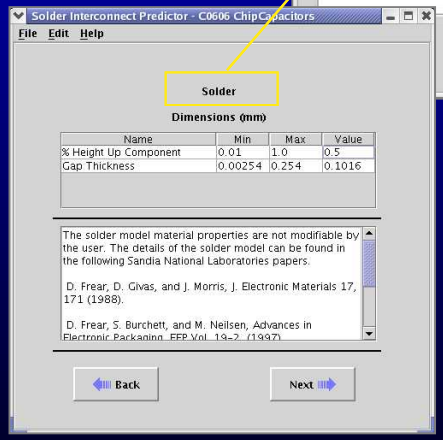
- **Material properties**
  - Elastic modulus
  - Coefficient of thermal expansion
  - Poisons ratio

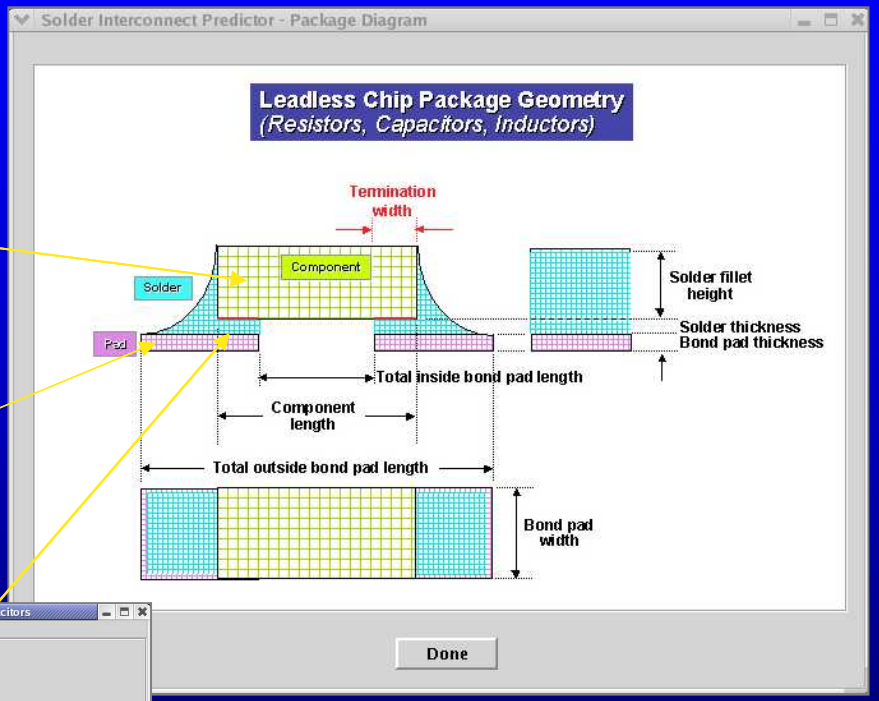
The Solder Interconnect Predictor (SIP)© software

- **Select materials and dimensions**





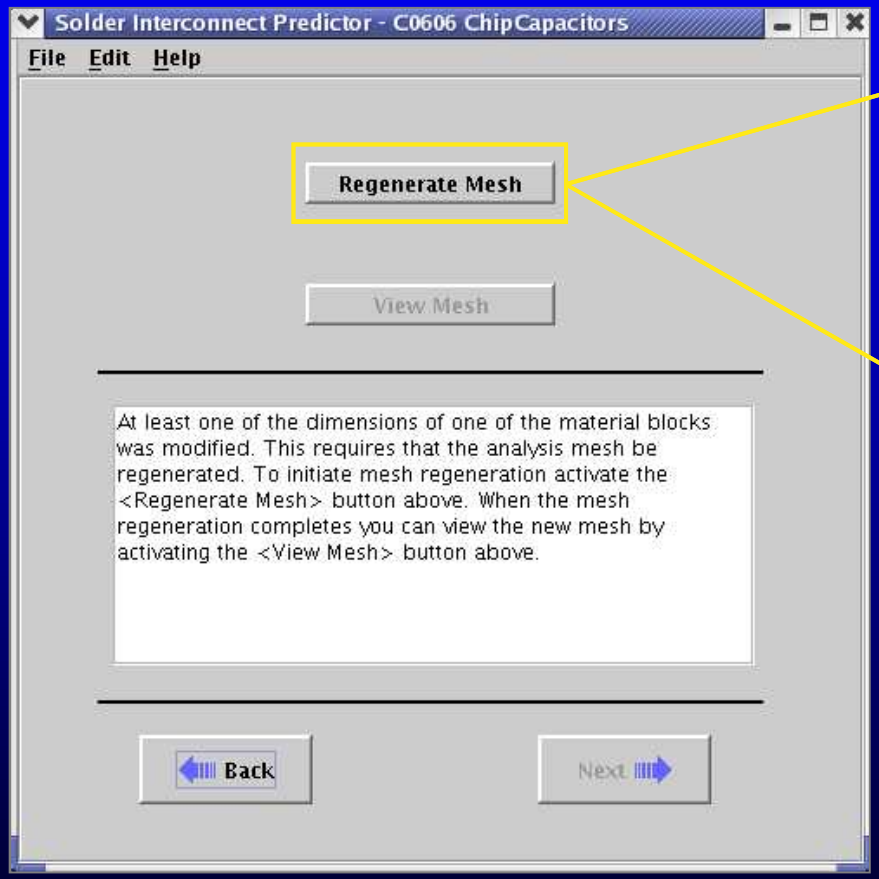


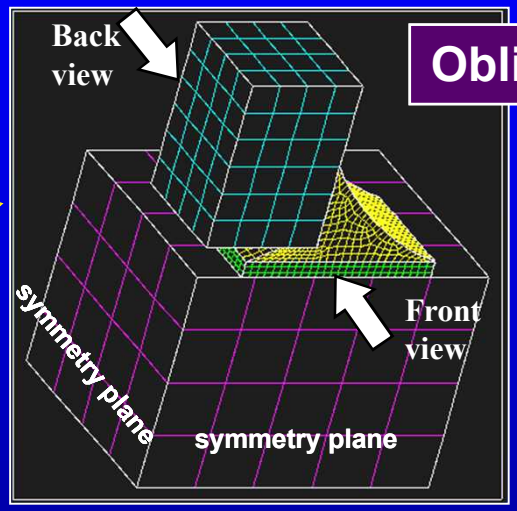


The fillet rise, fillet extent and gap thickness can be changed to reflect variations of manufacturing processes.

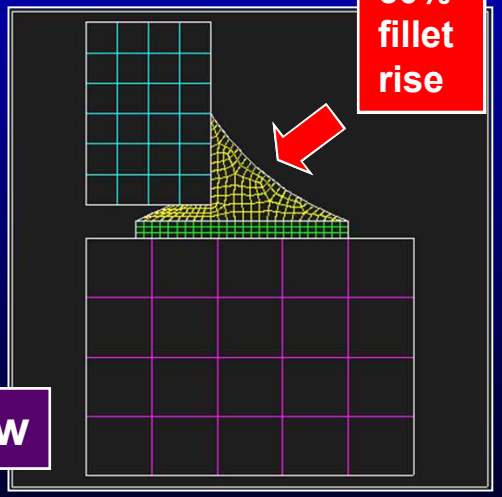
The Solder Interconnect Predictor (SIP)© software

- **Mesh generation routine**





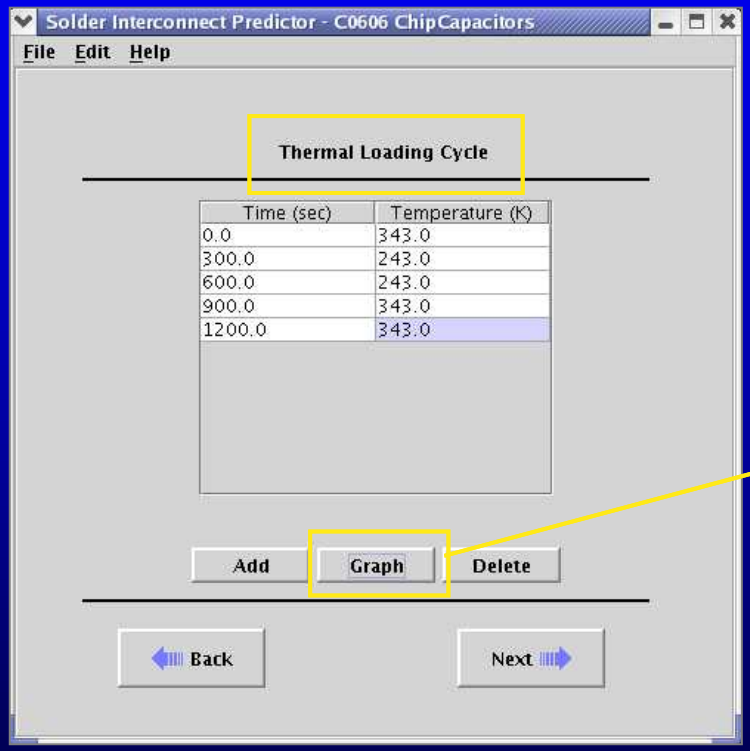
Oblique view

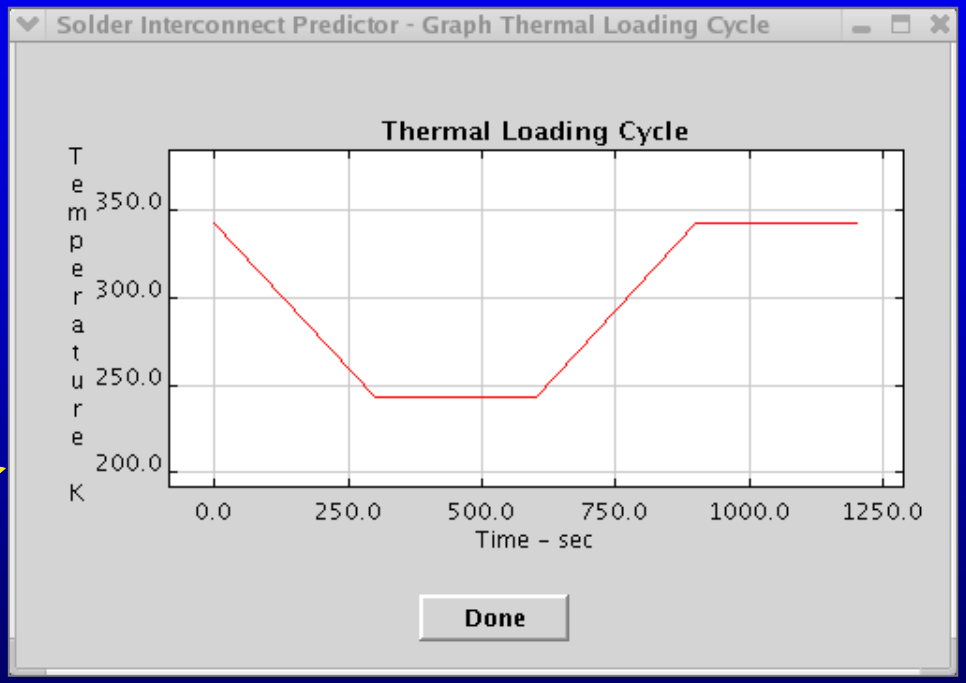


Front view

The Solder Interconnect Predictor (SIP)© software

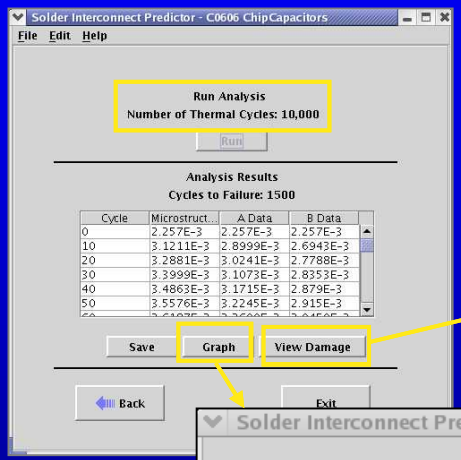
- **Thermal history / thermal cycle**

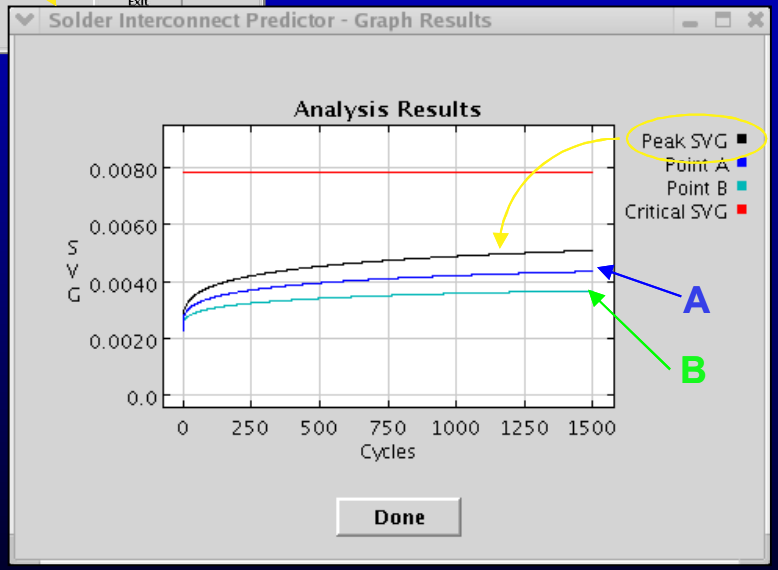




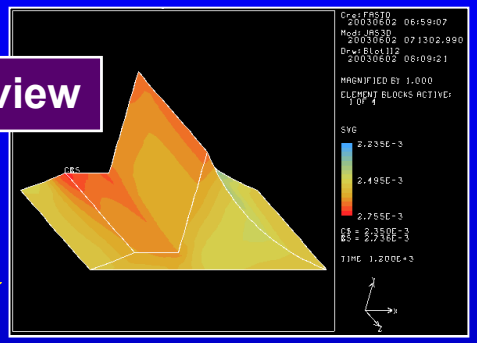
The Solder Interconnect Predictor (SIP)© software

- **SIP© prediction: chip device**

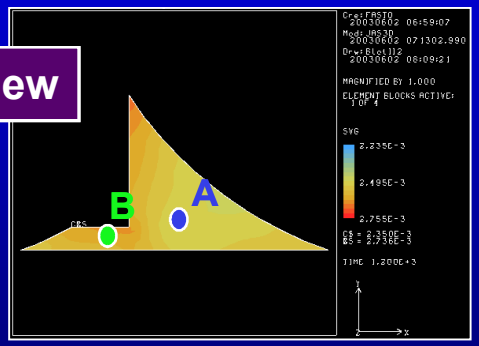




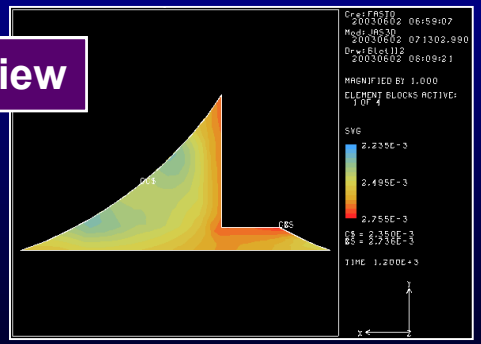
Oblique view



Front view

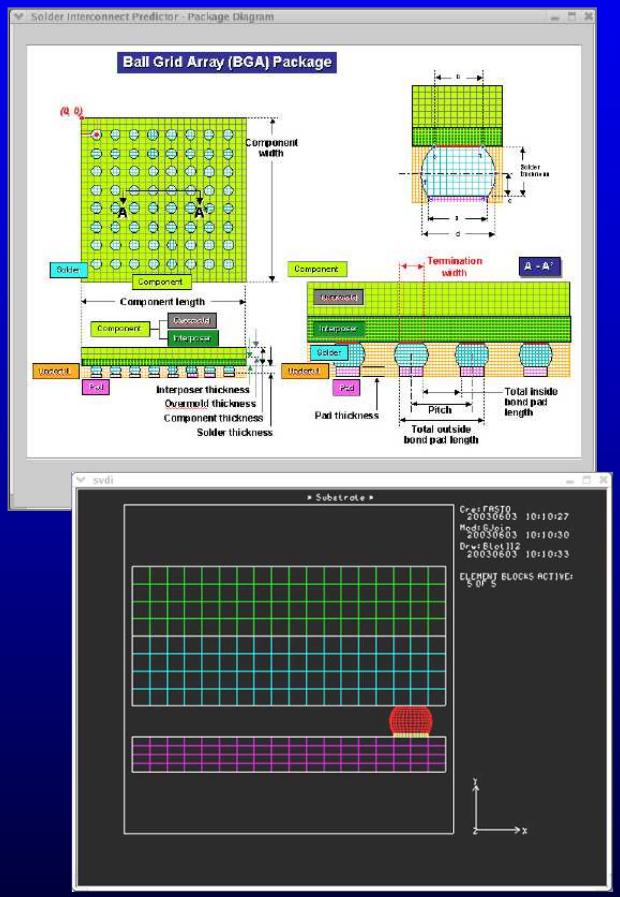


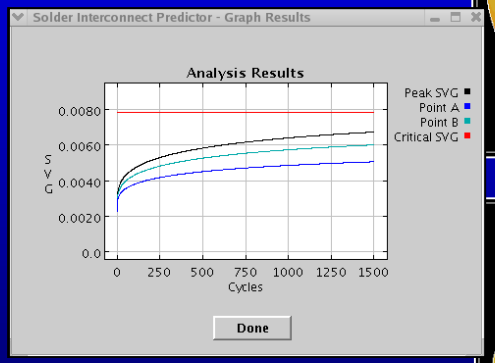
Back view



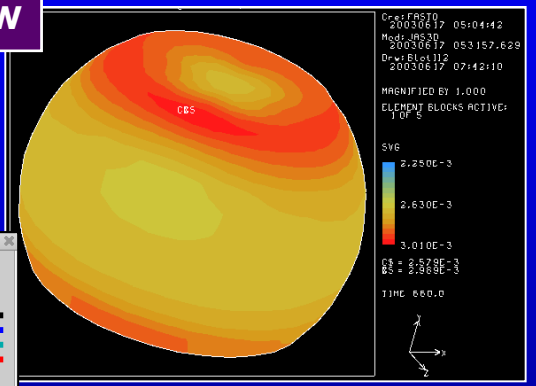
The Solder Interconnect Predictor (SIP)© software

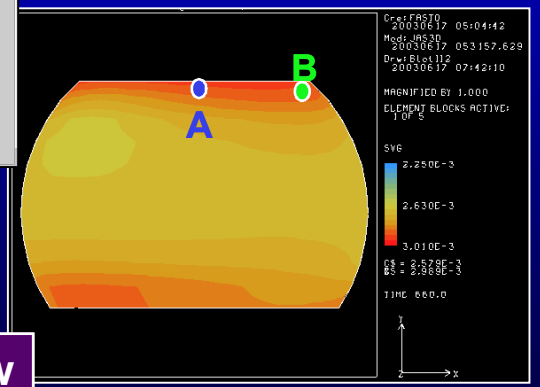
- **SIP© prediction: ball-grid array (BGA)**





Oblique view





Front view

FY06 Update

- **Developed Windows Version of SIP:**

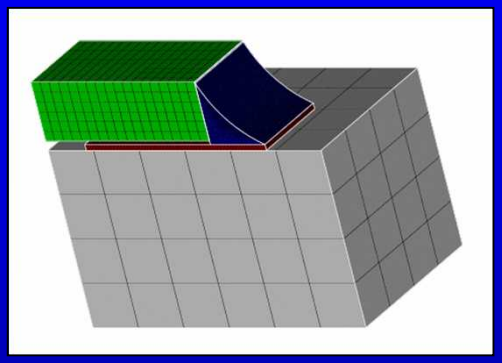
  Kansas State University Computer and Information Science Dept. developed a native Windows versions of the SIP engine:

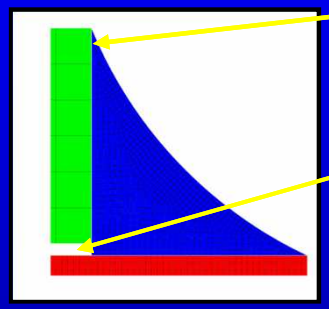
  - **Finite element code JAS-3D**
  - **Mesh generation tools Aprepro, FastQ, Gen3D, Gjoin, Grepos**
  - **Post-processing tools BLOT and Algebra.**

- **Modified SIP JAVA-driver code and linked up the new engine:**
  - **Much work converting the NOT SO PLATFORM INDEPENDENT Java code.**
  - **Significant help provided by KSU.**

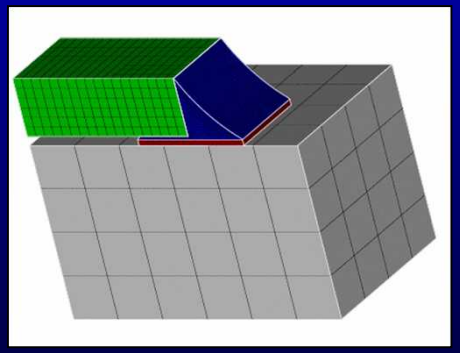
FY06 Update

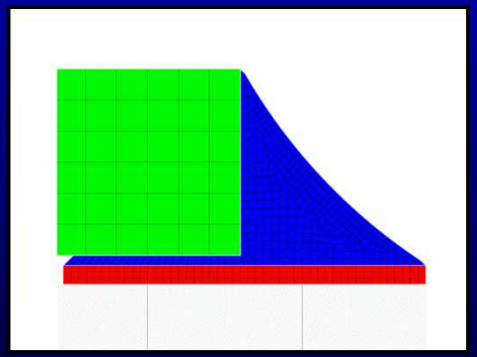
Improved robustness of automated meshing of chip capacitors.





- **Original SIP** – automated meshing failed for some parameter sets.

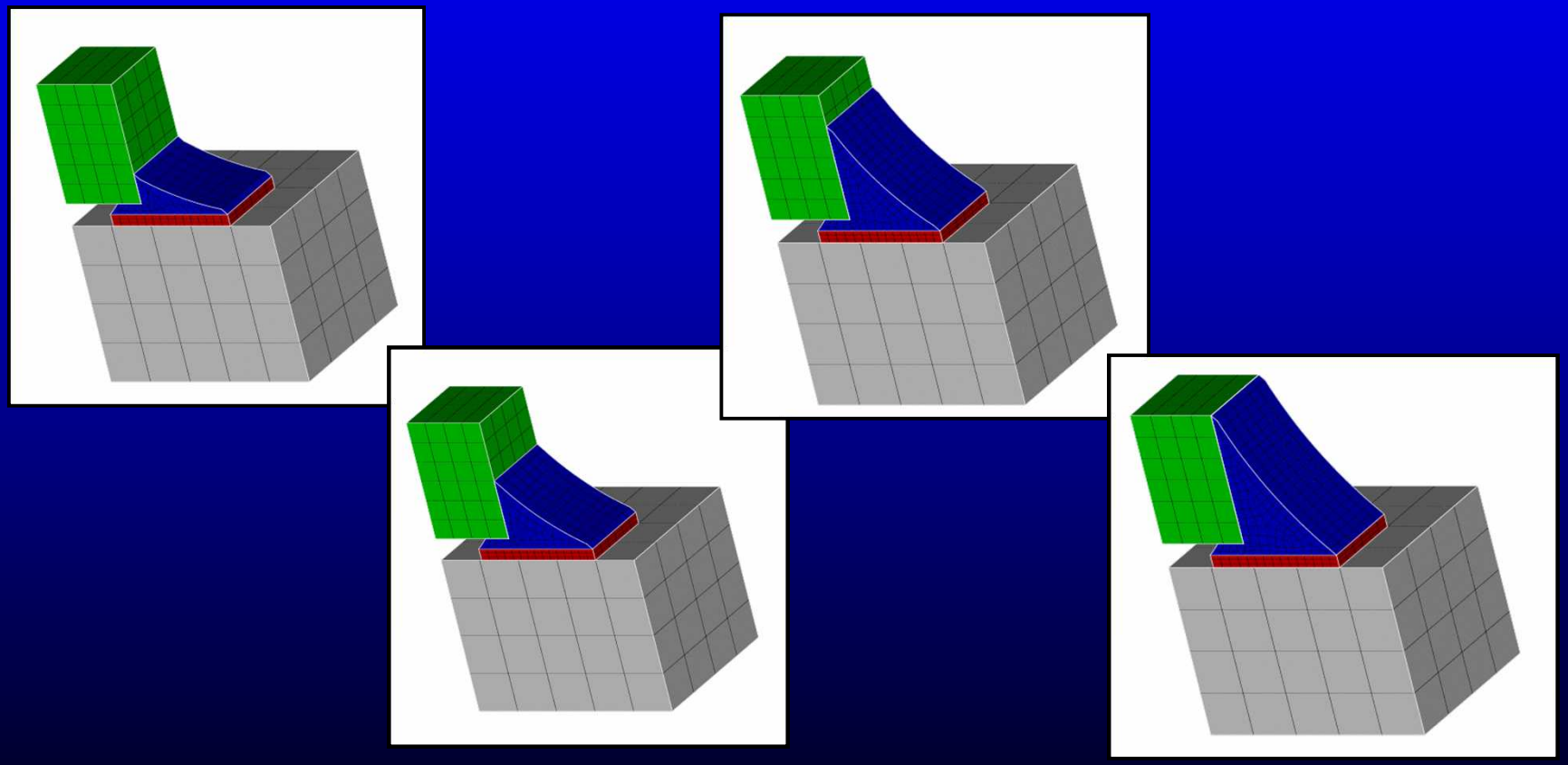




- **Modified SIP** – automated meshing generates quality mesh for parameter sets that had failed with old algorithm.

FY06 Update

Variety of solder fillets automatically meshed by changing a single parameter (fillet height).



FY06 Update

- **Develop SIP that is a true Windows Application**
  - Work performed by Kansas State University
  - Easier to use
  - Easier to install, modify, and maintain

    Doesn't require the installation of separate JAVA software, etc.

- **Implement the damage model and failure criterion into SIP (Sn-Pb) that was developed for the Pb-free UCPD model**

- **Participate in Sn-Pb Solder Failure Round Robin organized by Tom Clifford, LMCO**
  - Modify Sn-Pb solder failure criteria, if needed, based on comparisons developed from this collaboration.