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Circuit Simulations and Testing of the 1-MV LTD for Radiography

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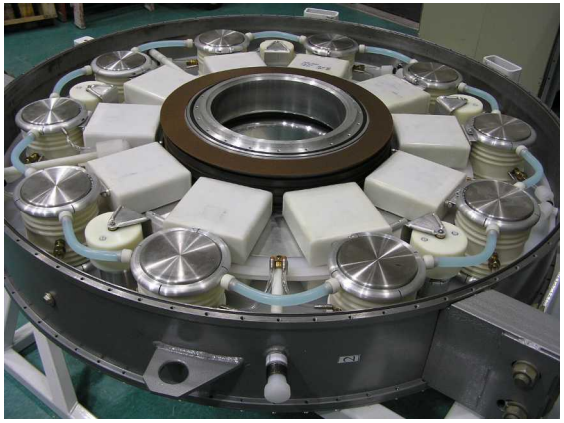
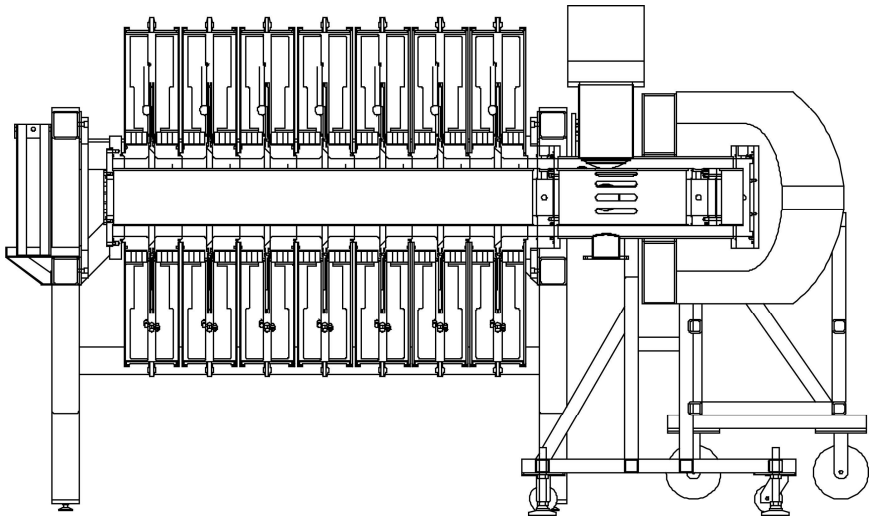
Introduction

- Brief review of the 7-cavity radiographic LTD circuit
- Compare circuit simulations to experimental results
- Discuss fault mode simulations of the 1-MV LTD and a 6.5-MV radiographic LTD.

1-MV LTD Architecture

- Consists of 7 series cavities
  - Each contain 10 parallel bricks of 2 – 20 nF capacitors and a multigap sparkgap switch
  - Each cavity can also have 5 peaking capacitors to increase the peak voltage and decrease the pulse width
- Voltage adds along central vacuum coax
- Tested with a large area electron beam diode load





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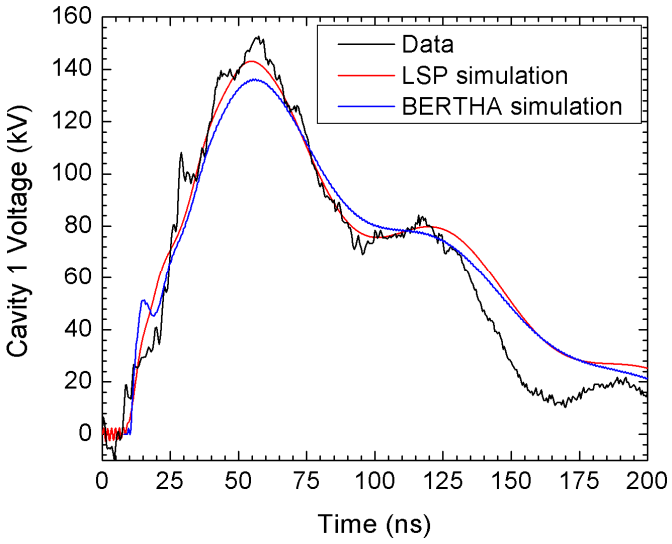
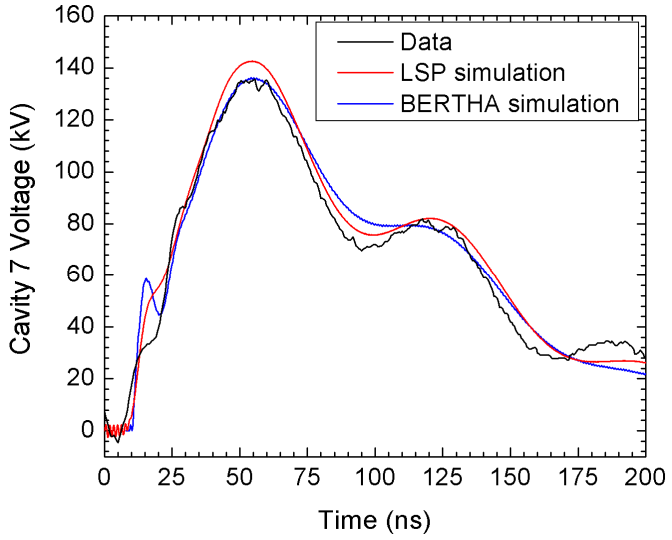
Results of initial testing match circuit simulations and LSP simulations

- Built and tested at HCEI in Tomsk, Russia
- Seven cavities with peaking capacitors (+/- 90 kV charge)
- Tested with e-beam diode load (1.5 cm AK gap)
- BERTHA and LSP simulations compared to voltages from two of the seven cavities





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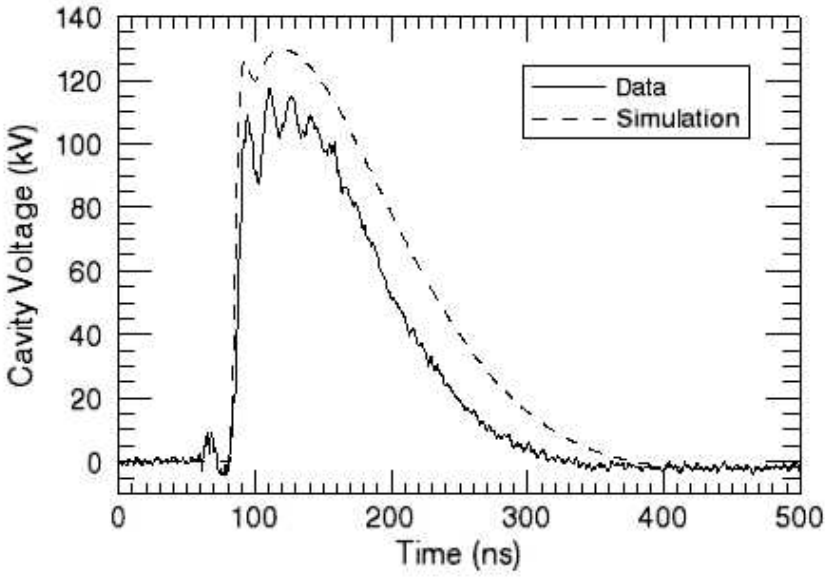
Initial testing at Sandia was performed without the peaking capacitors

- Testing at Sandia National Laboratories
- Each cavity tested individually with resistive load (~1.2 ohm)
- Voltage measurement utilizes DC high voltage cable and resistive voltage divider



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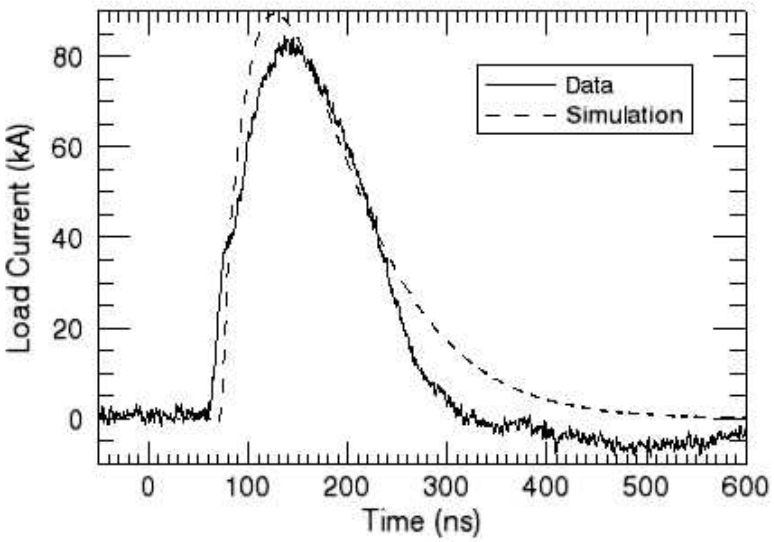
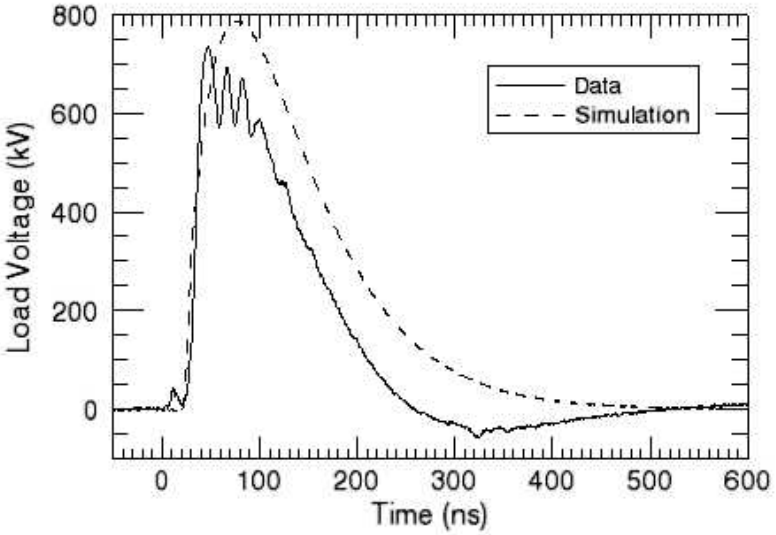
Compare Initial Results to Simulations

- Experiments with 6 cavities, no peaking capacitors, 2.5 cm AK gap, +/- 95 kV charge
- Current measurement – Rogowski coil between last cavity and diode
- Load voltage – Sum of cavity voltages measured with resistive voltage divider





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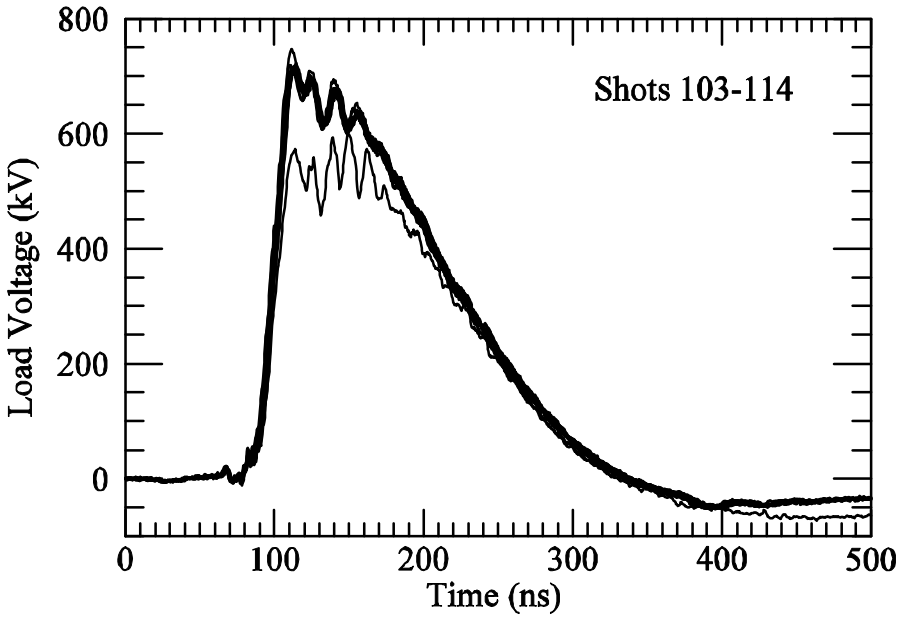
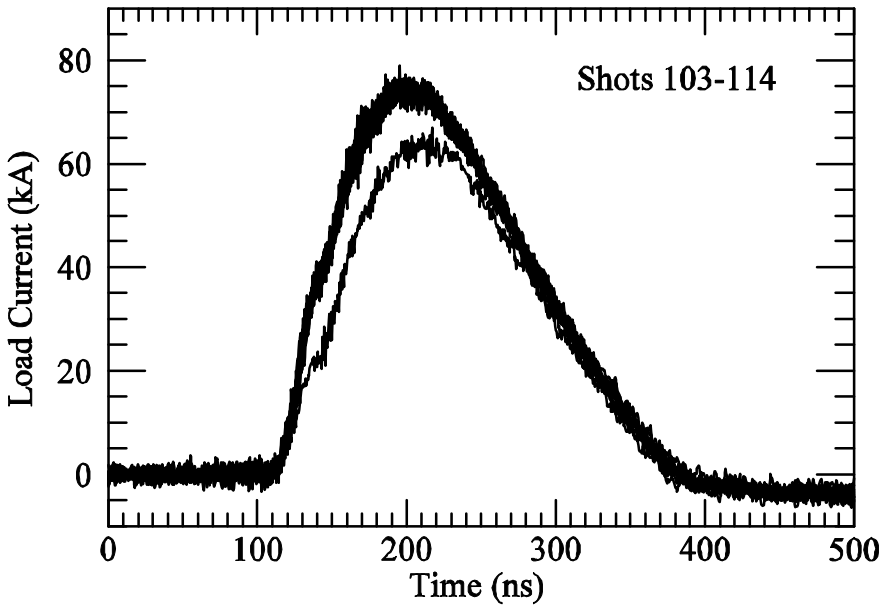
Six series LTD cavities were tested at Sandia for a limited number of shots.

- After initial machine checkout, we fired 24 consecutive shots with the following configuration:
  - Six series cavities
  - +/- 95 kV charge
  - No peaking capacitors
  - 12 consecutive shots at each of two diode AK gap
    - 3 cm and 2.5 cm

3 cm AK Gap Results

- **Total 12 Shots**
  - **Shot 104 – prefire in one cavity**





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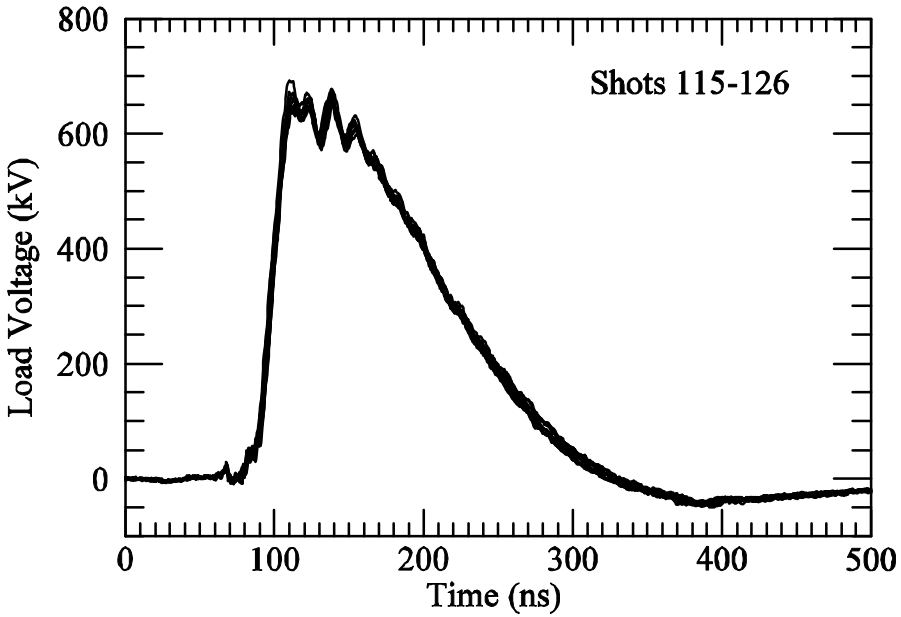
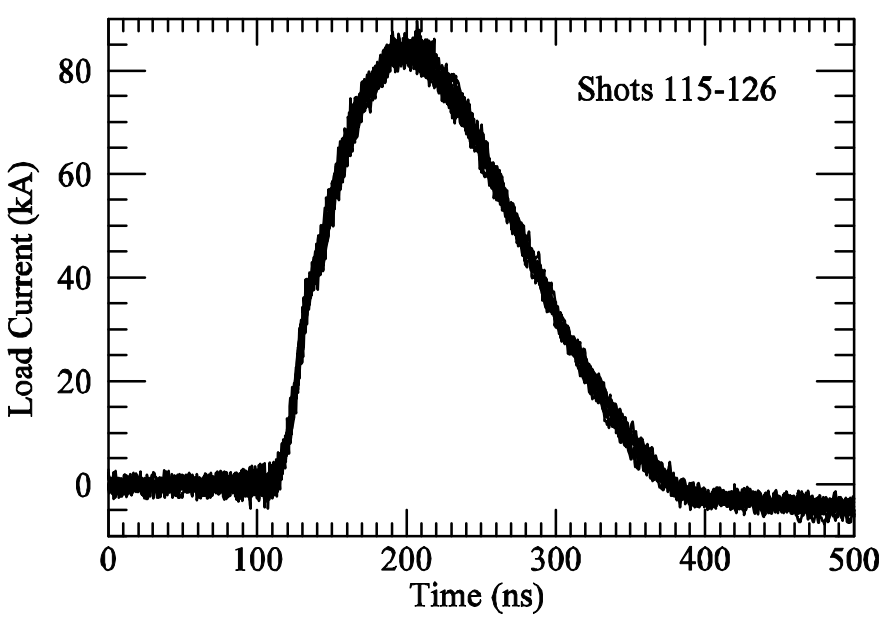
2.5 cm AK Gap Results

- **Total 12 Shots**
  - **No faults observed**





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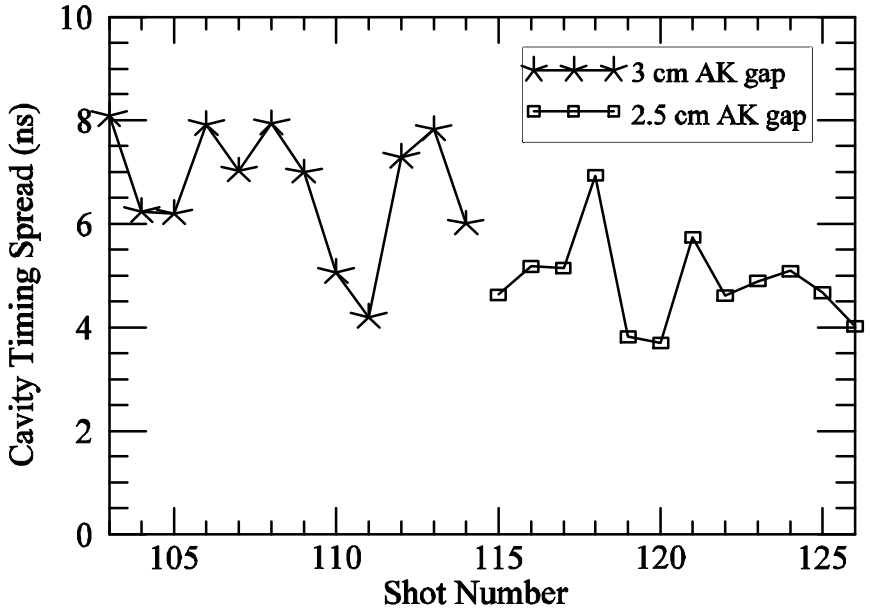
The cavity jitter over 24 shots was less than 8ns.

- Jitter measured as total timing spread from first to last cavity for each shot
- We cannot measure individual switch jitter with our limited set of diagnostics



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Fault simulations have been performed for LTDs with 6 and 48 series cavities.

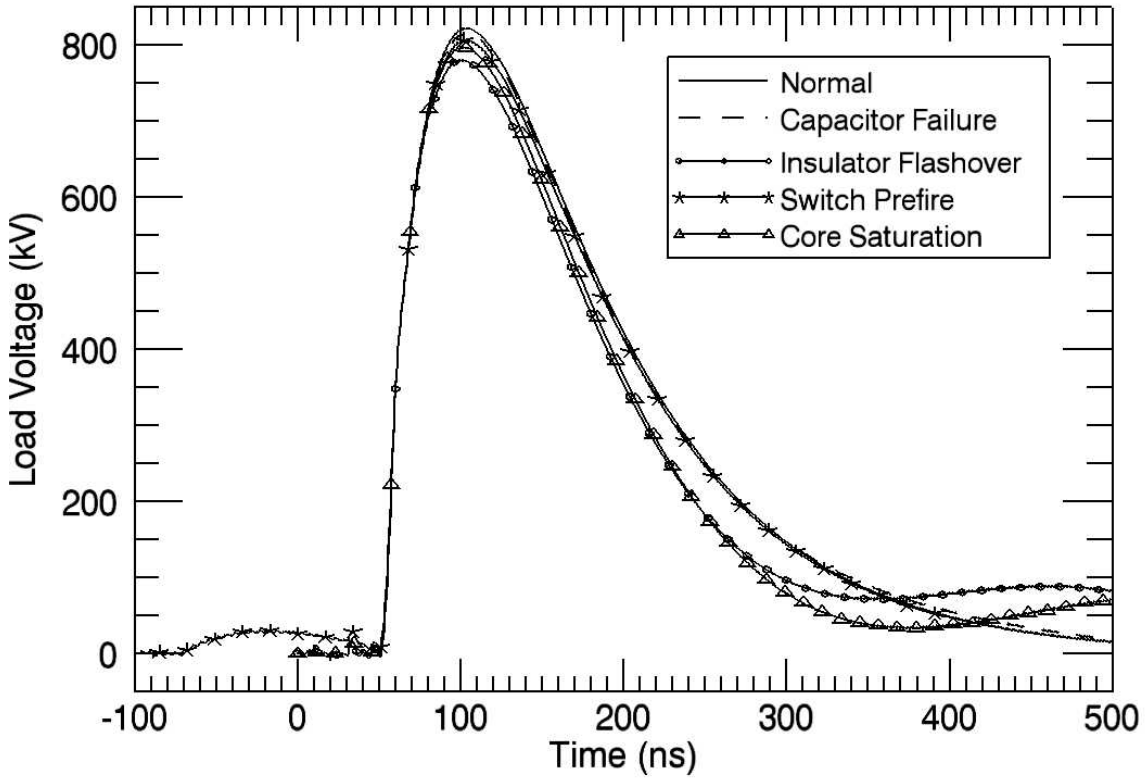
- Simulated fault modes include:
  - Switch prefire (remaining switches triggered after some delay)
  - Switch Jitter
  - Vacuum insulator flashover (when cavity voltage reaches ~90% of peak)
  - Capacitor failure (short one capacitor in one brick)
  - Core saturation (when cavity voltage reaches ~90% of peak)
  - Short circuit load impedance
- Used to determine effect on load voltage and probability of inducing additional faults
- Faults have been simulated for a 6.5 MV radiographic LTD, but apply to all fast LTD cavities of similar design

Fault Mode Circuit Simulations

- Each brick modeled individually to adjust timing of all switches
- Insulator flashover modeled as a switch with series inductance
- Core saturation approximated as a switch with inductance equal to circuit loop inductance without magnetic core
- Capacitor failure modeled as a wire across a single capacitor

Fault Mode Simulations for the 1-MV LTDR

- Peak load voltage decreased by less than 6%
- Pulse width (FW measured at 80% of peak) decreased by less than 4%



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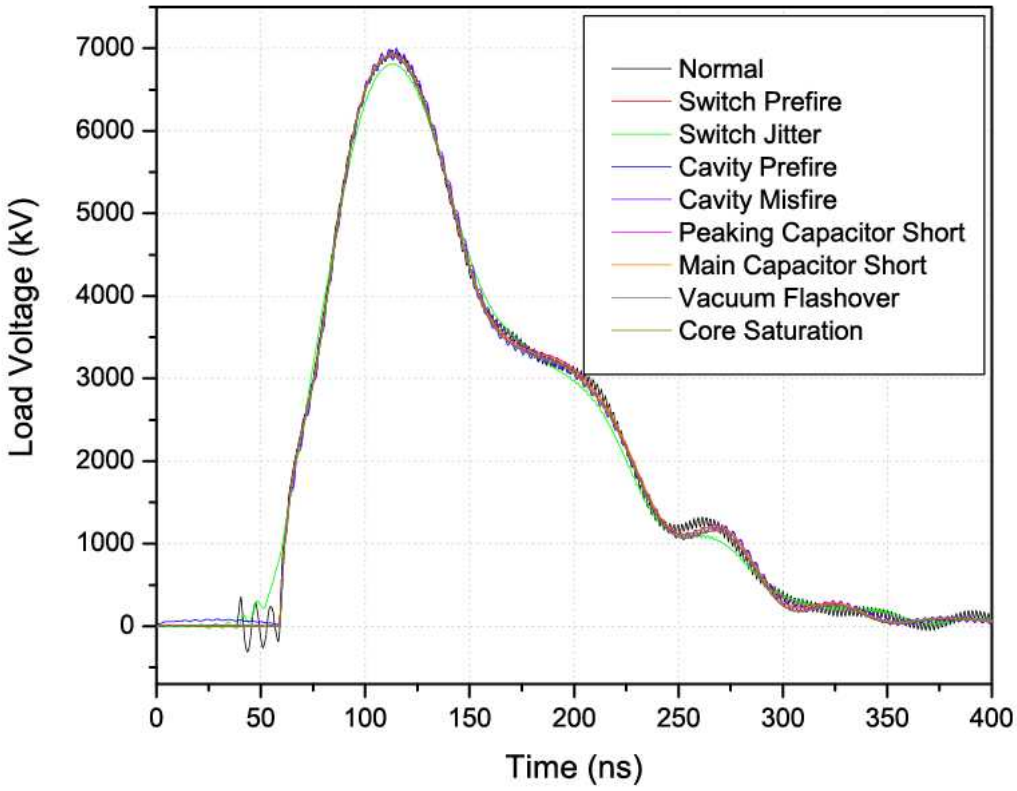
Fault Mode Simulation Results for a 6.5-MV LTD

- This plot shows the load voltage for 6 fault simulations compared to a normal shot
- None of the faults significantly affect the drive pulse
- Only a short circuit load affects all cavities in the circuit, other faults are confined to the cavity where they occur



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Increased Probability of Faults

- Insulator flashover
  - Voltage reversal decreases peaking capacitor life
  - No induced reversal on other cavities
- Core Saturation
  - Voltage reversal decreases peaking capacitor life
  - Insulator flashover likely
- Switch Prefire
  - Decreased main capacitor life (1 fault similar to 40 shots)
- Main Capacitor Failure
  - Slight decrease in capacitor life of other capacitor in the same brick (1 fault similar to 20 shots), other capacitors unaffected.

- None of the simulated faults induce faults in other cavities

Summary

- Six series LTD cavities have been tested with a e-beam diode load
- Simulations of fault modes show that a single fault has little effect on the output pulse shape.
- Fault modes do not induce faults in additional cavities
- The only fault that effects all cavities is a short circuit load, which is of most concern to high impedance LTD designs.

Additional Slides

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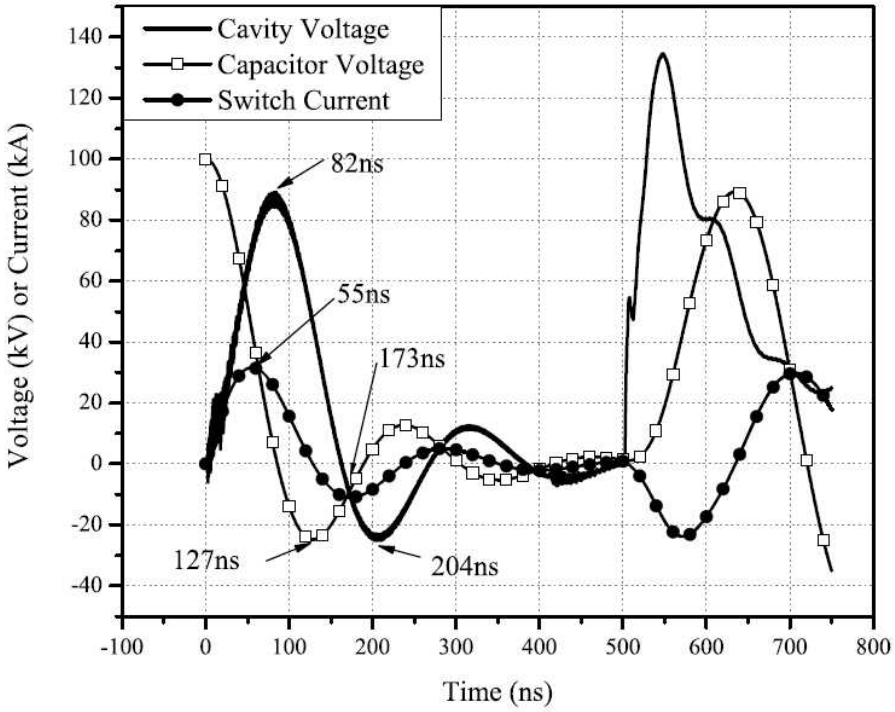
Switch Prefire

- Prefire with long delay used to determine timings for other prefire simulations
- Timing of peak currents and voltages were used in separate simulations

- Result
  - Worst-case timing scenario results in large capacitor voltage reversal
  - Other cavities unaffected



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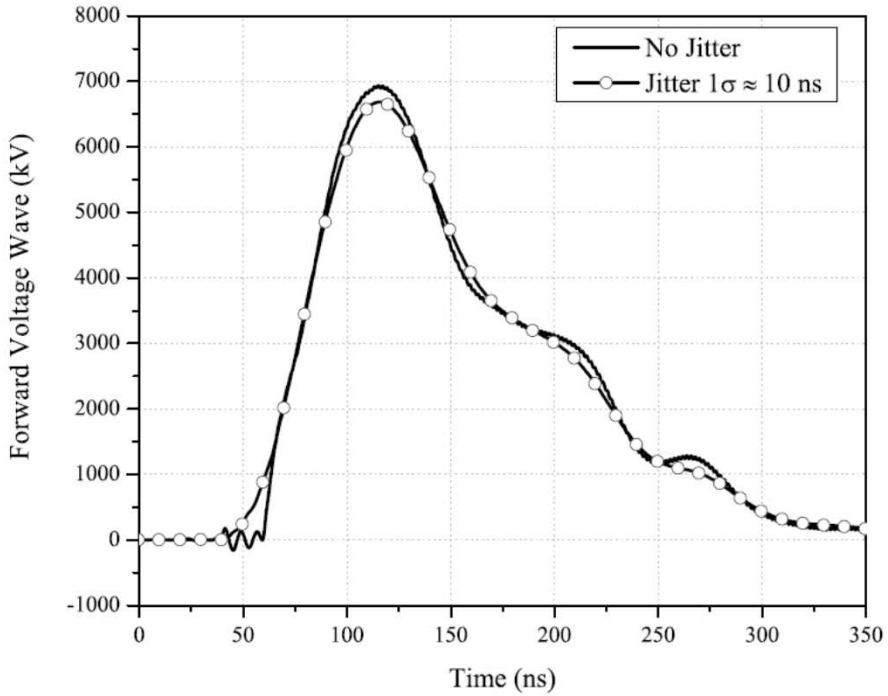
Switch Jitter

- Jitter simulation of 10 ns 1-σ jitter
- Result
  - Smoothes prepulse
  - Decreases peak output voltage by 4%
  - Increases risetime by 13%



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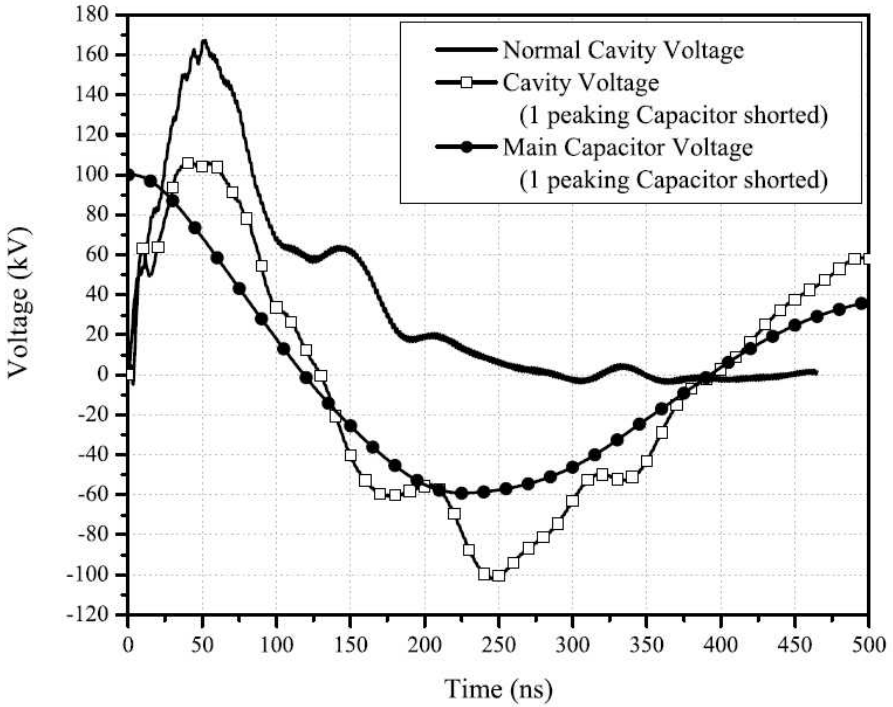
Peaking Capacitor Failure

- One peaking capacitor in a single cavity was shorted
- Result
  - Large cavity voltage reversal
  - Large main capacitor voltage reversal
  - Other cavities unaffected



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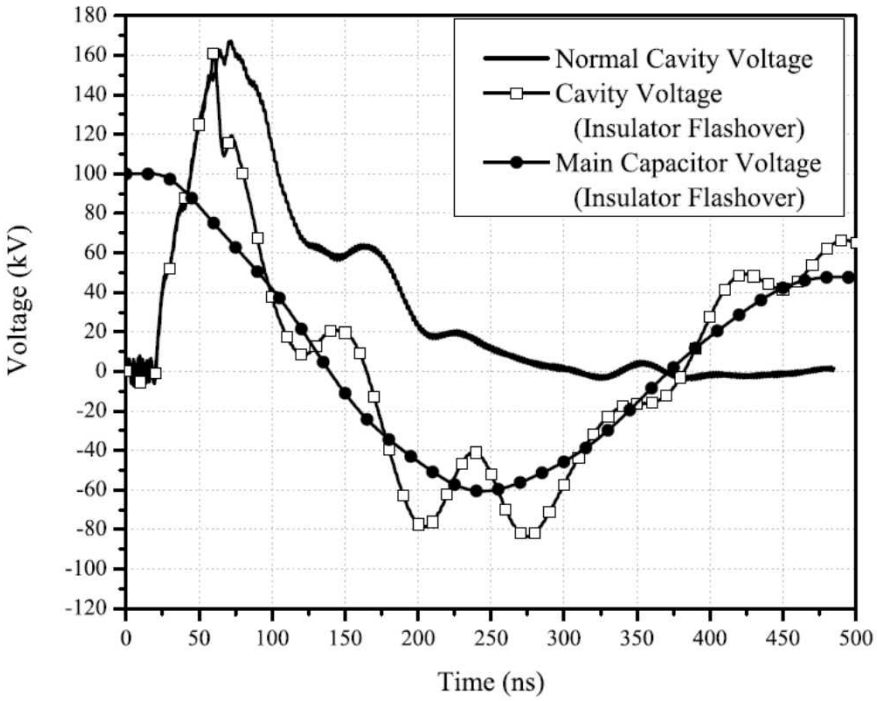
Insulator Flashover

- **Single cavity shorted at 90% of peak output voltage**
- **Result**
  - **Large main capacitor votlage reversal**
  - **Large peaking capacitor votlage reversal**
  - **Other cavities unaffected**



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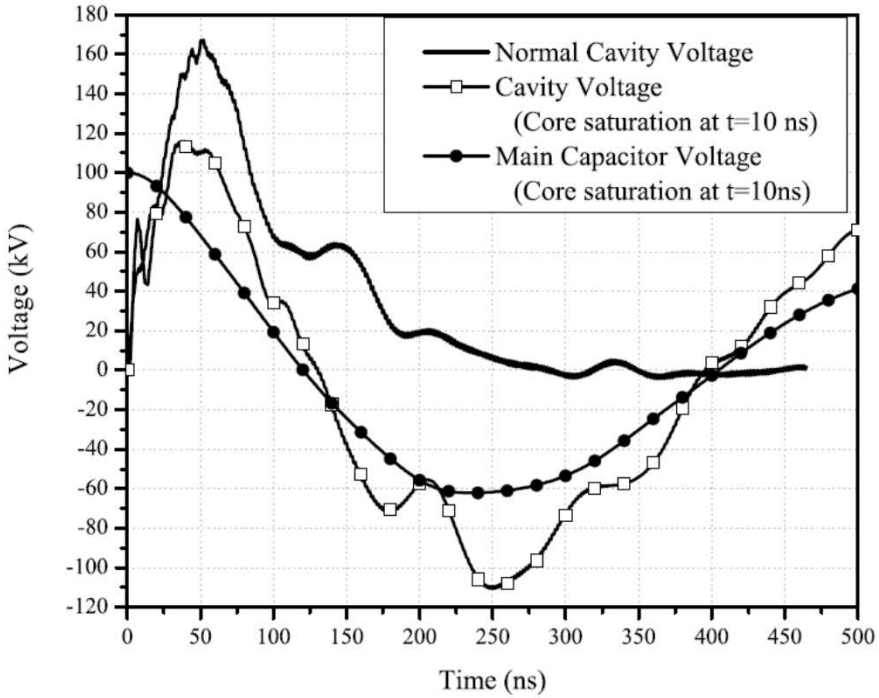
Core Saturation

- Simulated core saturation in one cavity early in output pulse
- Result
  - Large cavity voltage reversal
  - Large main capacitor voltage reversal
  - Other cavities unaffected



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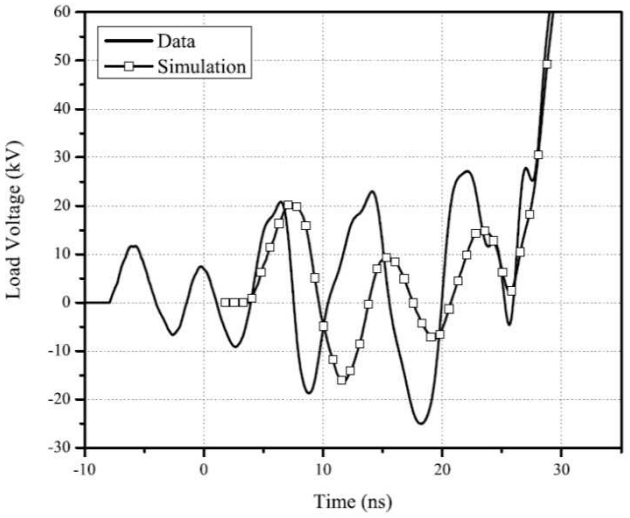
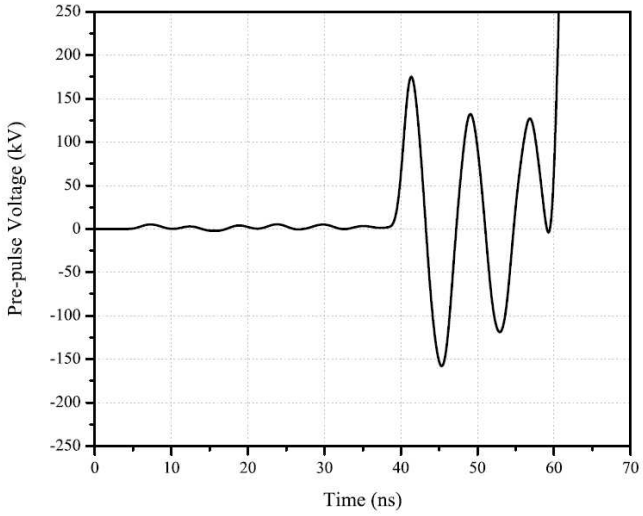
Pre-pulse

- **Simulated 7-cavity LTDR pre-pulse similar to experimental results**
- **Predicted 48-cavity pre-pulse of about +/-150 kV, only 25 ns duration**





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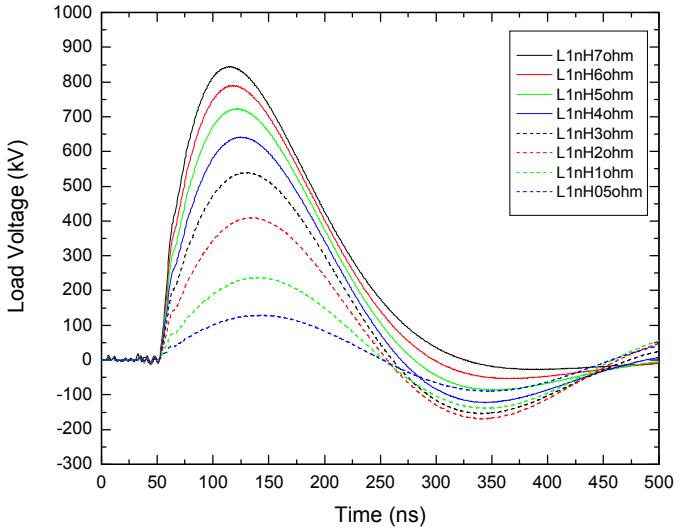
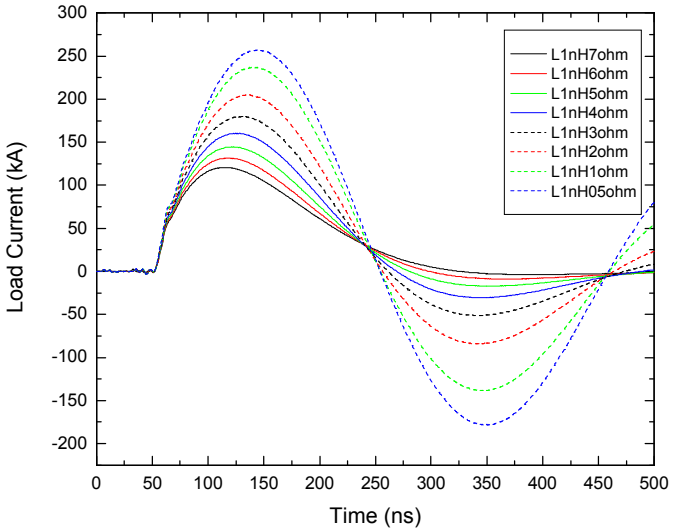
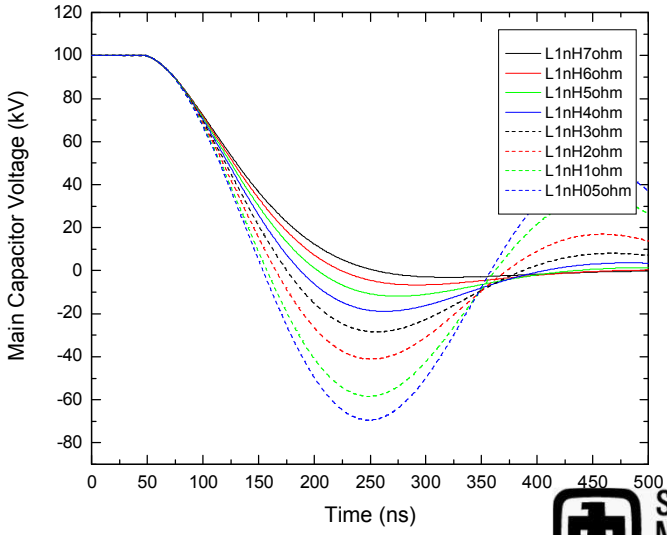
Short Circuit Load Impedance

- **Simulation of load impedance scan for a 7-ohm driver**
- **Result**
  - **Relatively small cavity voltage reversal**
  - **Large main capacitor voltage reversal in ALL cavities**







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