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Introduction to CMOS Technology

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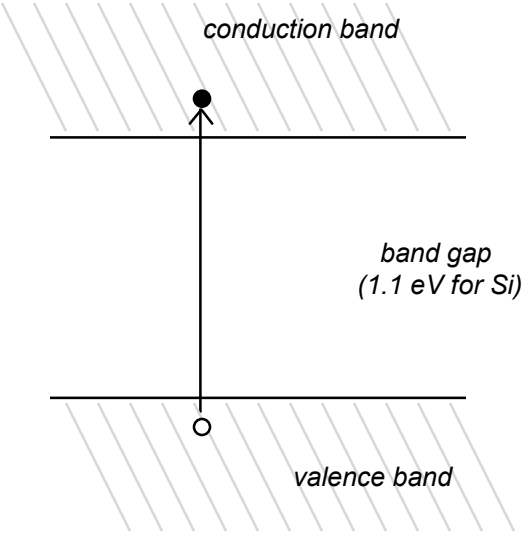
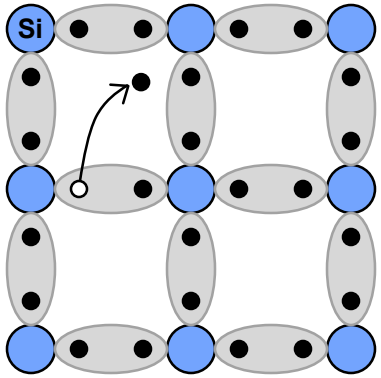
Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company,
for the United States Department of Energy's National Nuclear Security Administration
under contract DE-AC04-94AL85000.

There's a trillion-dollar industry built around it, but basic silicon is a "dumb" material, unable to perform complex functions.





The only straightforward ways to create electron-hole pairs for conducting electricity in intrinsic silicon are thermal excitation or radiation.

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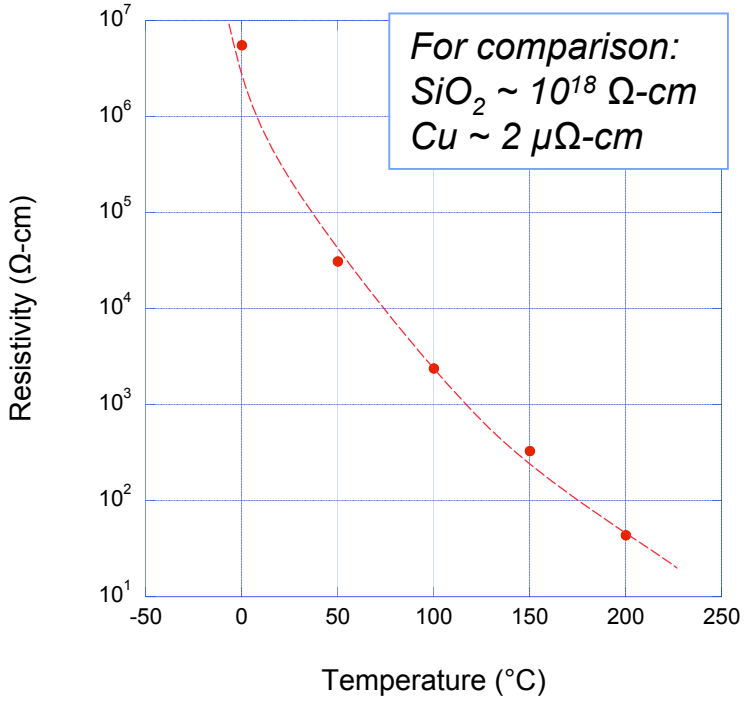
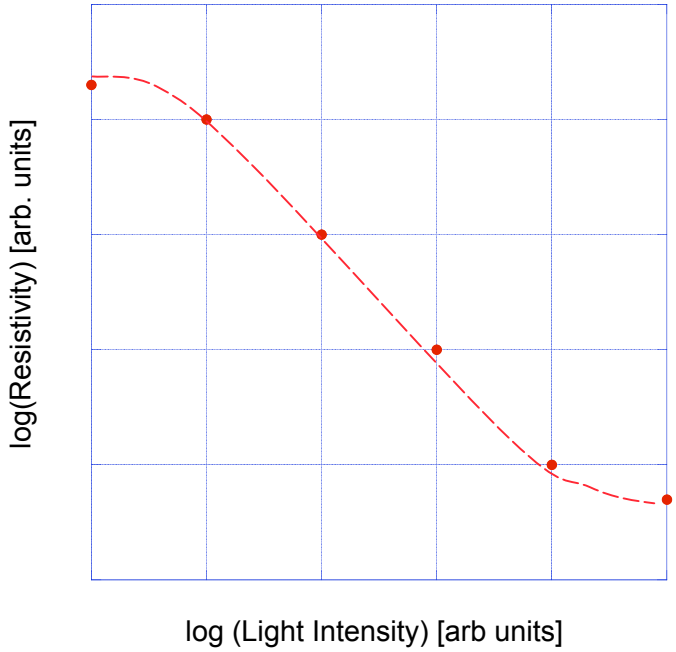
In fact, intrinsic silicon can be used as a thermometer…



$$n_i \propto T^{3/2} e^{-E_g/2kT}$$

…or a light detector.



These devices are just resistors, whose resistance depends on temperature or photon flux.

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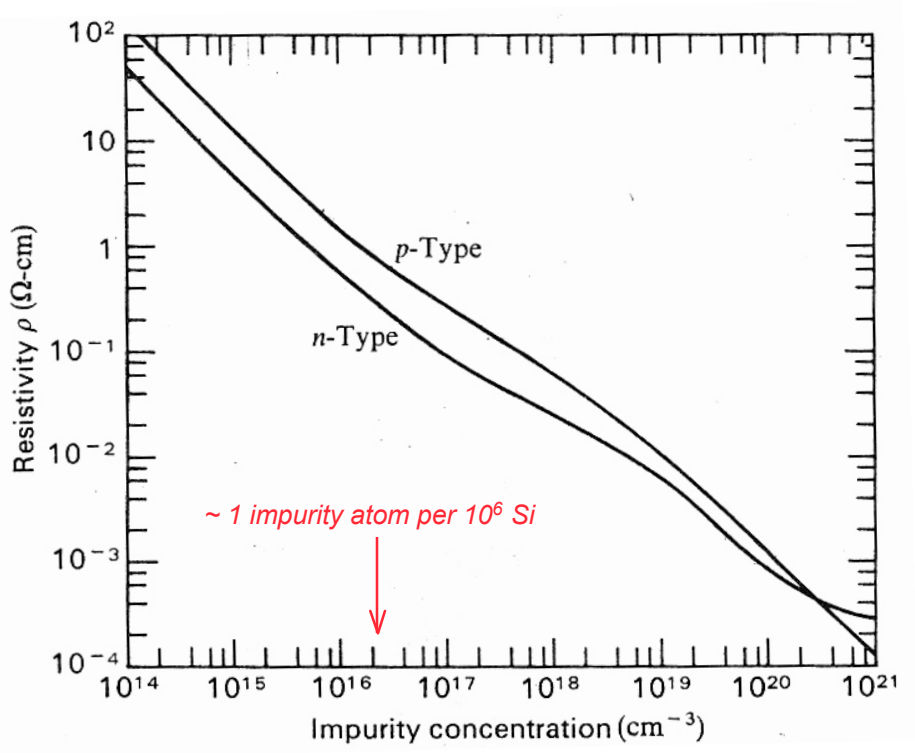
It's easy to change the resistivity of silicon by adding electron donors (usually column V elements) or acceptors (usually column III elements).



N-type: donors, extra electrons.

P-type: acceptors, extra holes.

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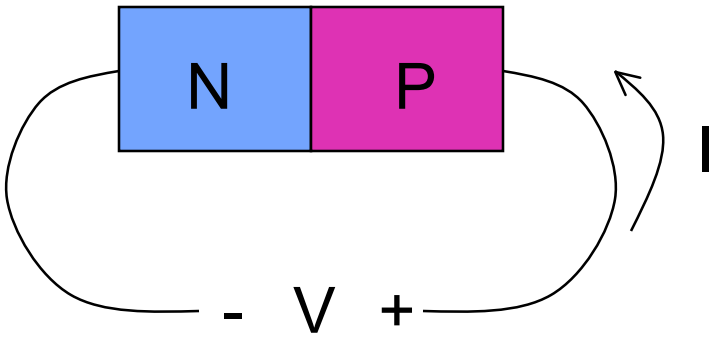
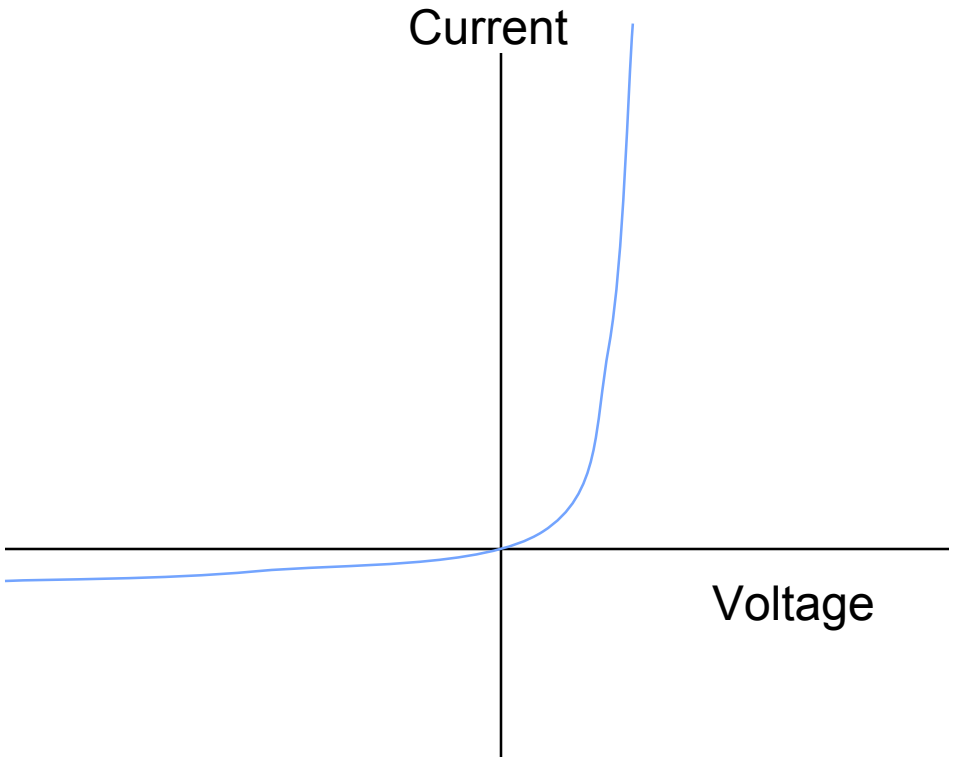
Putting n- and p-type materials in intimate contact with each other creates a *p-n junction diode*





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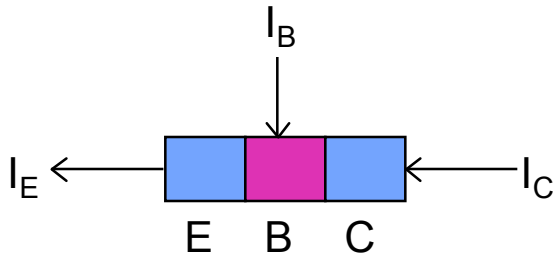
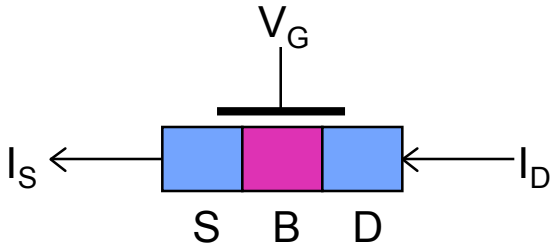
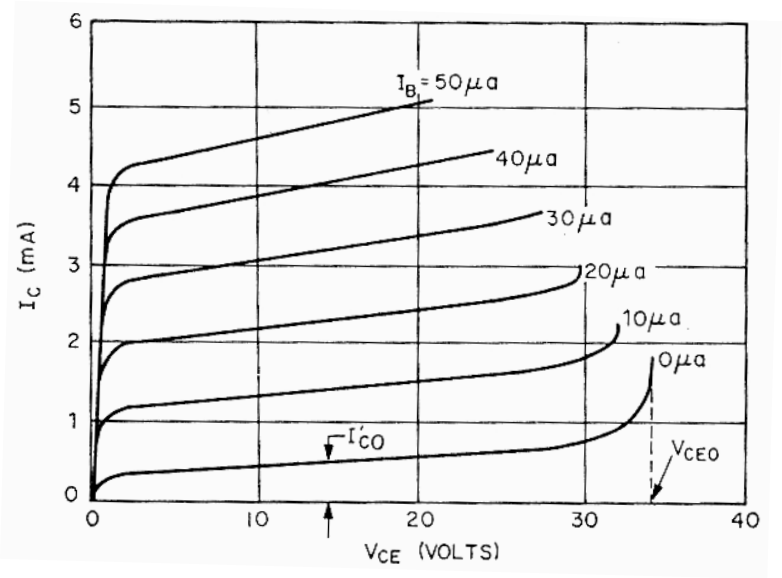
Adding more regions creates even more interesting devices

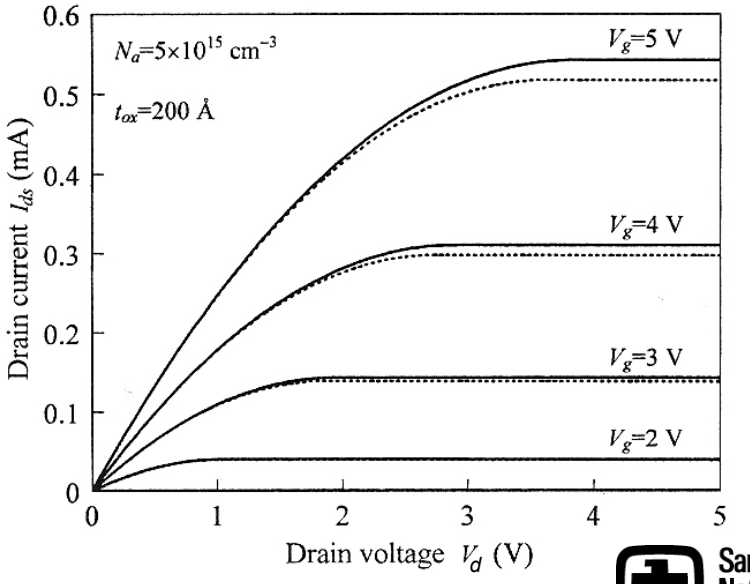


Bipolar junction transistor, current controlled.



MOS field effect transistor, voltage controlled.





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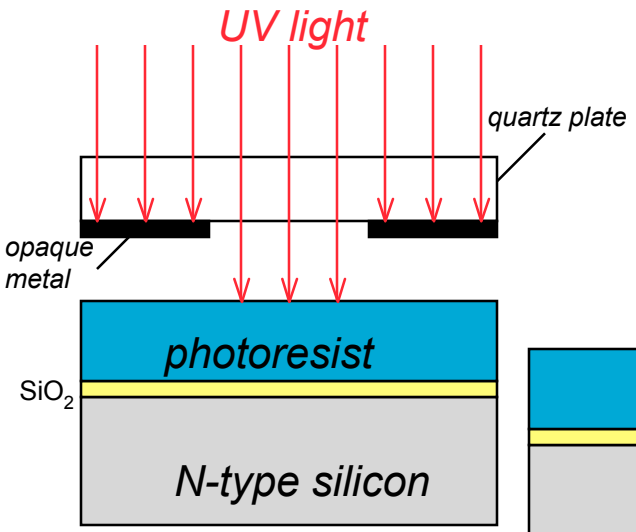
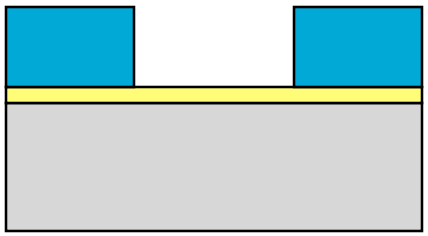
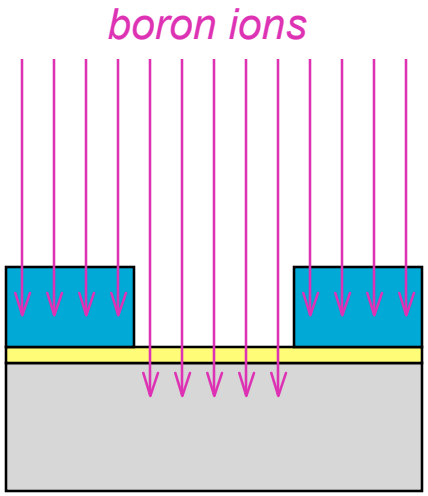
In practice, devices aren't made by moving blocks of doped material together.

The *planar process* creates various doped regions by working from the surface.

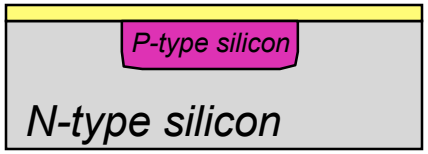




Develop the photoresist, leaving a pattern of openings in the film.



Ion implantation: A beam of energetic ions is used to dope the region of silicon exposed by the opening in the photoresist.



Remove the photoresist, thermally anneal the ion implant damage.

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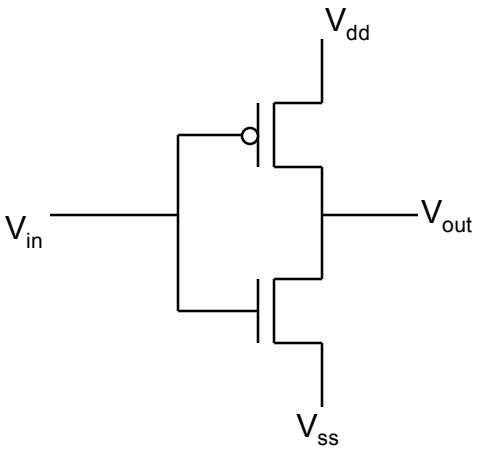
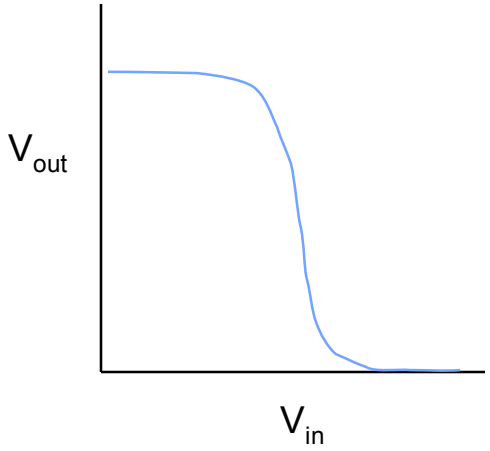
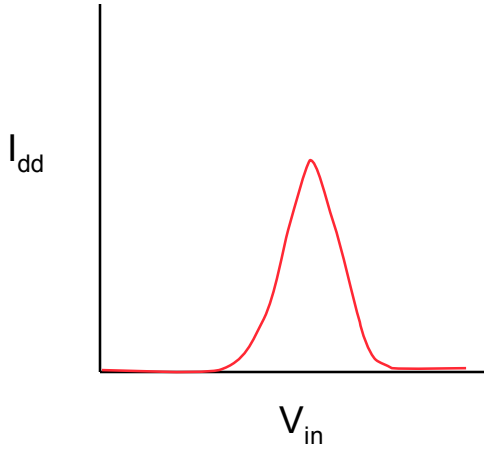
CMOS: Complementary Metal-Oxide-Semiconductor

Both p-channel and n-channel FETs are used in ways that greatly reduce the DC current requirements.

Simplest example: CMOS inverter:







Most ICs are comprised of nearly all CMOS.

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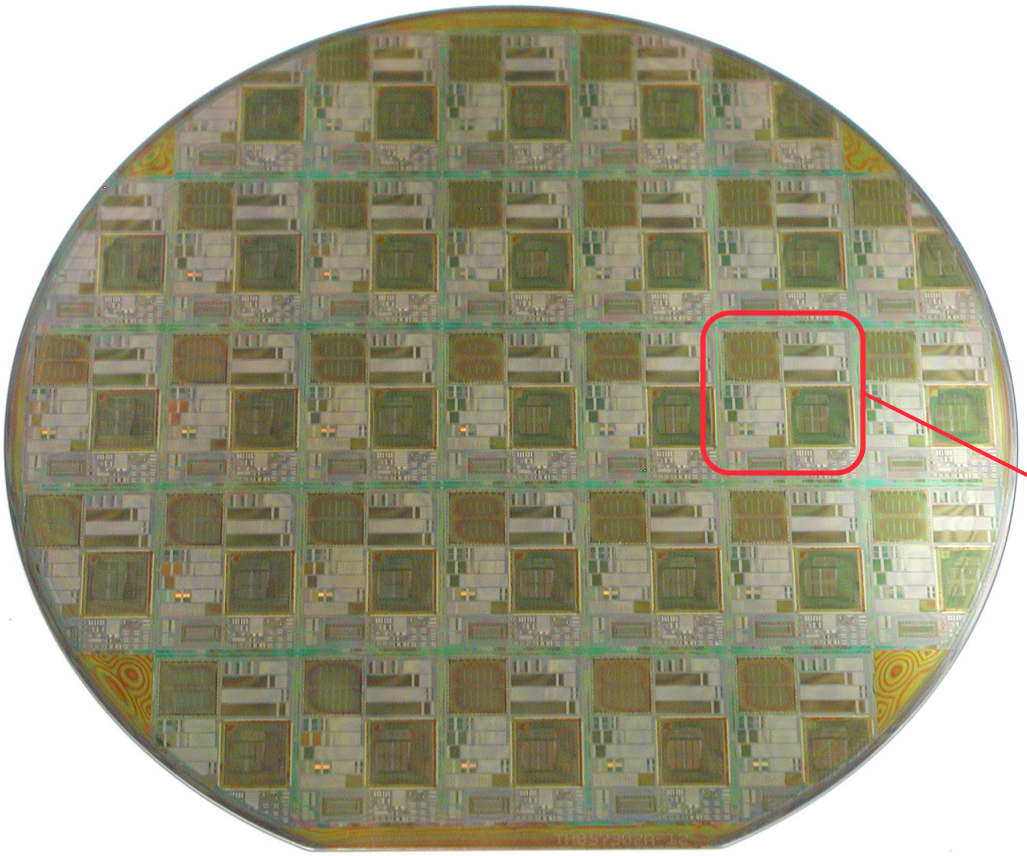
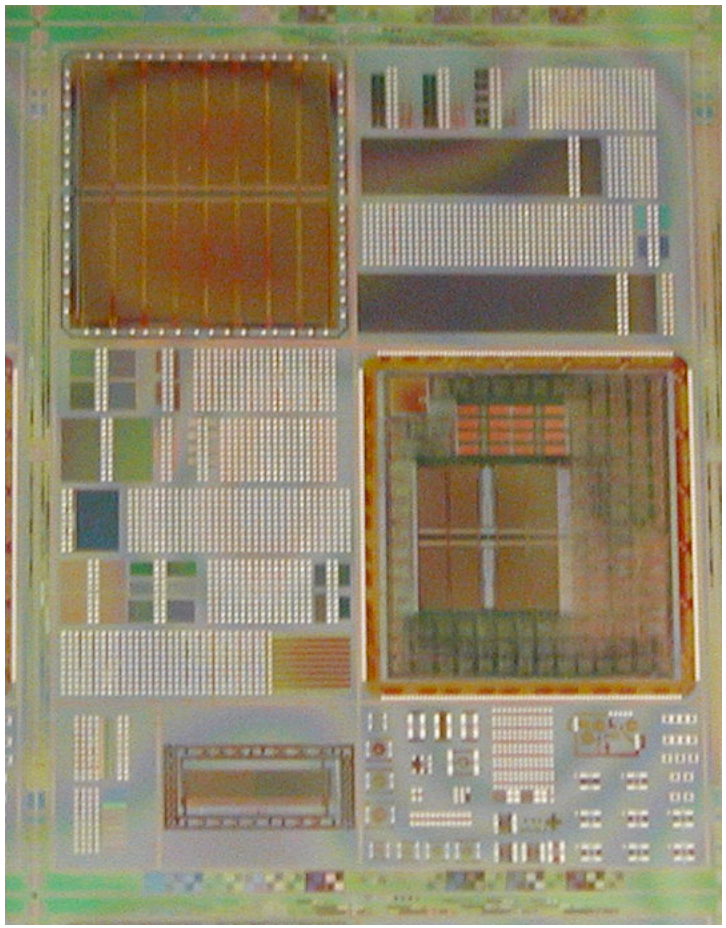


CMOS circuitry is processed in repeating patterns on Si wafers.

This wafer has about 30 identical die sites.

Each die site can have many different parts, or it can be dedicated to one particular product/function.

This one has hundreds of different pieces.



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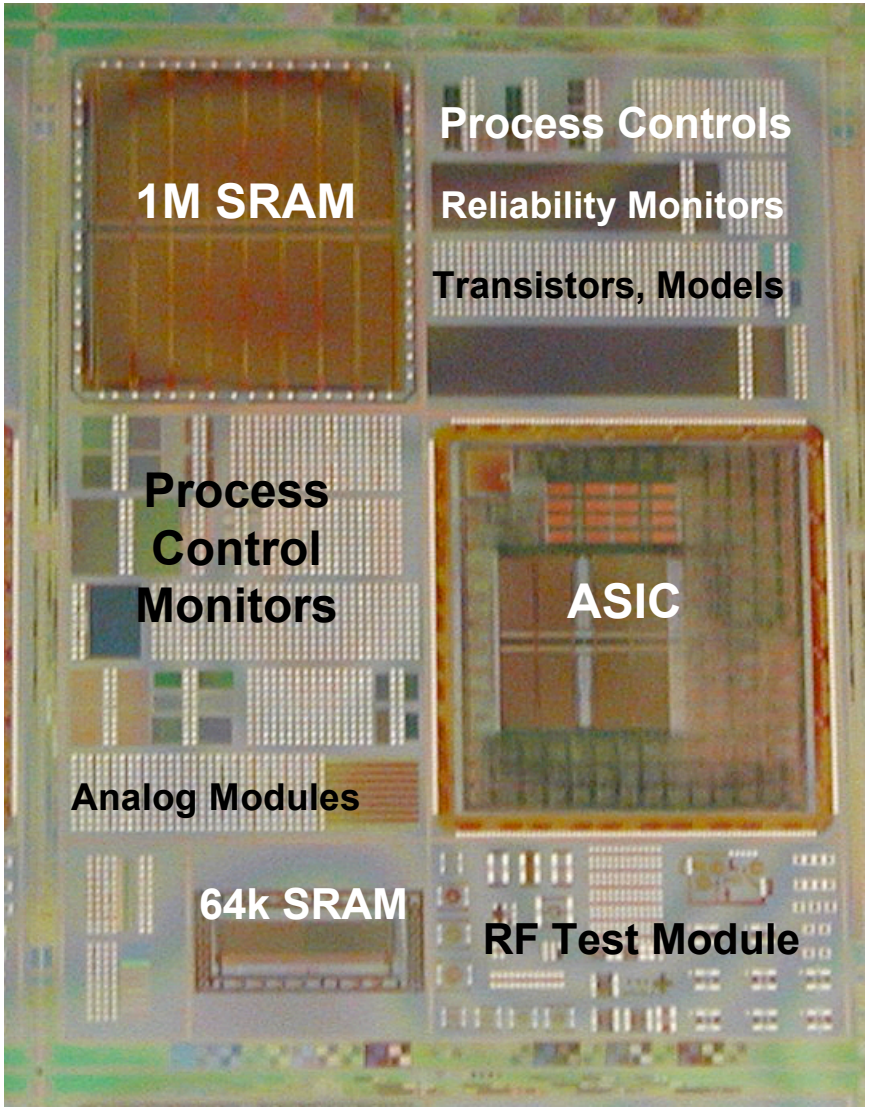

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Show a product die.
Label I/O, addressing, SRAM, etc.

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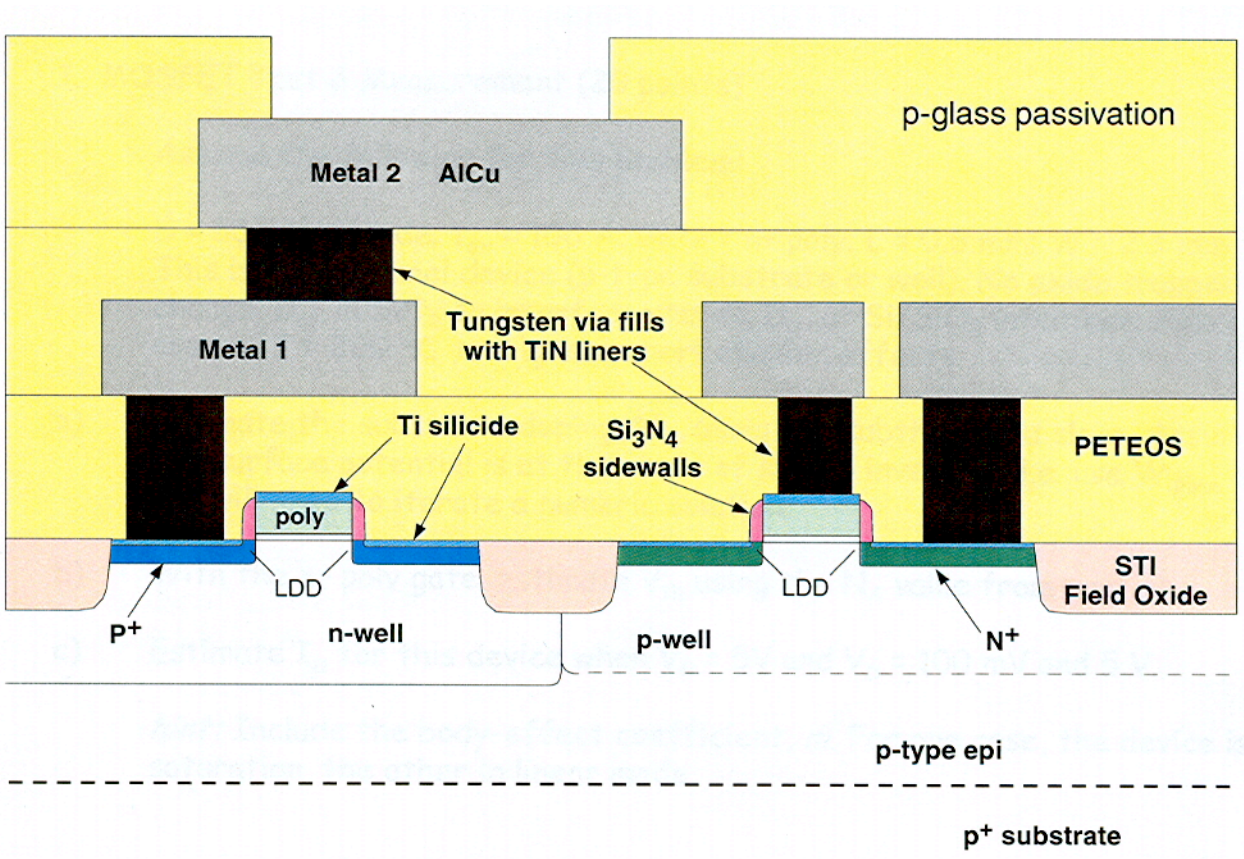
All of the circuitry is made up of the same building blocks



original wafer surface

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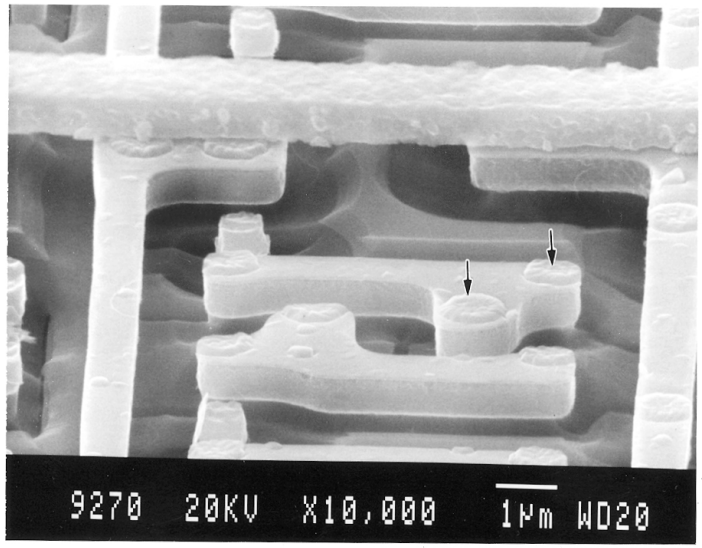
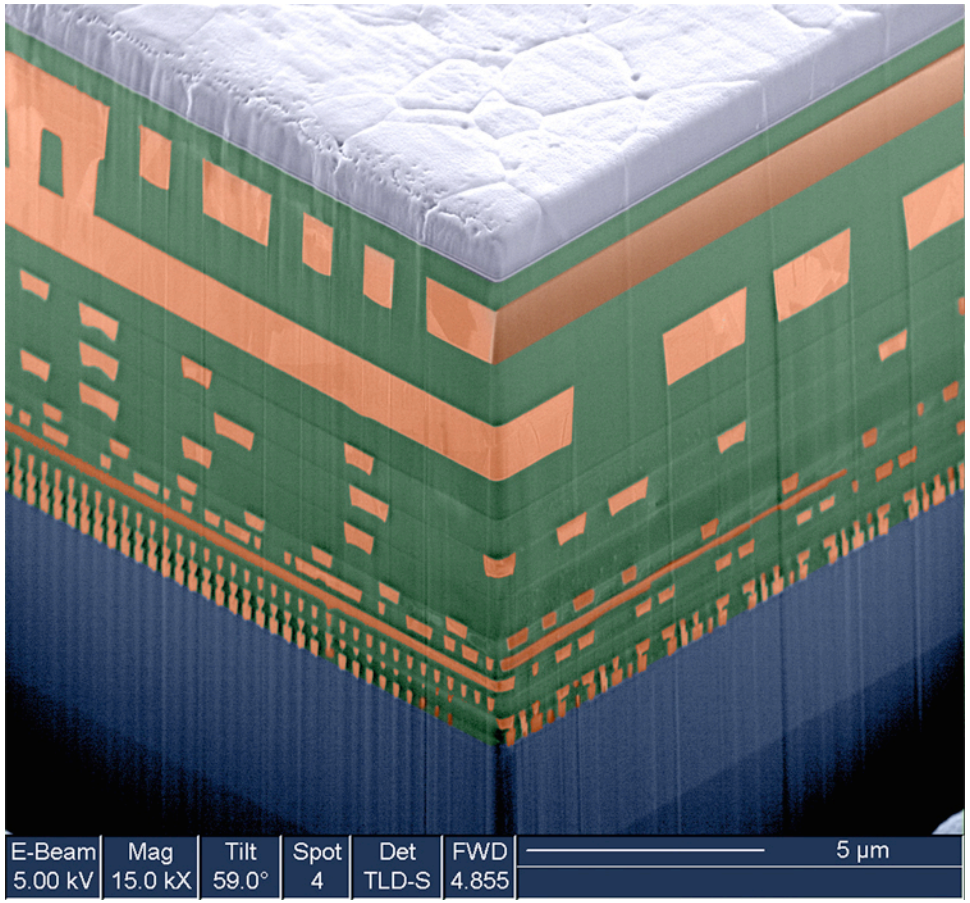
SEM x-section





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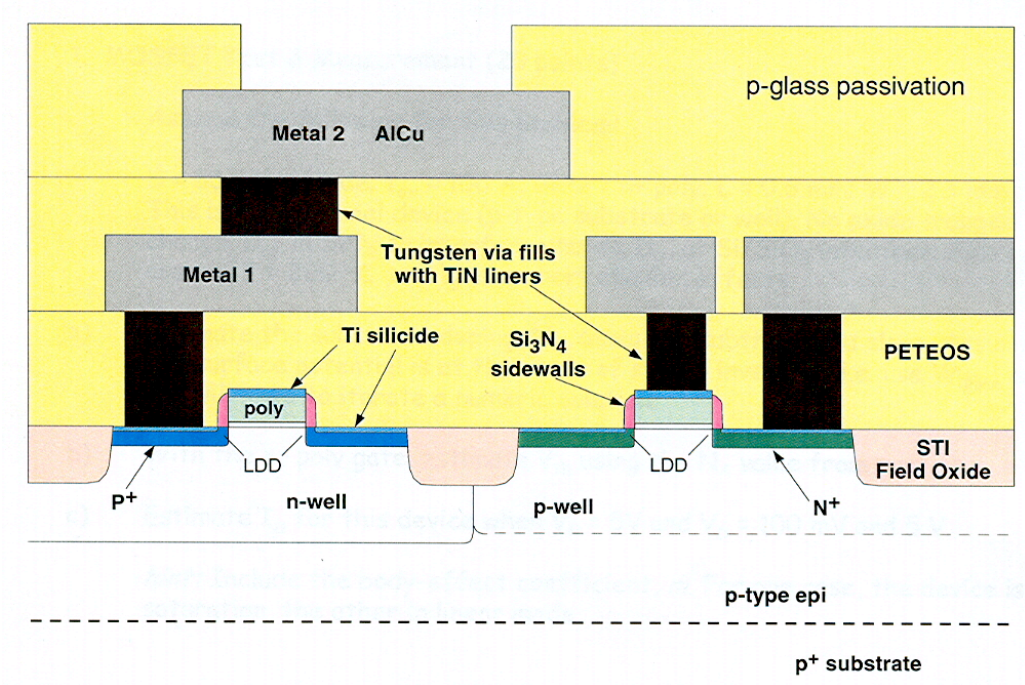
There are hundreds of steps and dozens of masks involved in making a CMOS integrated circuit.



Back End of Line (BEOL):
- Interlevel dielectric layers (SiO_2 based)
- Metallization (Al or Cu)
- Vias (usually filled with W or Cu)
- Final passivation

Front End of Line (FEOL):
- Ion Implants
- Lateral isolation (STI or LOCOS)
- Gate oxide growth
- Polysilicon
- Drain engineering (spacers, implants)
- Silicide formation

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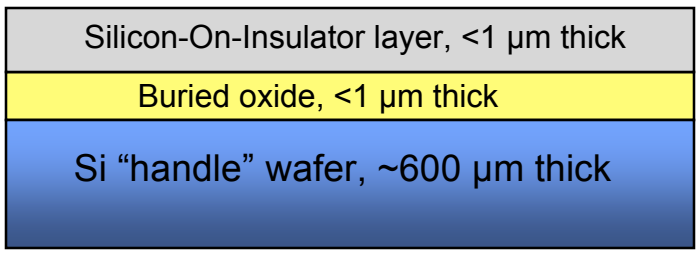
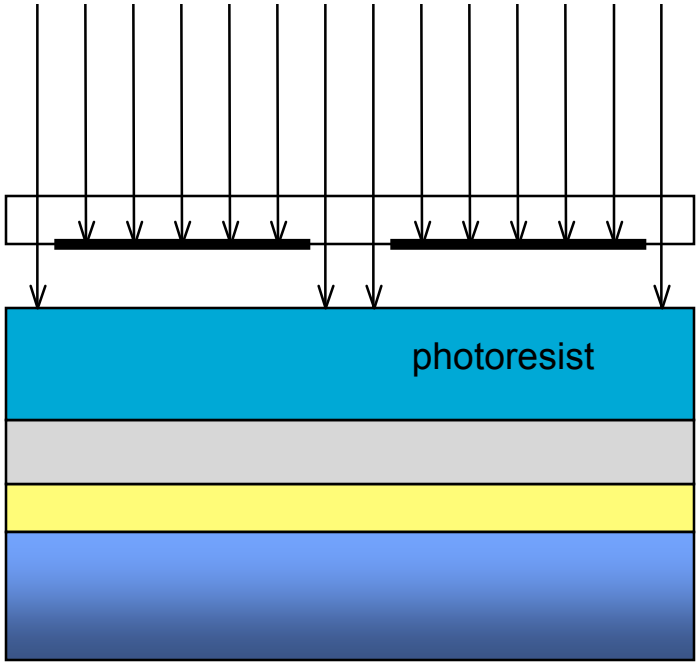
A Typical CMOS Fabrication Sequence



SOI starting wafer.
All of the microelectronics will be built in the top half micron of Si.
The interconnections will add another 5-20 microns.



Projection/reduction lithography is used to define a pattern in a layer of spun-on photoresist

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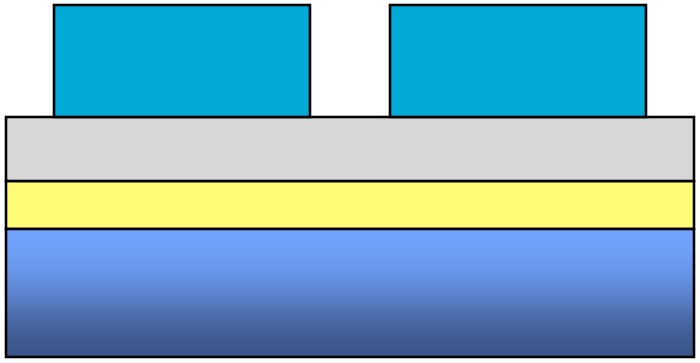
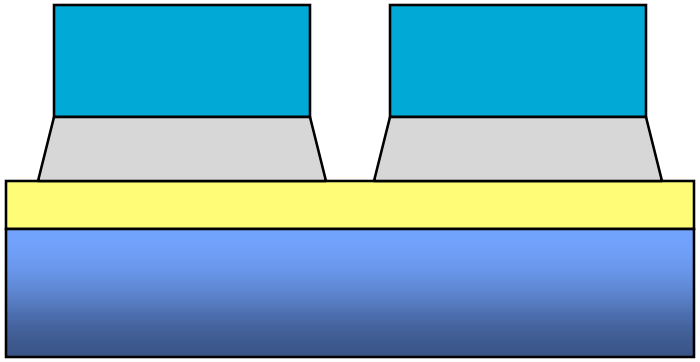
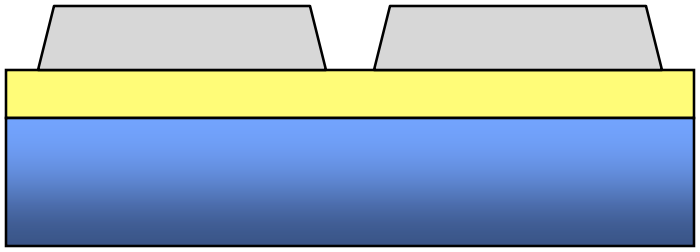


The photoresist is *developed*, leaving a patterned mask for the next step.



The PR is used to transfer the pattern into the SOI layer through reactive ion etching.



The PR is stripped, leaving isolated silicon islands where individual transistors will be built.

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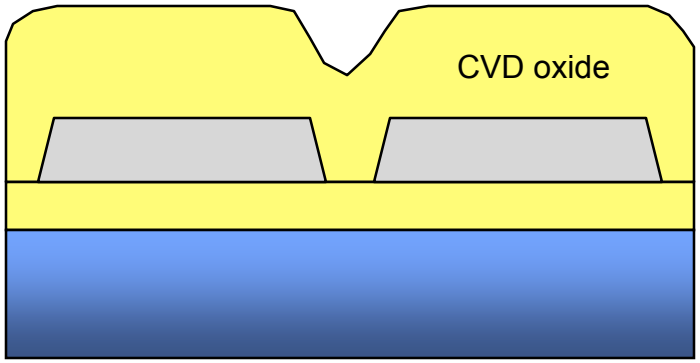
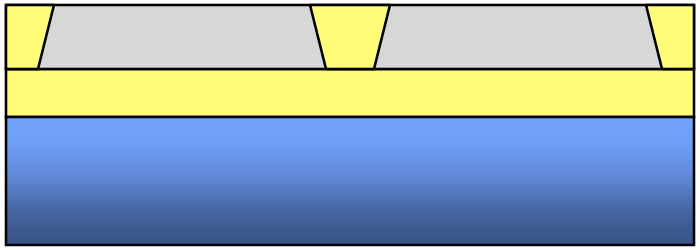
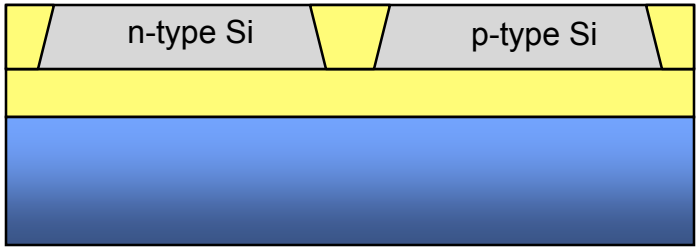


A *chemical vapor deposition* process creates a layer of oxide on the surface, also filling in the gaps between the Si islands.



Chemical-mechanical polishing is used to remove the oxide on top of the active Si islands, leaving the trenches filled.

This kind of construction is call *Shallow Trench Isolation* (STI).



Two separate photoresist masks are used in the ion implant processes to dope the islands either n-type (As^+ or P^+) or p-type (B^+).

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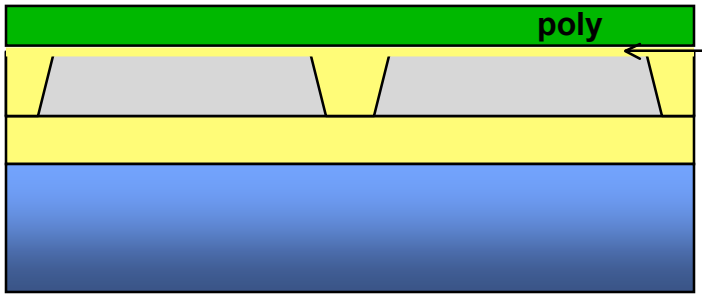


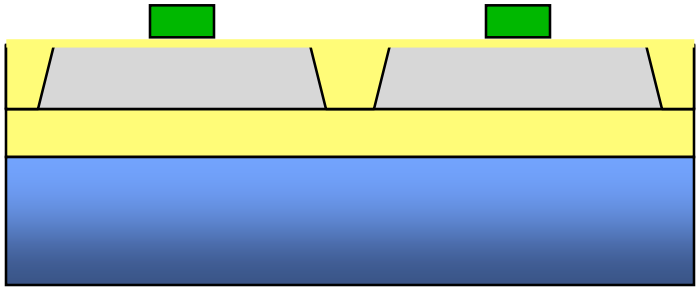
Grow a thin oxide on all exposed Si.

High-quality SiO_2

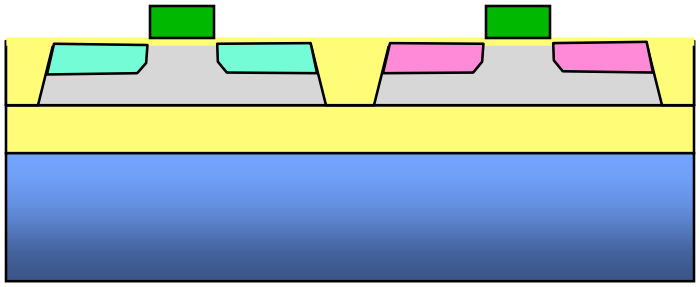
800-950°C, in O_2 or H_2O

Deposit polycrystalline Si everywhere.

Used for the FET control gate, and local interconnections.



Use photolithography and RIE to pattern the poly gates.



Use two separate photoresist masks (one for the n-channel FETS, another for the pFETs) and ion implantation to form the *lightly-doped drain* (LDD) regions.

The PR openings are fairly large. The polysilicon gates block the implants, creating *self-aligned transistor* structures.

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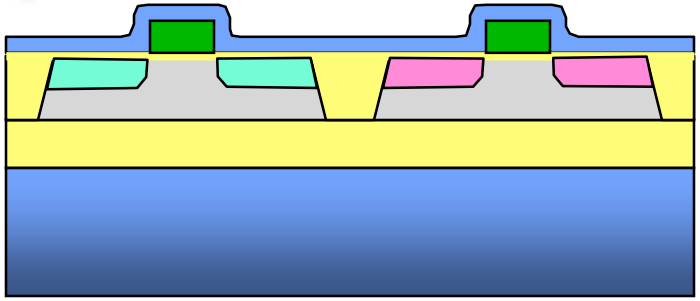
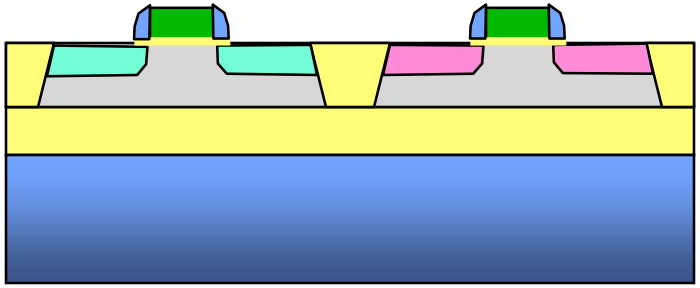
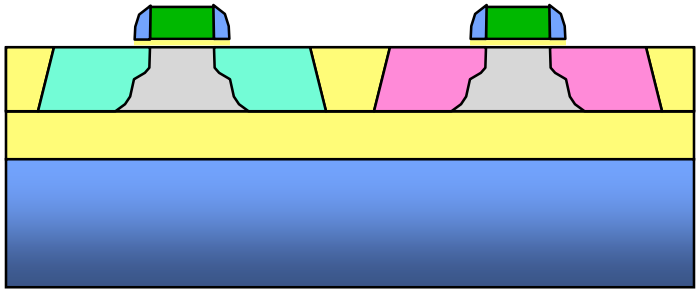


Deposit (CVD) silicon nitride over the entire surface.



Use *anisotropic* RIE to remove just enough nitride to clear the horizontal surfaces. Note that the vertical thickness of the nitride on the sidewalls of poly gates is much greater than on the horizontal surfaces (see the sketch above), so small fillets will remain.

These are called *sidewall spacers*, and play an important role in the device behavior.



Use two separate photoresist masks (one for the n-channel FETS, another for the pFETs) and ion implantation to form the deep drain and source regions of the transistors.

As with the LDDs on the previous page, the poly gates (and now the additional spacers) block the implants and create self-aligned transistor structures.

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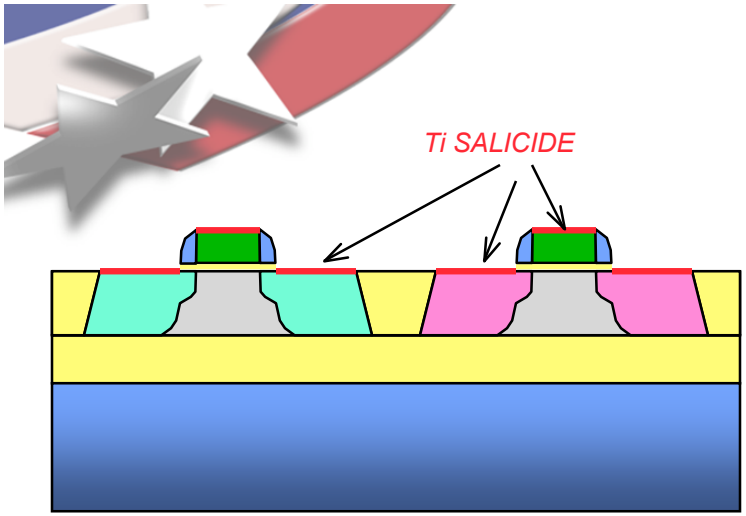
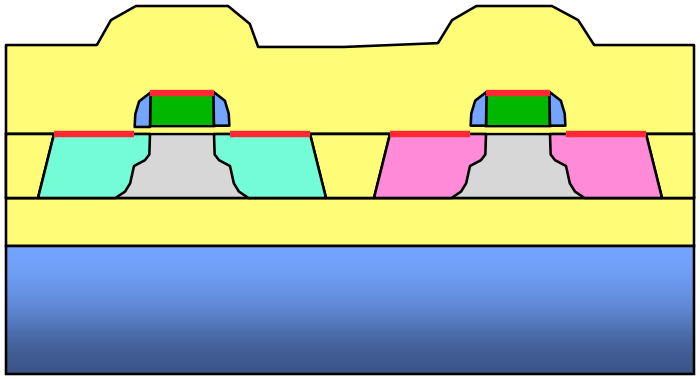
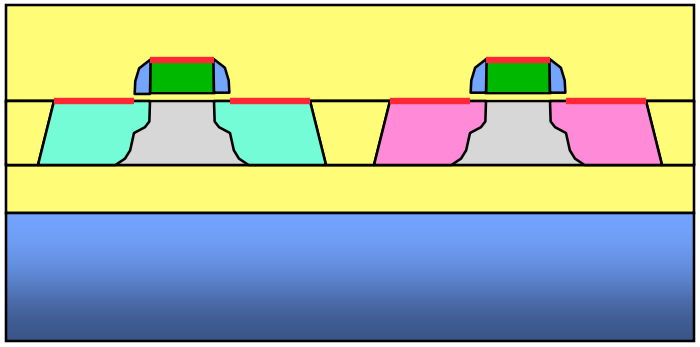


Deposit a thin layer of Ti everywhere, then anneal the wafers. Wherever the Ti is in contact with Si, $TiSi_2$ will form.

Using a selective chemical etchant, strip off the unreacted Ti. This leaves silicide only on Si surfaces.



Begin the BEOL processing:
Deposit thick (CVD) SiO_2



Use chem-mech polishing to planarize the surface.

This is important for photolithography and the facilitation of the damascene processes that follow.

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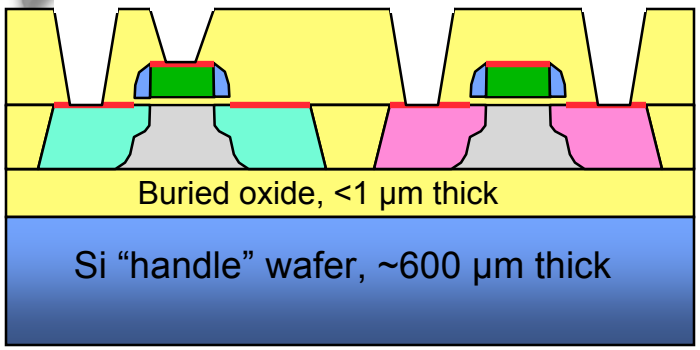
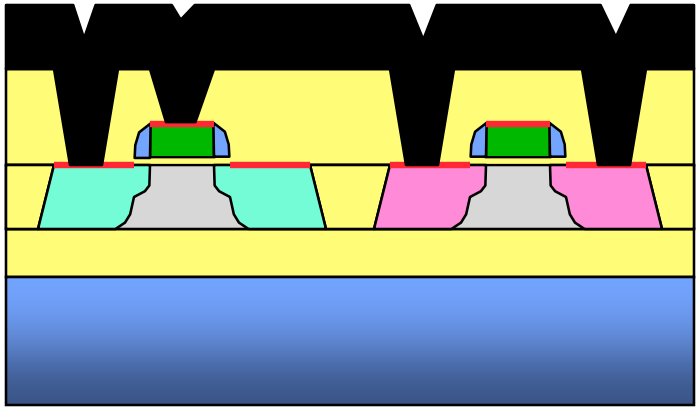
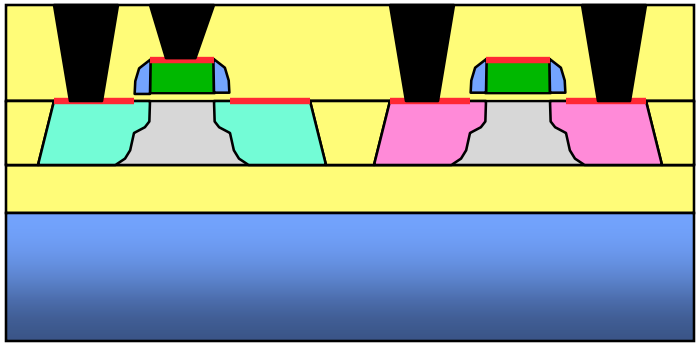


Use photolith and RIE to create openings in the interlevel dielectric.



Deposit (CVD) tungsten everywhere.



Use chem-mech polish to remove the tungsten from the planar horizontal surfaces, leaving the holes in the oxide filled with metal.

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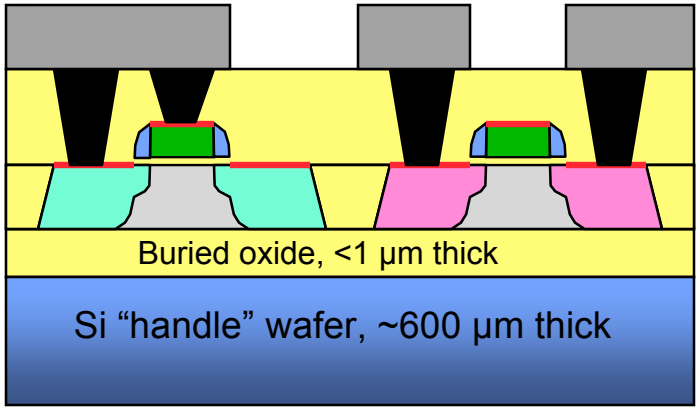
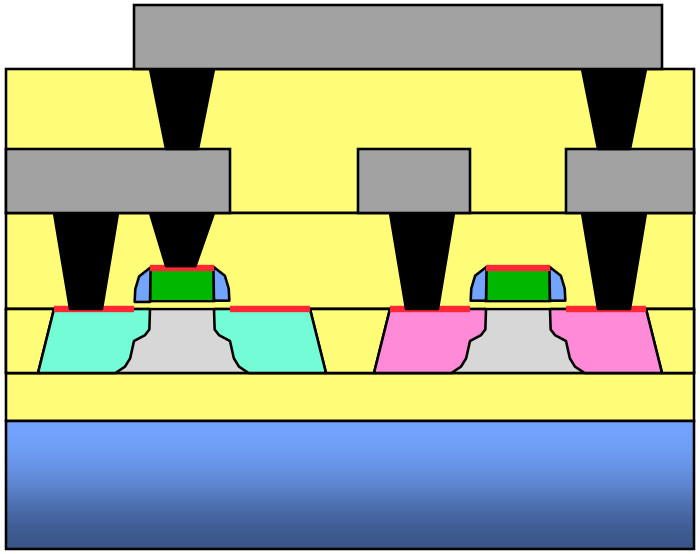


Deposit metal everywhere (usually Al-Cu alloy, sputter deposition).

Pattern with lithography and RIE.



Repeat as many times as needed:

- Deposit another interlevel dielectric.
- Planarize.
- Etch holes (vias).
- Deposit tungsten, polish.
- Deposit and pattern aluminum.

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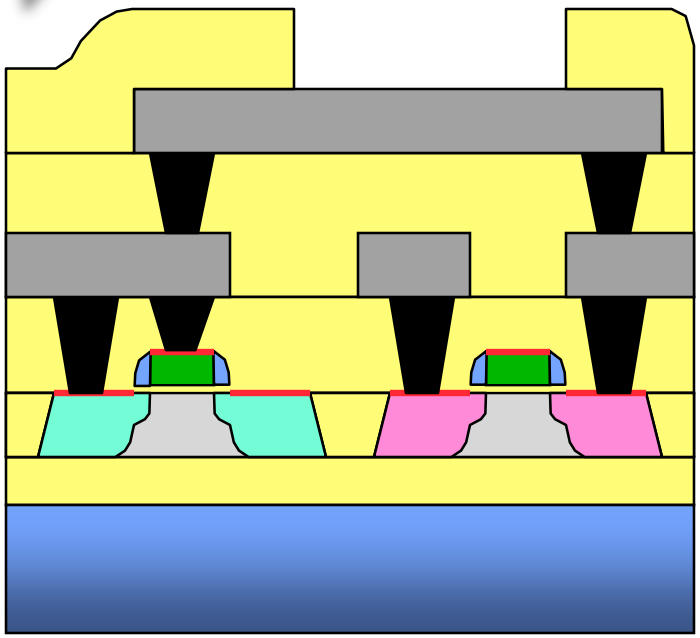

Finally, add a passivation/protection layer on the top.

Open up windows that allow access to the top level of metallization (for electrical probing and packaging).

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Current State of Manufacturing

150 to 300 mm wafers.
0.1 to 0.5 μm lateral dimensions.
Gate dielectrics down to ~ 2 nm.
    Oxides, nitrided oxides, high-K materials.
>10 levels of metallization, either Cu or Al.
Many millions of transistors per cm^2.
Single chip areas up to ~ 3x3 cm.

Both digital and analog functions (with integrated R/L/C components).
Speeds up to several GHz.
    Strained lattices, SiGe, etc.

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