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Microsystems-Enabled Scalable Array Synthetic Aperture Radar (MESASAR)

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Topics

- SAR Overview
- MESASAR Overview
- QDWS ASIC Design
- Other Trusted Foundry Design Examples
- New Initiatives
- Questions

SAR Overview

Synthetic Aperture Radar Efforts

- SAR is an imaging system that produces unique imaging capabilities for environmental monitoring, earth-resource mapping, and military systems
- Sandia National Laboratories is a recognized leader in the development of
  - Real-time, fine-resolution, high image quality SAR/IFSAR
  - Imaging/focusing algorithms
  - SAR hardware development
- System examples include
  - *LYNX radar (1999)*
    - Built for Predator UAV and incorporate GMTI capability
  - Operational, fielded IFSAR system for DTED mapping
    - Korea, Olympics, etc.
  - Other SAR variants: CCD, IFSAR, Video SAR, Vertical SAR
  - Precision guidance capability demonstrated with ITAG program (V-SAR w/ monopulse)

Synthetic Aperture Radar Efforts

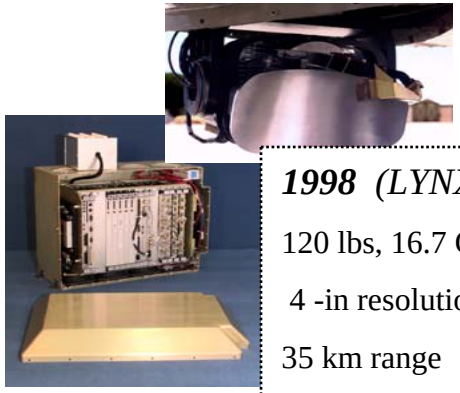
- SAR System Evolution
  - 1991 – Large system was 1st generation
  - 1998 – Lynx system was a significant reduction from 1st generation
  - 2005 – MiniSAR is the next generation (MCMs and FPGAs)
  - 2009 – MESASAR is the generation-after-next (microsystems/ASICS)

1991

500 lbs, 15 GHz

6-in resolution

16 km range



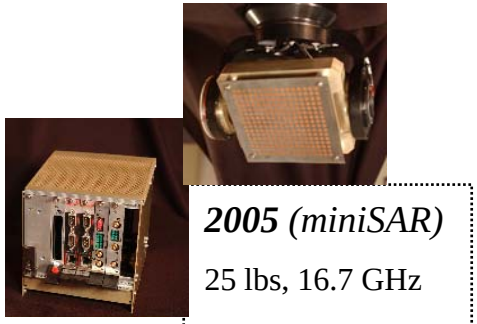
1998 *(LYNX)*

120 lbs, 16.7 GHz

4 -in resolution

35 km range

CCD & GMTI



2005 *(miniSAR)*

25 lbs, 16.7 GHz

4-in resolution

15 km range

2009 *(MESASAR)*

multi-phase center

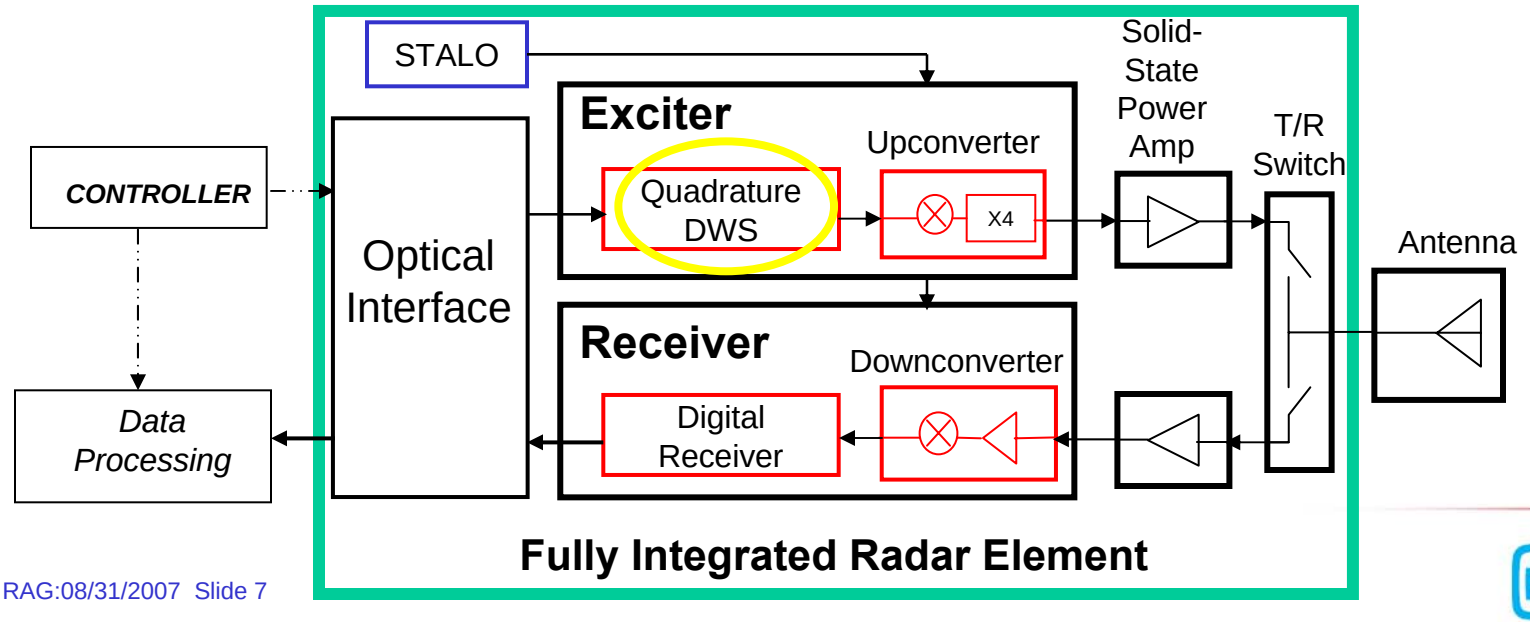
agile/scalable

MESASAR Overview

MESASAR: Compelling Technology and System Innovation

- **Technology**: Fully Integrated Radar Element (FIRE module)
  - Integration Level: Revolutionary leap in integrated RF/digital technology for Radar
  - Functionality: Incorporate advanced radar waveform generation, power amplification, digital receiver technology, and bandwidth compression and filtering in small, integrated module
- **System**: FIRE facilitates multiple, unprecedented Radar system capabilities
  - Size and Cost: **Extreme miniaturization** and affordability (Lynx/10)
  - Performance: Broad bandwidth, high fidelity signal generation and data acquisition
  - Independent Phase Centers:
    - Combine in large conformal ESAs, with hyper concurrent (multiple, simultaneous beams/modes).
    - Single Fiber optical/digital I/O.

FIRE Module Simplified Block Diagram



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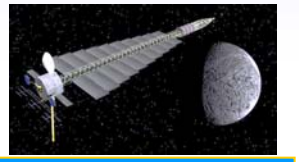
Demonstration: Extreme Miniaturization

Radar / Parameter	*Lynx*	*miniSAR*	*MESASAR$_1$* *(4 FIRE modules, ext. SSPAs option, RF MEMs-based ESA)*	*MESASAR$_2$* *(18 x 9 =162 FIRE modules; sub-array-based ESA)*
weight	W	W /5	< W /10	< W /2
total volume	V	V/6	< V/20	V/7
range	R	R/3 (sho t)	R (medium)	> **2R** (long)
cost	X	X/4	< X/10	1.5 X
conformal structure	No	No	Yes	Y s
# phase centers	1	1	4	162
IFSAR	No	No	Yes	es
GMTI	Exoclutter	Exoclutter	Exo/Endoclutter	Exo/Endoclutter
gimbal or ESA	3 axis gimbal	2 axis gimba	ESA	ESA
hyper-concurrency, adaptive nulling, etc.	No	No	No	***Yes***

Microsystems-Enabled Scalable Array SAR

Aerial Intelligence
Fine resolution SAR
Moving-target tracking
3-D mapping

Conventional Weapons
Affordable seekers
Communications



Space Systems
Space-based radar
Planetary-probe SAR

Asset Identification
Radar-responsive tags
Autonomous tags

Enables Systems

antenna (sometimes integrated)

Miniature Radar Module

computer

images

Miniature Radar Module

2 Chip Exciter
3 Chip Receiver
High-Density Interconnects
Solid State RF Power

RF MEMs | Photonics | Mixed Signal (SiGe) | Solid-State Power (GaN)

Miniature Packaging & Integration

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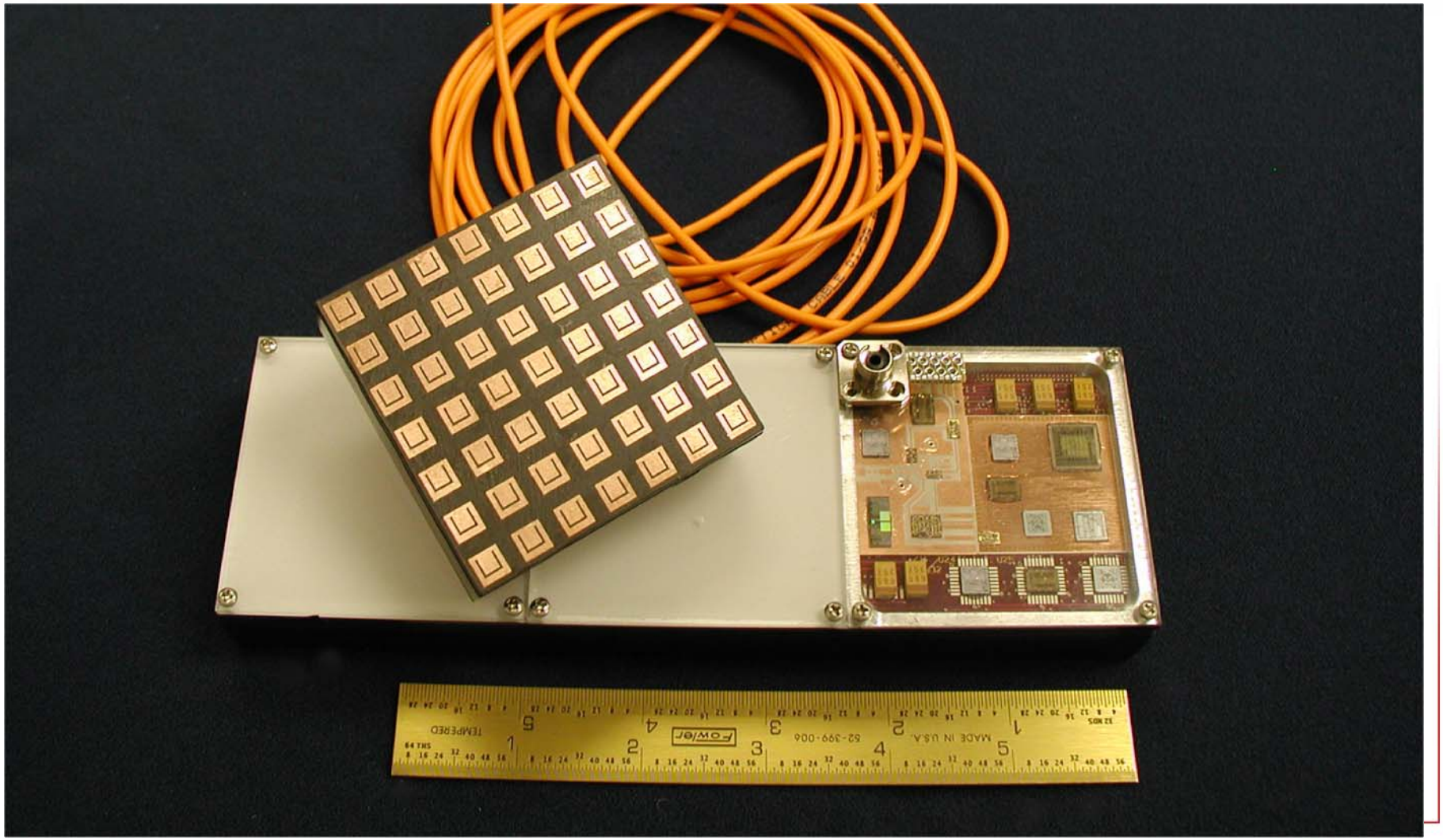
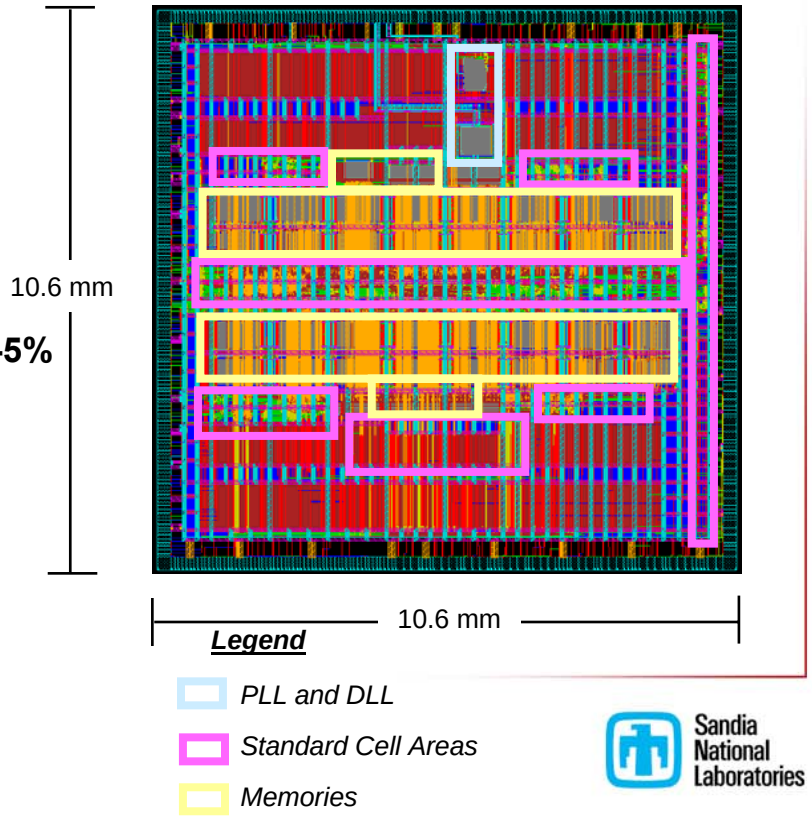
Fully Integrated Radar Element Module mockups



QDWS ASIC Design

QDWS ASIC Overview

- **Function**
  - The QDWS ASIC is a waveform generator that uses direct digital synthesis techniques to generate a linear FM chirp for use in a next generation synthetic aperture radar (SAR) system (MESASAR)
- **Goals**
  - To design an ASIC that will be a drop-in replacement for the Quadrature Direct Digital Synthesizer (QDDS) FPGA in the existing Mini-SAR system as well as integrate the two error correction SRAMs on chip
    - Reduce power and area
- **Targeted Technology**
  - Trusted Foundry IBM 130 nm CMOS8RF
- **Operating Conditions**
  - Temperature: …. -40 to 85◦C
  - Power Supply: ….Core 1.5 V +/-5% , I/O 2.5V +/-5%
  - Frequency: ……. 66MHz, 150 MHz, 300 MHz
- **Gate Count**
  - 3,991,468 2-input NAND Equivalent Gates
- **I/O Count: 478**
  - 263 signal I/O
  - 215 power/ground



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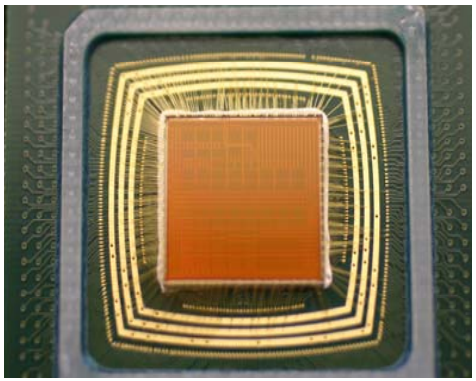
QDWS ASIC Status

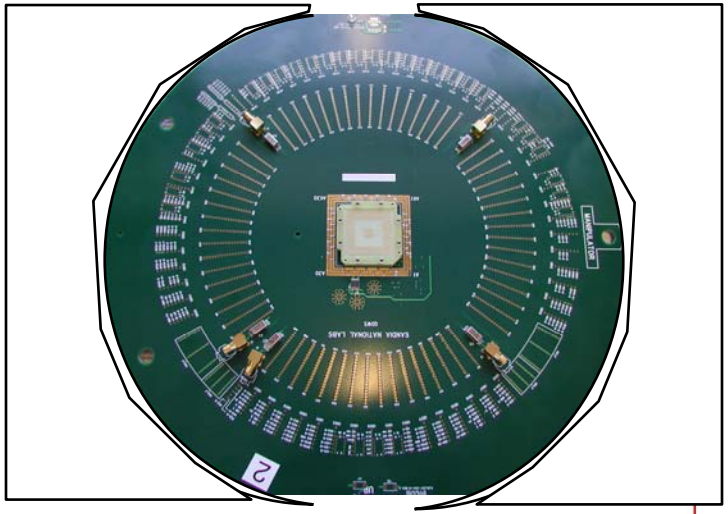
- Successfully translated FPGA to ASIC design
  - Reduction in both area and power
- Design tape-out in May 2006
- Silicon fabrication complete in October 2006
- Testing complete with first silicon functional success!
- Fabricated via Trusted Foundry run at a cost savings of greater than $500K, initiated by Gerard Titi (now at BAE) and continuing with Mark McClure, DARPA/IXO.



Packaged QDWS ASIC

QDWS ASIC Testing Results

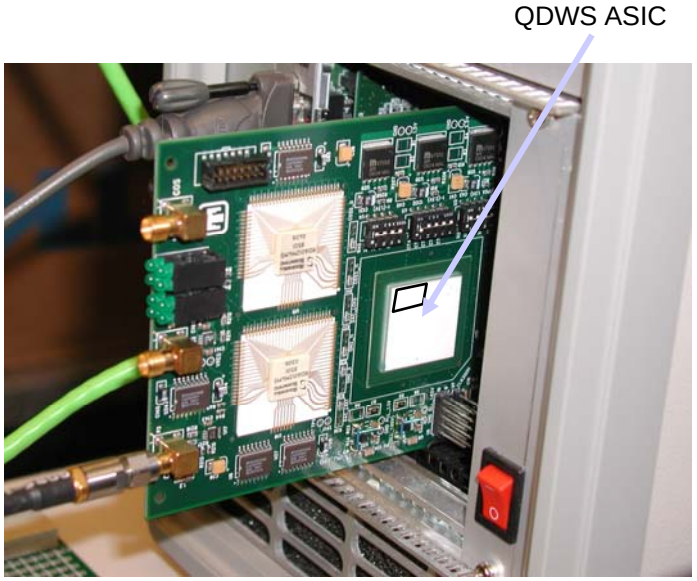
- **Automatic Test Equipment (ATE) Tests Performed**
  - **Analog Tests ..... Passed**
    - **Phase Lock Loop**
    - **Delay Lock Loop**
      - **Designed for a delay of 103 ps result was delay of 206 ps**
      - **Deemed acceptable by system designers**
  - **Functional Tests (68 total) ..... Passed**
    - **Output dithering**
    - **Chirp waveform variations**
    - **Error correction**
  - **Manufacturing Tests ..... Passed**
    - **Memory Built In Self Test (BIST)**
  - **Temperature Variation ..... Passed**
    - **Cold Testing: Functional tests performed at -55 °C**
    - **Hot Testing: Functional tests performed at 80 °C**



QDWS ATE Load Board

System Level QDWS Testing

- **System Level Integration**
  - **The QDWS ASIC has been incorporated into a Mini-SAR system by replacing the QDDS FPGA on the exciter board**
  - **Functional testing in progress**
  - **Power analysis pending**



Mini-SAR Test Environment

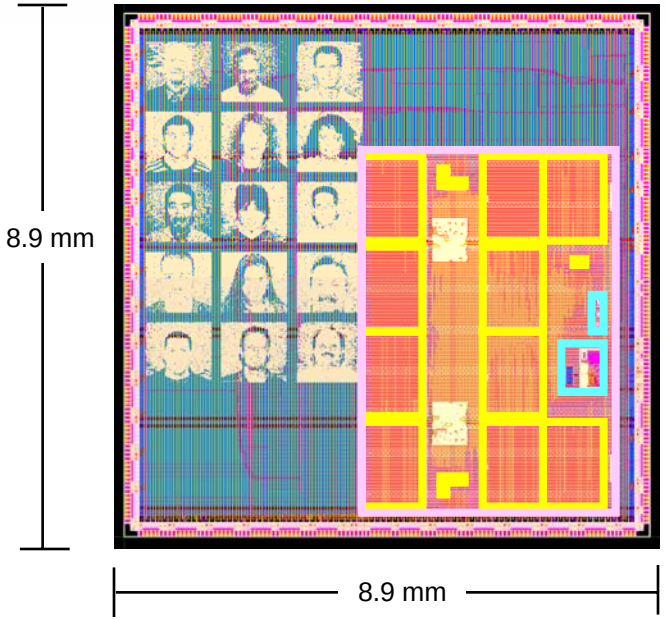
Other Trusted Foundry Designs

Trusted Foundry Fabrication Experience

- Mature working relationship with IBM Trusted Foundry
  - Fabricated several integrated circuits via Trusted Access Program Office (TAPO) at several process nodes (180nm, 130nm, and 90nm CMOS; 250nm and 180nm SiGe)
  - Majority of experience in CMOS8RF technology
    - 130nm, bulk CMOS technology
    - Mixed-signal process, 1.2/1.5v core, 1.8v/2.5v/3.3v tolerant I/O
- Access and working experience with newly approved Trusted Foundries
  - Fabricated devices National Semiconductor CMOS8 technology
    - 250nm bulk CMOS technology
    - Mixed-signal process, 2.5v core, 2.5/3.3v I/O
  - Fabricated devices with Honeywell
    - Legacy devices in 350nm technology node
    - In proposal stage for a potential 150nm design

Trusted Foundry Design Example

- **Application**: NSA security certified microcontroller design
- **Description**: The KDP-III is a secure microcontroller design
- **Technology**: IBM 130nm CMOS8RF
- **Design Methodology:** Custom mixed-signal IC design using standard cells, custom analog, IBM IP, and Artisan compiled memories
- **Design Statistics:** 4.6M NAND Gate Equivalents
  - ~ 2.7M memory
  - ~ 1.9M core & IO
- **I/O Summary**: 480 pads
  - 268 signal I/O
  - 210 power/ground
  - 2 break pads



Operating Frequency: 25-100MHz

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Current Initiatives

Current Initiatives

- Custom ASICs
  - KDP-IV ASIC
    - Custom ASIC for SAASM GPS units funded by DOD
    - NSA security certified microcontroller design
    - Targeting IBM 90nm CMOS9LP technology
  - Focal Plane Array Grand Challenge
    - Joint development with Satellite
    - Targeting a 2K x 2K Pixel Array, extendable to 8K x 8K
    - Developing 3-D silicon stacking capability
    - Targeting IBM 130nm CMOS8RF technology
  - UTSOI ASIC
    - Synthesis, physical design, and fabrication of Navy SPAWAR microcontroller data acquisition system for Ultra-thin GPS application
    - Targeting CMOS7 0.35um process
- Sandia technology Analog IP Development
  - Developing several analog modules for use in future systems
- Sandia technology ViArray Structured ASIC Development
  - Developing a quick-turn solution for use in future systems

Questions?