Building More Powerful Less Expensive Supercomputers Using Processing-In-Memory

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LDRD
LABORATORY DIRECTED RESEARCH & DEVELOPMENT

Sandia National Laboratories

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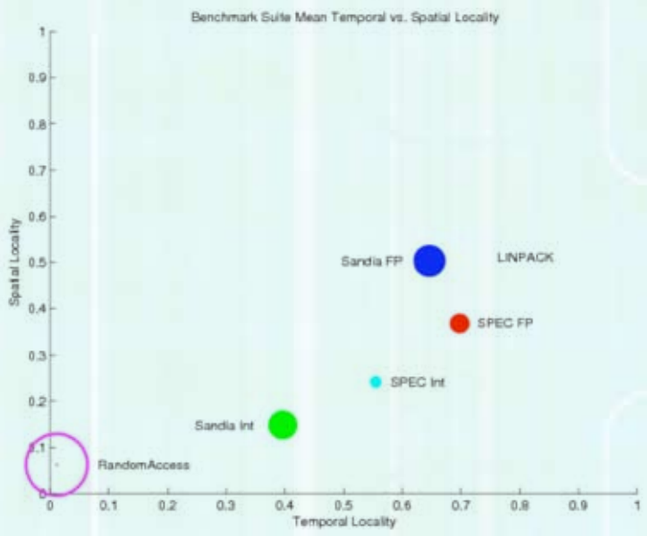
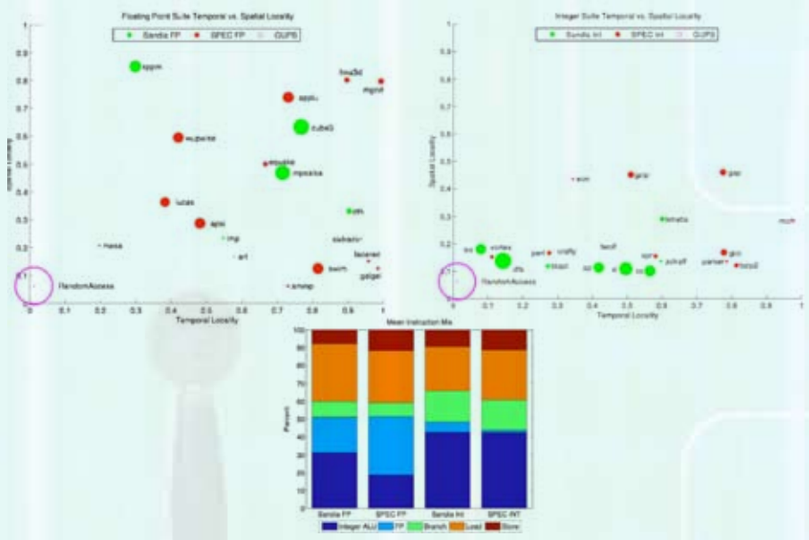
X-caliber ARCHITECTURE

The Problem

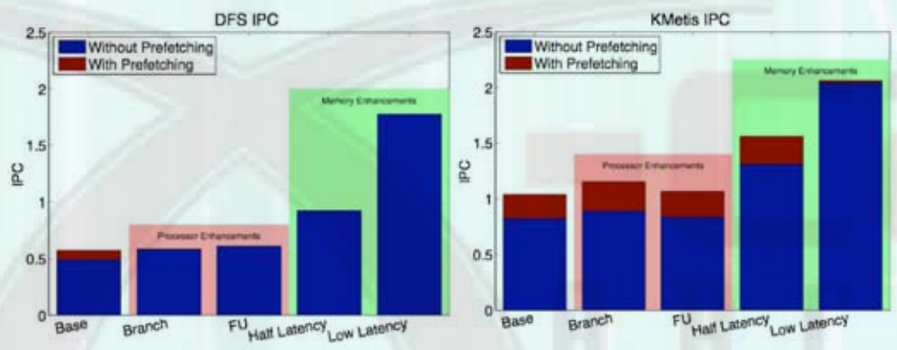


Applications (especially supercomputer applications) are dominated by memory performance

Individual Applications Compared to SPEC

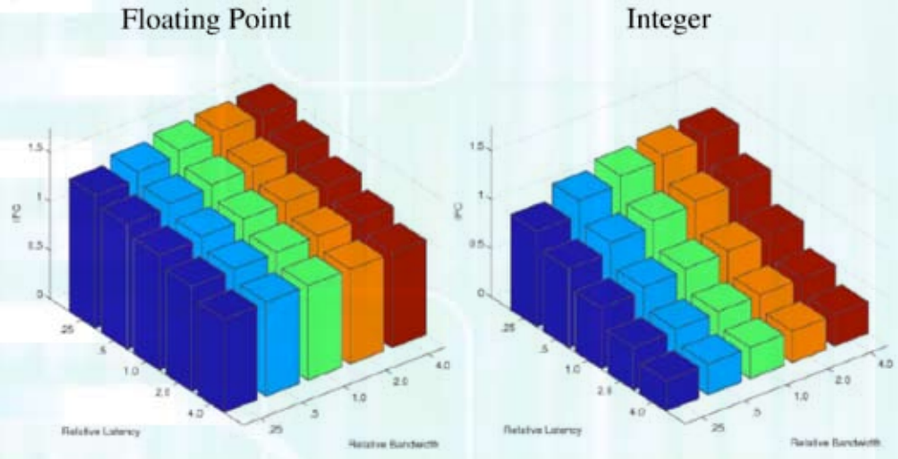


Finding the Bottleneck: Computation, Branches, or Memory



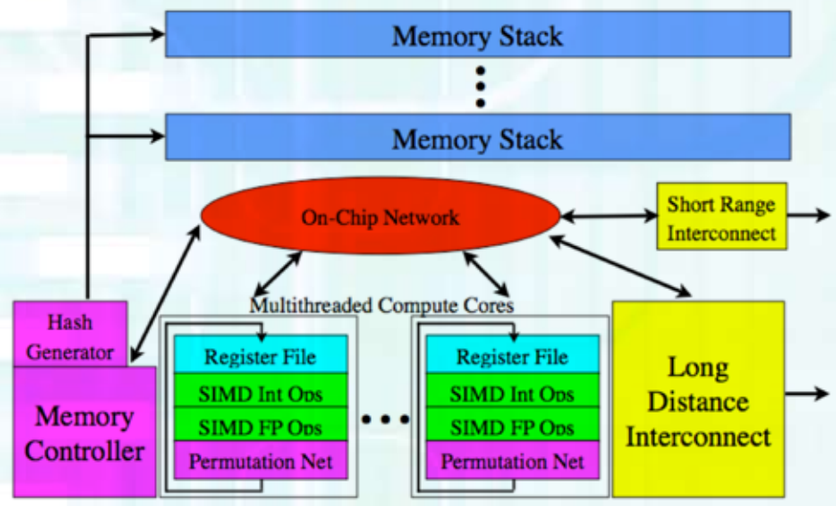
Even perfect branch prediction and infinite functional units would be less valuable than improving memory latency!

Latency/Bandwidth Sensitivity



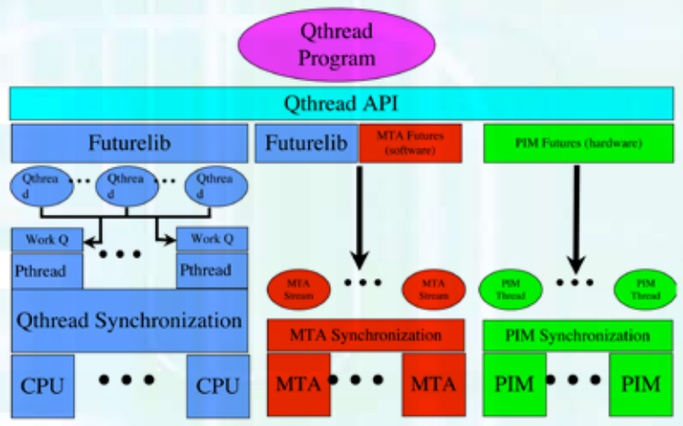
Emerging applications nearly 3x more sensitive to Latency and Bandwidth than traditional codes!

Approach: the X-Caliber Architecture



Combines high-speed logic and dense DRAM in a 3D stack

Experimental Results: DFS



- **Up to 30% better than conventional with free coherency**
- **2x-10x+ improvement over conventional!**
- **4x+ better than an MTA running at 2 GHz**

Significance

- **This project has the potential to create a new generation of supercomputers that are higher performance, lower power, and less expensive**
- **An outgrowth of this effort is joint work with a major memory vendor to define a new commodity memory part that is higher bandwidth, allows more outstanding memory references, and enables inexpensive 3D integration**
- **This work has quantified the impact of memory performance on a set of real Sandia applications and introduced a methodology for doing so with any other set of applications**
- **PIM simulation and Qthread runtime library developed**
- **14 Applications Studied, 1 Journal Paper, and 3 Conference Papers in FY07**

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