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In-Situ Solar Photovoltaic I-V Characterization Notions

Dave Campbell, SNL Organization 1767

Abstract

This paper scopes concepts for implementing in-situ photovoltaic I-V characterization. The discussion takes the perspective of providing guidance for independent implementation by perhaps a university undergraduate class as a research and development learning exercise. As such, it identifies details of each element needed without explicitly defining a specific implementation, left as an exercise. It notes too, a few trades that merit further examination particularly with respect to cost and power.

Problem Set

The notional application concept proposes that in-situ I-V characterization offers opportunity for improved operational performance and automated maintenance requests applied to power-plant-scale photovoltaic installations.

Approaches based on commercial-off-the-shelf (COTS) data acquisition systems (i.e. Compact Rio and LabView) and numerous specialized hardware sensors (i.e. Current Viewing Resistors with individual Programmable Gain Amplifier modules) offer quick prototyping and flexible reconfiguration. However, this becomes very expensive very quickly, easily topping $10K per 5-10KW array configuration with many installations per plant.

The baseline concept proposes the use of a custom dedicated data acquisition board used in conjunction with any of a number of readily available inexpensive open-source single-board computers. This requires some up front development cost for lower fielded unit costs. Such an approach can tailor the data acquisition and optimize power losses and fielded cost.

Panel Constraints

For purposes of discussion this work assumes a baseline branch capacity of 600V open circuit voltage and 15A short circuit current, which equates to an approximate maximum power point output of approximately 7KW. Eventual application goals would push this to 1000V and 25A, equivalent to 20KW. Some trades hinge on this operating constraint as discussed.

Configuration Assumption

Typically, multiple solar panel arrays, referred to as stings, route to an electrical combiner box, which interconnects them and routes the aggregate total power to a DC/AC grid-tie inverter, which outputs AC power into the consumer grid. This work assumes the use of combiner boxes and availability of space within the box for locating the necessary electronics.

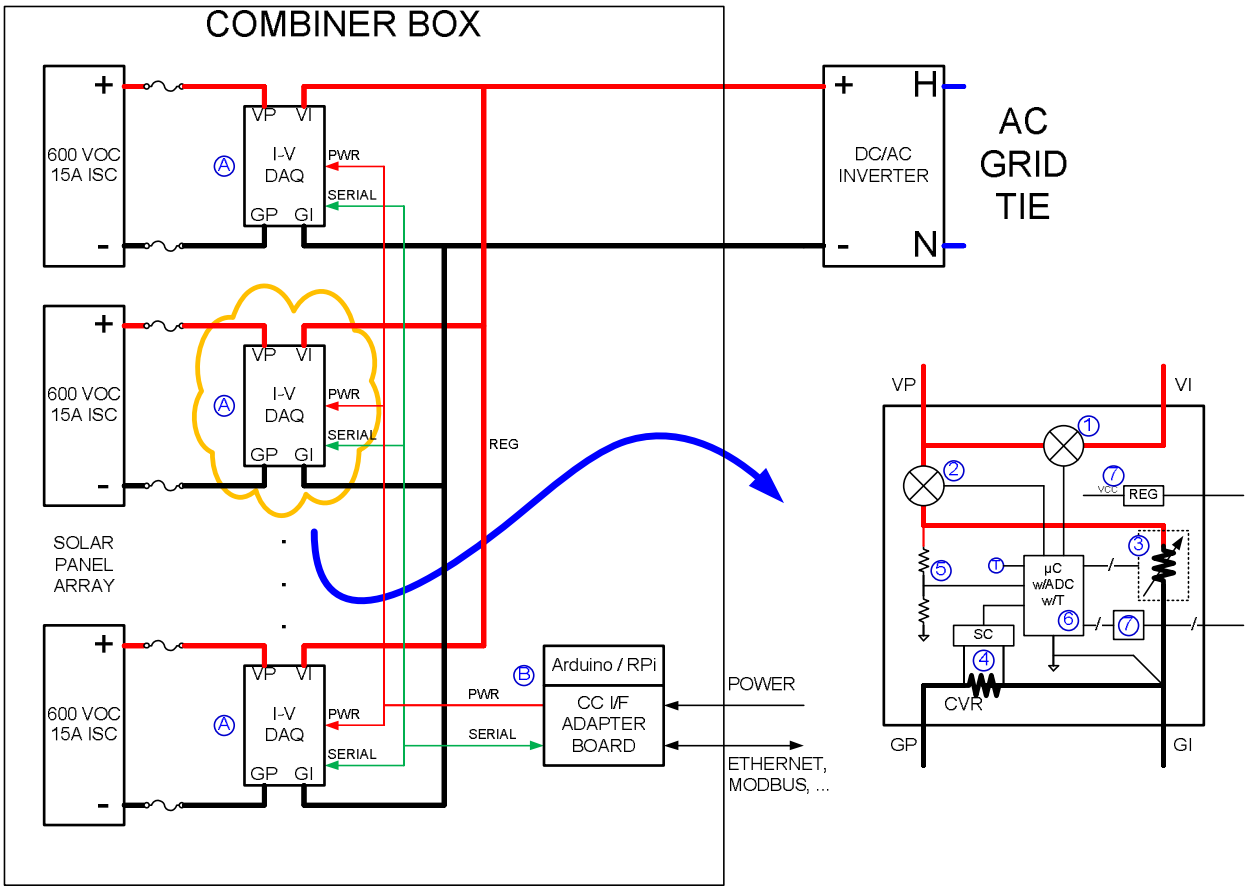

Figure 1: In-situ Photovoltaic Characterization Concept

Concept and Problem Elements

Figure 1 outlines the high-level implementation concept. This concept proposes inserting an I-V data acquisition (I-V DAQ) board into the path of each branch or string of the combiner box. All of these boards in turn talk to a computation and communications interface (CC I/F), which provides automatic characterization on demand and relay of information to plant operations. The insert of the lower right corner of Figure 1 provides a simplified schematic of the DAQ functions. The boards and their functions include:

A. I-V Data Acquisition Board (I-V DAQ)
   1) String Disconnect Switch
   2) String Monitoring Connect Switch
   3) Programmable Load
   4) Current Measurement
   5) Voltage Measurement
   6) Controller and Data Acquisition (DAQ)
   7) Power & Communications
   8) Calibration (software, not shown in figure)

B. Computation and Communications Interface (CC I/F)
    1) Data Collection
    2) Computations
    3) Central Communications

The following sections outline issues and solution space for each of these functions. With knowledge of these elements discussion concludes with some trades to consider in the overall implementation.

I-V Data Acquisition

String Disconnect Switch

The disconnect switch functions to isolate the solar panel string from the inverter for the purpose of performing I-V measurements. In operation it is normally ON and in the power delivery path, therefore, series losses as well as drive efficiency become critically important.

The electronic disconnect switch represents a simple concept that becomes surprisingly difficult to implement at reasonable cost. The disconnect switch requirements, each a specific challenge, include:

- LONG SERVICE LIFE.
- HIGH-VOLTAGE, HIGH-POWER SWITCHING.
- LOW ON RESISTANCE (LOW LOSS).
- BIDIRECTION HOLDOFF.

Long service life suggests semiconductor switching solutions. Arcing associated with relay based DC current switching complicates solutions and compromises performance and reliability over time. Oil-immersed relays may be applicable at greater power levels and may merit further cost trade study, but this discussion discards them in favor of semiconductor switching.

The high-voltage and high-power, 10-20A at 600V to 1000V, constraints place a significant cost burden on the solution. The low loss further compounds this. A 0.1% loss at 500V requires a maximum of 33 milliohm series resistance. (Note: in MOS technology, ON resistance trades inversely to operating voltage.) A quick product search shows devices in this realm cost $20-30 each and would likely require multiple parallel devices to simultaneously achieve both the voltage standoff and low on resistance, especially with scaling.

Furthermore, the switch must accommodate bidirectional standoff. When disconnected the string open circuit voltage exceeds the inverter input voltage; when loaded for short circuit current characterization the inverter voltage exceeds the panel voltage as it approaches zero. This requires a bidirectional switch, meaning two devices in series, which doubles the number of parallel devices.

High-voltage and power also drive the actual switching implementation and requires isolated high-side power, isolated switching control, and fast switching.

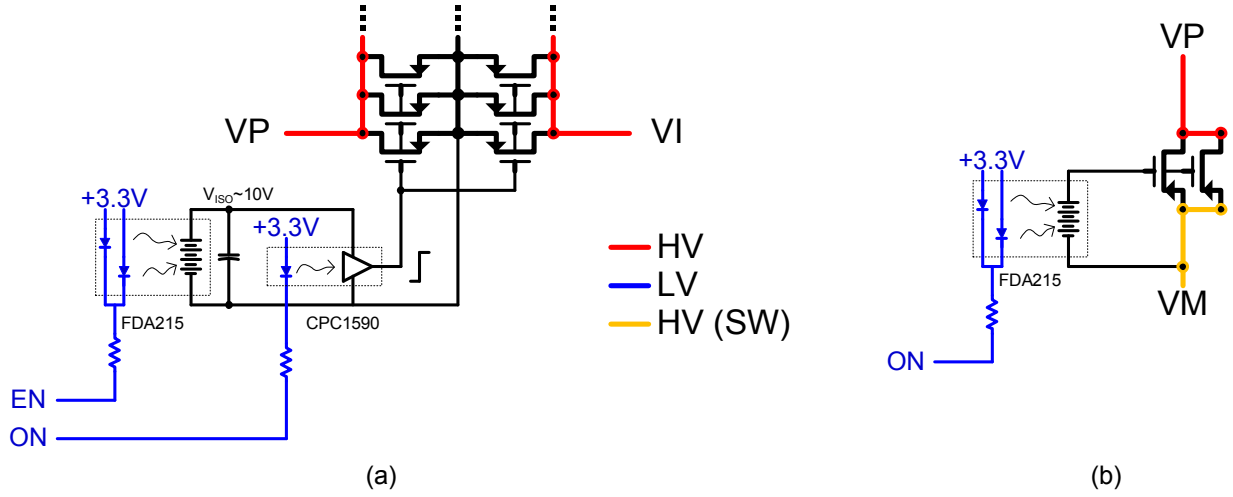

Figure 2: (a) String Disconnect Switch and (b) String Monitoring Connect Switch

(a) gives a conceptual representation of the disconnect switch issues. It configures multiple pairs of back to back MOSFETs as the switch. The circuit demonstrates the use of a Claire FDS215 photovoltaic optocoupler to generate an isolated supply (~10V @ 2-3uA) referenced to the shared source connection of the MOSFETs. This charges a capacitor to store the necessary switching charge. A simple simulation shows device power on the order of 500W in the switches during state transition making switching speed on the order of microseconds an important consideration. A second CPC1590 optocoupler drives the gate quickly to minimize this power dissipation during switching. The transistors do not require significant heat sinking for the transient dissipation. The use of optocouplers allows control from standard 3.3V logic levels.

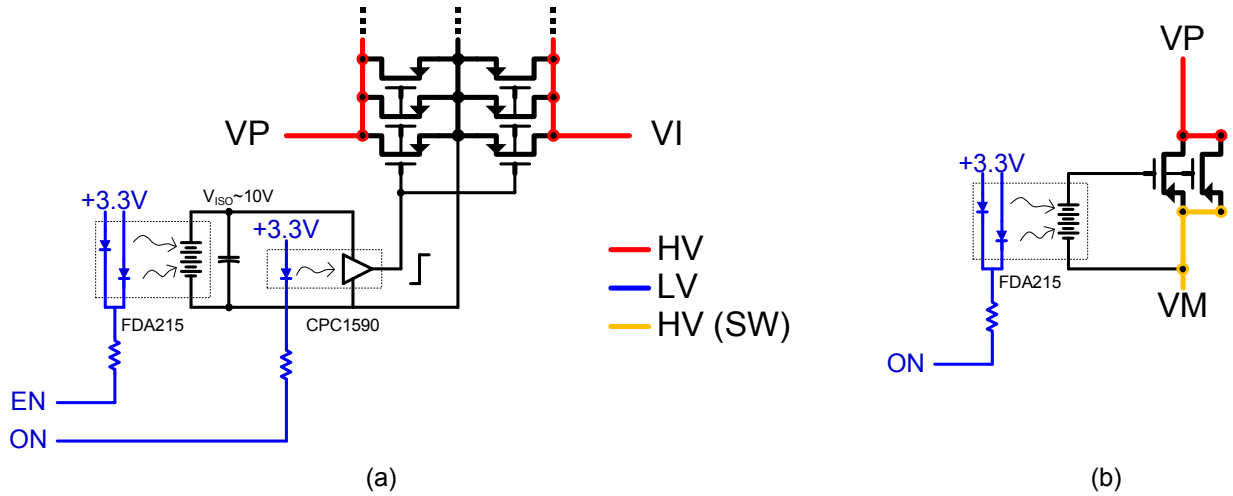

Figure 2: (a) String Disconnect Switch and (b) String Monitoring Connect Switch

The DC switching may present a reliability concern for the disconnect switch. Continuous current flow in one direction exacerbates electromigration failure, which may lead to eventual open circuit failure of the switch. This may be mitigated by oversizing the switch and operating at lower current densities, already required to achieve low series resistance.

String Monitoring Connect Switch

The string monitoring connect switch provides the means for connecting the solar panel string to the load and measurement circuitry. It involves the same long-life, high-voltage, and high-power requirements of the disconnect switch, but can tolerate greater losses since it operates at a very low duty cycle. It requires only unidirectional switching and can operate slower since it can be switched during the load off-state. The connect switch does not have the same reliability concerns as the disconnect switch because of its low on-time.

Shown in **Error! Reference source not found.**(b), the connect switch becomes a simplified version of the disconnect switch. Unidirectional switching eliminates half the switch elements and less concern for power losses during measurement further reduces the number devices. Switching state with no load allows for slower switching speed that eliminates the extra optocoupler.

Note, for an implementation involving a dedicated DAQ module per string, as given in Figure 1, the panel monitoring connect switch may be eliminated altogether, as the programmable load incorporates switching directly, as described later. For an alternate shared load scheme outlined later in the notion trades, each string requires this switch.

Programmable Load

The application requires collection of a number of data points across the operational range of the panel to establish a performance load curve. This requires a series of load conditions spanning the 0 to short circuit current, I_{SC}, and 0 to open circuit voltage, V_{OC}, under full sunlit conditions. This represents a significant power handling challenge as the load must be able to dissipate the full string capacity, nominally 7KW or more. Pulsed or low duty cycle operation can lower heat sinking needs, but power handling capacity exceeds that of any single semiconductor device. That equates to cost and relative difficulty as devices must be paralleled. This suggests notable trades between string capacity and load sharing, as discussed in the notional trades section. The programmable load circuits shown in Figure 3 apply to any scenario as described below.

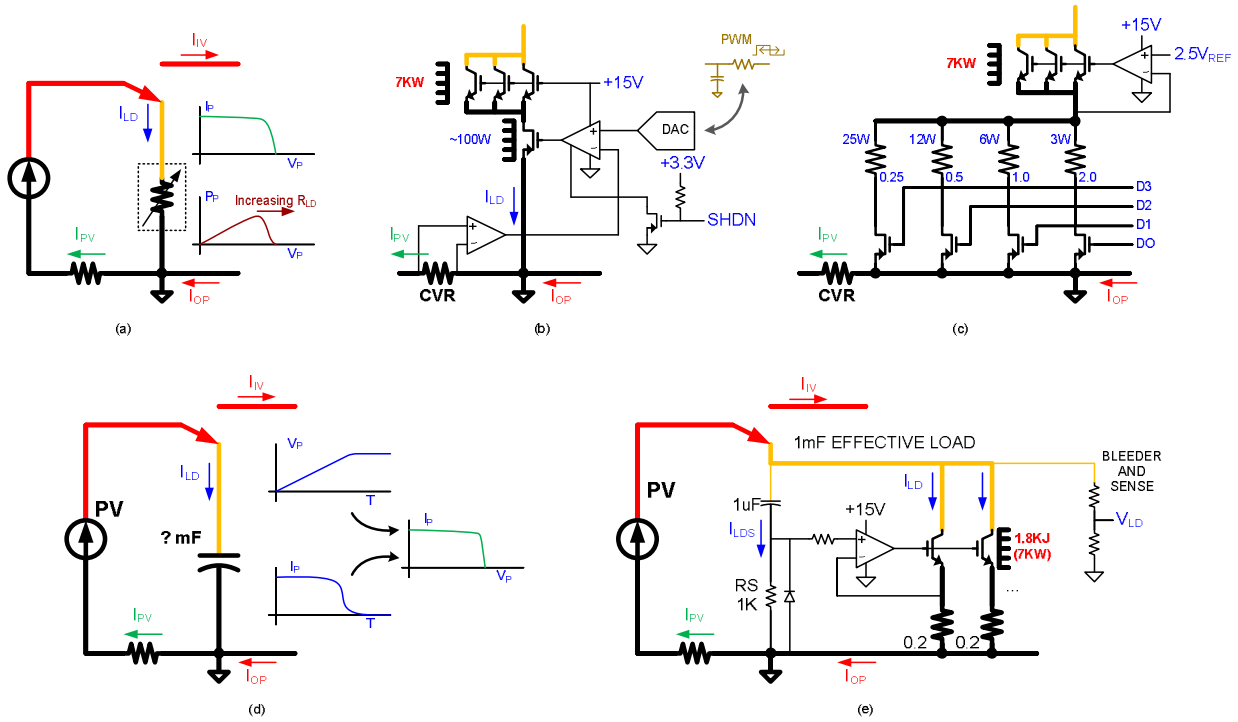

Figure 3: Programmable Loads

Figure 3(a) illustrates the function of the load circuit. As the load varies from a short circuit to open circuit the system collects panel voltage and current data to generate its characteristic curve. The product of the instantaneous voltage and current gives the panel output power clearly defining the maximum power transfer point. Note, critically important to the load design, the load must safely dissipate the maximum panel power in sweeping this curve. This programmable load may be defined in numerous ways as shown.

Analog Closed Loop DAC Load

Figure 3(b) illustrates a basic digital to analog (DAC) driven approach. The DAC converts a digital value to a proportional analog signal. The amplifier servos the panel current as measured across a current viewing resistor to track the DAC output. Thus sweeping a range of DAC values loads the panel with a proportional current. An analog to digital converter (ADC) would sample both panel voltage and current at each step. This circuit illustrates a cascade driver placing the voltage and power burden across the IGBT devices, which relaxes the MOSFET requirements. In the most primitive case, a simple filtered pulse width modulated (PWM) digital I/O signal can be used to generate the analog output or simply sweep the current range directly based on the RC time constant. The I-V curve could be swept in either direction, V_{OC} to I_{SC} or I_{SC} to V_{OC}. The closed loop response of this circuit must be designed for stability to prevent destructive oscillation. This circuit may be simplified by eliminating the feedback and driving the MOSFET to simply produce a timed pseudo-linear sweep, much like the capacitive load below.

Brute Force Switched Load

The approach of Figure 3(c) implements a "power" DAC by brute force using a set of digital I/O signals, (D[3:0]). The signals drive a series of MOSFET switches with binary weighted resistors. As shown, a logic 1 on D3 applies a 10A load, D2 applies a 5A, and so forth for 0-18.75A in 1.25A increments. More resolution requires more bits of data, switches, and resistors, but the circuit does not have the stability issues of Figure 3(b). The I-V curve could be swept in either direction as well.

Capacitor Load

Figure 3(d) illustrates an alternative approach that uses a capacitive load in place of the resistive load. Since photovoltaic cells act like constant current devices, applying the panel across an uncharged capacitor results in it charging linearly with time up to the open circuit voltage.

Safety

For all capacitive loads representing lethal sources a bleeder resistance must be included. A bleeder resistance as low as 100K does not significantly impact the measurements and provides a 0.1s discharge time for a 1uF capacitor. As configured in Figure 3(e), the panel voltage sense can serve as the bleeder.

A capacitive load has the advantage that only the amount of **energy** required to charge the capacitor must be dissipated versus a **sustained power**; however, this energy remains quite large and **peak power** remains the same. Given a 600V, 15A panel, a 1.5mF capacitor would charge in 60 ms (i.e. V*C = i*t). Longer sweep times require a larger capacitor. Secondly, a 1.5mF capacitor charged to 600V stores 180 joules (i.e. ½ CV^2) representing a significant safety hazard. Capacitors of this size and voltage rating have limited availability and typically cost into the hundreds of dollars.

A derivation of the capacitive load appears in Figure 3(e) based on a gyrator or capacitor multiplier circuit. The circuit senses the charging current of a small capacitor across R_S. The amplifier reflects this voltage across a much smaller resistance resulting in a scaled load current and an effective multiplication of the capacitor value. This reduces the cost of the capacitor (although it incurs additional IGBT cost), but perhaps more importantly reduces the stored charge by orders of magnitude making the circuit much safer.

A capacitive load charges automatically based on panel current and capacitor size generating an defined time sweep for sampling that transitions only from I_{SC} to V_{OC}. This requires a sufficiently fast sample rate and possibly sample and hold stage for the ADC, as well as adequate buffer size to store collected samples. The time dependent data collection also means the connect switch must be designed for fast turn-on switching.

Current Measurement

Current measurement can be accomplished by straightforward resistive sensing. Two approaches offer some operational trades. First approach, shown in (a) of Figure 4, places a current viewing resistor (CVR) is series with the panel load to directly measure the load current condition, which equates to panel output. This approach has the benefit of only exhibiting loss during measurement. The second approach, shown in (b) of Figure 4, places the CVR in series with the panel return line. This approach has the

benefit of continuous panel output monitoring at the cost of a minimal loss (~0.01%). This would allow immediate fault detection and potential automatic shutdown response by the local controller. Continuous monitoring would provide real time panel power output statistics.

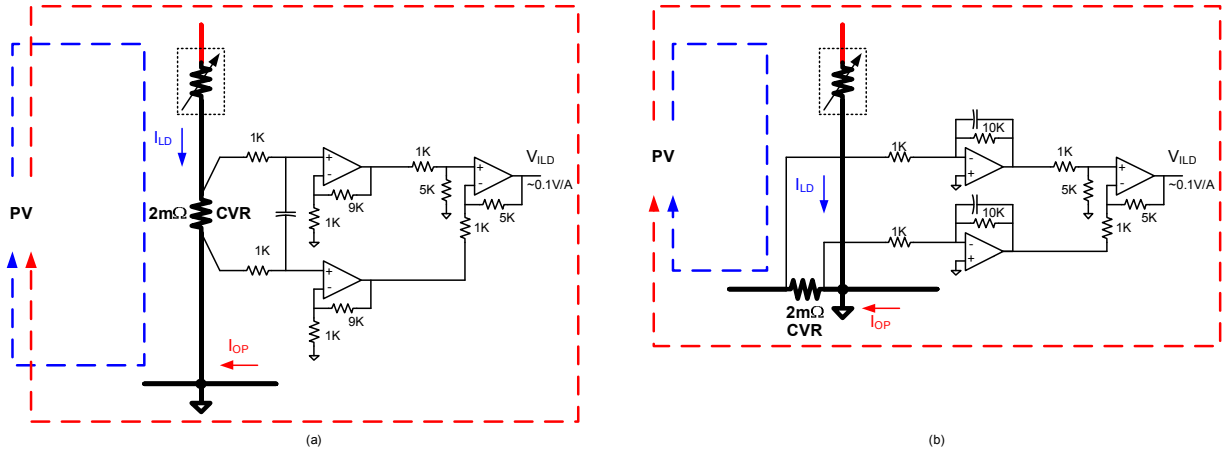

Figure 4: Current Measurement Schemes

In either case, the CVR produces a very small output signal that requires signal conditioning prior to A/D conversion. Both circuits require instrumentation amplifiers to reject common mode ground noise and amplify the small signals to the full range of an A/D. A gain of 50 with a 2mΩ CVR provides a 100mV/A output and nominal full scale of 25A or more. The return line sensing case generates a negative voltage input signal that dictates the inverting input stages. The series source resistors protect amplifier inputs from overvoltage surges caused by current switching transients.

Commercial-off-the-shelf CVRs offer high accuracy, but at significant expense. A couple lower cost alternatives include, 1) the use of a 12” length of #14 gauge copper wire (which can be folded — any way but spirally — to save space, and 2) a printed circuit board trace, nominally 1” wide and 4” long on 2 oz copper clad. Both provide a 2 milliohm resistance with 20A capacity. In both cases layout should use 4-point Kelvin connections. Calibration can be used to restore accuracy, as noted in later discussion.

Voltage Measurement

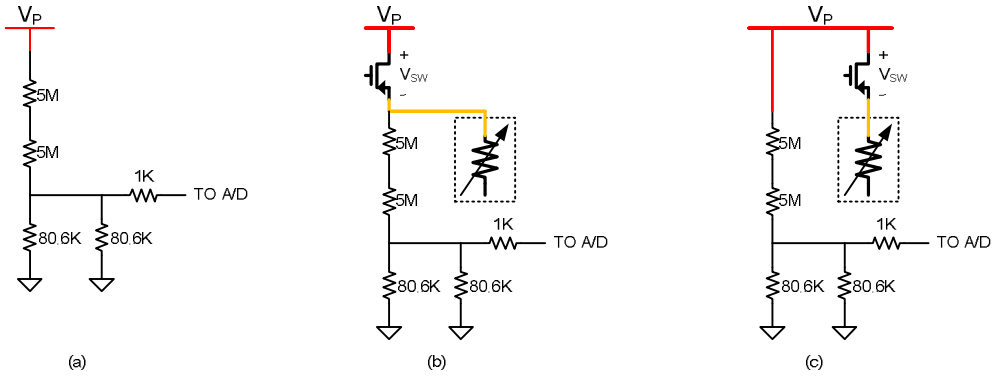

Figure 5: Voltage Measurement Variations

Likewise, voltage measurement represents a similarly easy task, as shown in Figure 5. A voltage divider scales the signal to a range appropriate for A/D conversion. A couple things should be considered in the divider design. For safety, the high side resistance should be broken into 2 or more individual resistors so long-term whisker growth does not cause catastrophic failure to other parts of the circuit. (This may be desirable from a power dissipation perspective as well.) Similarly, the parallel low side resistors guard against open failures. The ADC series input resistor further isolates the circuitry without impacting the measurement. One can decide to sample either switched panel voltage (b) or unswitched (c), or possibly both. Power dissipation in the resistors must be considered too.

As noted in current sensing, calibration can also correct for voltage divider scaling errors. Alternately, the second low side resistor could be used to trim the scaling too. The first resistor is set to approximately 10% higher than the parallel combination and the second adjusted in value to trim the divider to a desired scaling.

Controller and DAQ

(Too) Many options exist for control of the data acquisition board. This proposal assumes that the DAQ operation involves the use of a simple local microcontroller as the tasks are minimal. Designers today tend to jump to high end processors running an operating system (OS) such as Linux, but this represents a severe over kill and compromises critical real time control and sampling actions, at greater expense.

The controller simply needs to respond on demand to perform an I-V data acquisition characterization operation and/or gather real time performance data such as output current, voltage, power, and temperature. This involves controlling and timing the disconnect and connect switches and in between sampling the load current and voltages. When complete the controller outputs a data record.

The particular microcontroller requires a relatively high-resolution, high-speed 12-bit ADC, a serial port, a half dozen digital I/O for switch control, an optional DAC, optional temperature sensing, non-volatile memory for calibration and address information, sufficient RAM for data storage, and flash for program storage. One particular processor, ATXMEGA32E5, meets these requirements and comes in a 32-pin package for about $2. This processor has support via the popular open source Arduino project, but many choices exist.

One of many available processor boards, for example a Spark Core, could be used for development and proof of concept, but real savings would be achieved by dedicated DAQ board implementation that just includes the absolute minimal hardware needed.

Power & Communications

Each DAQ board would require support for on board regulation. Regulating power locally bypasses distribution problems such as ground differences caused by the high power circuits as each regulator can reference its local ground. This prevents ground loops that result in loss of accuracy of analog signal processing and measurement. Routing a +12-15V source per combiner box provides the higher voltage needed by some of the MOS driver circuits. A simple series regulator can provide the +3.3V at minimal current needed by the processor and other signal conditioning circuits.

The DAQ board to CC I/F board communications should use a differential interface such as RS-485, or better an optically isolated interface based on simple optocouplers. New *iCoupler* technology from Analog Devices can offer isolated differential RS-485 interfaces in a single package. Differential signaling provides significant noise immunity relative to ground-side high-current surges. An opto-isolated interface would allow DAQ boards of multiple combiner boxes to route together without fear of power line shorting. Low power Wi-Fi and Bluetooth solutions also offer ground isolation, but security and interference concerns would need to be addressed, as well as the constraint of metal enclosures.

The communication protocol can be a very simple line based (i.e. newline-terminated) command and response handshake messaging. The CC I/F board commands a data acquisition cycle for a particular "address" and when complete the DAQ board echoes its response or an error. This talk/listen approach eliminates bus collision issues and complicated semaphore procedures.

Calibration

Though calibration involves no hardware, it represents an important feature of the DAQ board worth mentioning. Commercial sensors, such as CVRs and voltage dividers, require precise and costly manufacturing to make field interchangeable units that do not adversely affect performance. The presence of a local processor with non-volatile memory allows one to perform a calibration operation on the whole subsystem which translates to much lower cost hardware. Calibration simply requires performing an I-V sweep of a controlled stimulus, processing the data to extract calibration factors (i.e. offsets and scale factors or fit coefficients) that then get loaded back into the DAQ board via a command sequence. Software then corrects real measured data based on the calibration data to output ideal measuremnts.

Computation and Communications Interface (CC I/F)

The computation and communications interface board provides a tiered approach to these two functions. This approach abstracts the system functions dedicating the I-V DAQ board to collecting measurements and offloading data processing and reporting to the CC I/F board. Any of a number of single-board computers could serve this need with two recommended paths: 1) an open-source Arduino based board, and 2) a Linux based board such as the Raspberry Pi, BeagleBone, or Galileo.

An Arduino based board offers an open source publically available design base. These designs do not implement an operating system (OS). This allows better real time interaction with significantly less overhead and maintenance, but lack higher level capability such as scripting languages and greater interoperability.

The Linux based boards offer much higher performance and capability at the cost of OS maintenance where load term operation, security, and upgrades can be a nightmare for embedded hardware. The Raspberry Pi offers breakout of several popular interfaces for low level hardware communications as well as SD Card storage and Ethernet communications. The Galileo board sports both a high end processor running Linux and an Arduino compatible interface with an appropriate cost trade.

These factors must be traded. One system may be better suited for faster or easier prototyping and another for field implementation. In both cases a minimal adapter board would undoubtedly be

required mainly to provide a local RS-485 or optical interface, as well as power distribution, to the I-V DAQ board. Arduino likely has off-the-shelf “shields” to support prototyping but lower cost would be achieved by a custom board.

The CC I/F block could support one or more combiner boxes and performs the following operations.

Data Collection

This task simply involves commanding each I-V DAQ board to request I-V data from each specific panel and parsing the return data into variables data. As mentioned for the I-V DAQ board, communications would be minimal. Data should be structured with a message wrapper header encapsulating some form of simple point data records, such as voltage-current pairs for easy parsing. Each message should include a cyclic redundancy check (CRC) or error correcting code to ensure data integrity.

Computations

The computational throughput depends largely on the level of analysis needed or desired at this tier. To a first order, I-V data needs to be checked and validated as a representative I-V curve. One could further extract vital parameters such as open circuit voltage, short circuit current, maximum power, and a figure of merit for collector output. Advanced processing could apply filtering techniques and curve fitting for data smoothing and noise immunity.

The computational analysis could be used to decide string performance independently or more appropriately by comparison across a group of strings. Since a single combiner box aggregates a number of “equal strings”, the analysis could locate outlier performance of individual strings relative to a group of strings. This would for example normalize sun intensity as variable sun level would result in a common mode shift of all strings.

Any of the mentioned boards have more than enough capability to perform such computations particularly since it does not involve any significant time constraint. However, Linux based systems would have a variety of much more powerful tools available for the task.

Central Communications

Any implementation would require higher level communications to a central authority. This could be used to report maintenance problems, including identifying the specific problem string.

An important consideration for the communications at this level involves ground isolation to prevent ground loops and noise that would otherwise corrupt communications and potentially result in safety and operational concerns. Ethernet, which uses transformer isolation or fiber, becomes an ideal medium in this case.

Cost Evaluation

Table 1 provides a very simple cost breakdown for quantifying the concept. This is provided to identify relative cost sinks for the purpose of concept trades, not absolute implementation costs. Obviously, cost represents a large driver for system effectiveness. The goal would be to minimize costs both from an

initial investment of hardware as well as across the operational lifetime, which likely extends multiple decades.

ELEMENT	DESCRIPTION	ESTIMATE
I-V DAQ BOARD		
	Printed Circuit Board	$20
	Disconnect Switch: 2 MOSFETS, fast switching	$67
	Connect Switch: 1 MOSFET, fast switching	$37
	Load: IGBT (8ea IXYH820N120C3), 1 uF cap, power resistors, heatsink	$100
	CVR: #14AWG, quad opamp	$3
	Voltage Divider: resistors	$1
	Controller: ATXMEGA32E5	$2
		$230
CC I/F BOARD		
	Raspberry Pi	$35
	USB Power Supply	$10
	Adapter board: RS485 I/O, power inverter (e.g. VBT1-S5-S12-SMT-TR), PCB	$20
		$65
COMBINER BOX EXAMPLE		
	8 each I-V DAQ boards	$1840
	1 each CC I/F board	$65
COMBINER BOX TOTAL		**$1905**
COST PER WATT @ 56KW		**<$0.034/W**

Table 1: Cost Estimate

NOTES:

1. Assumes prototype quantities. Does not include board development and assembly labor. Large scale costs could be significantly reduced.
2. Miscellaneous terminal connectors, screws. Mounting hardware, etc. not considered.
3. Load design capacity, 10KW, 1200V.

The table shows a total combiner box cost estimate of $1905 amortized for the representative 56KW capacity equates to less than $0.04/W system impact. The obvious cost driver is the load, which is driven by the IGBT cost of $80. Secondary cost drivers include the disconnect and connect switches driven by the low-loss MOSFETs.

Notional Solution Trades

The discussion to this point has assumed the application of the I-V DAQ function on a per string basis broken into 2 board implementations. Obviously many options exist for implementation and many trades to consider. The following addresses a few significant cases.

Shared Load

The most obvious trade, which focuses on cost, involves the use of a shared programmable load circuit. A single load circuit shared across 8 strings would cut cost nearly in half to $0.021/W. This notion drives

the board partitioning too, as it suggests perhaps it makes more sense to implement a standalone per panel switching and sense function, which can be easily physically distributed as needed, that feeds to a central DAQ and adapter board. The adapter then connects to a processing board, as shown in Figure 6, which might even be shared across multiple boxes. This partitioning would not be as flexible and generally limited to within one combiner box as routing of the control, sense, and load signals becomes less forgiving over greater distances. Figure 7 shows a possible artistic rendering of this notion.

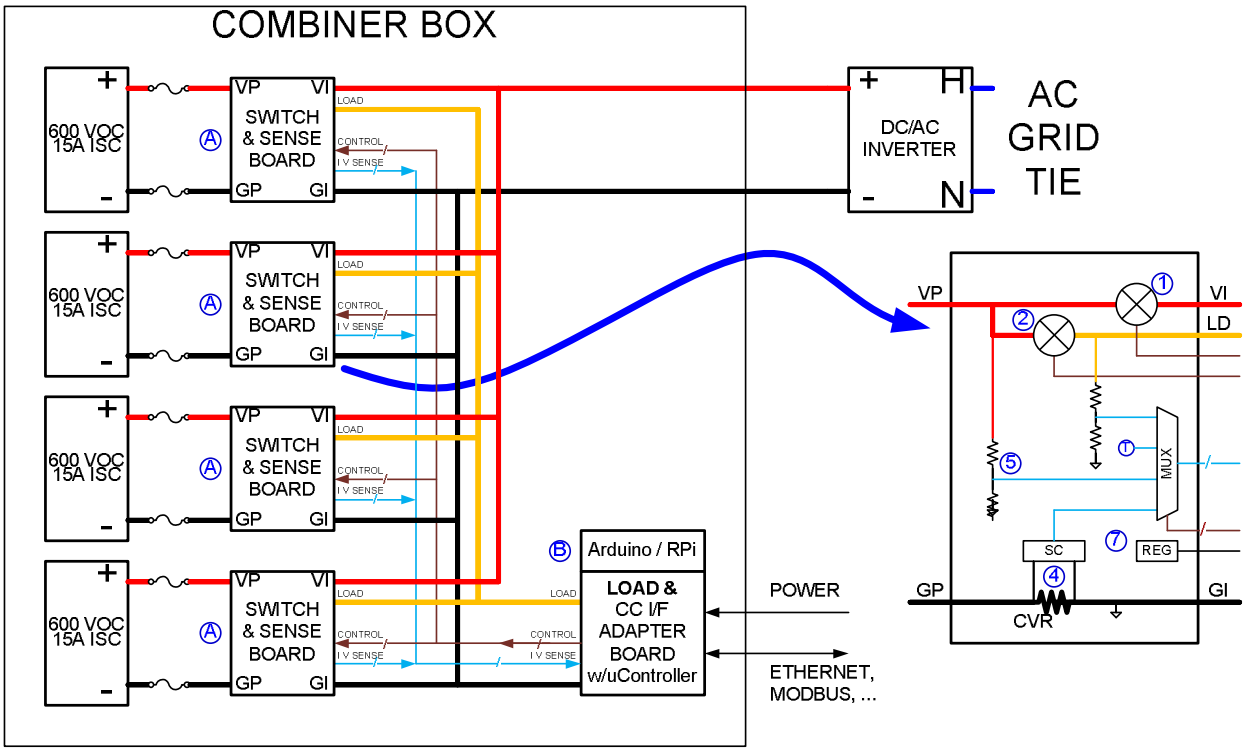

Figure 6: Shared Load Architecture

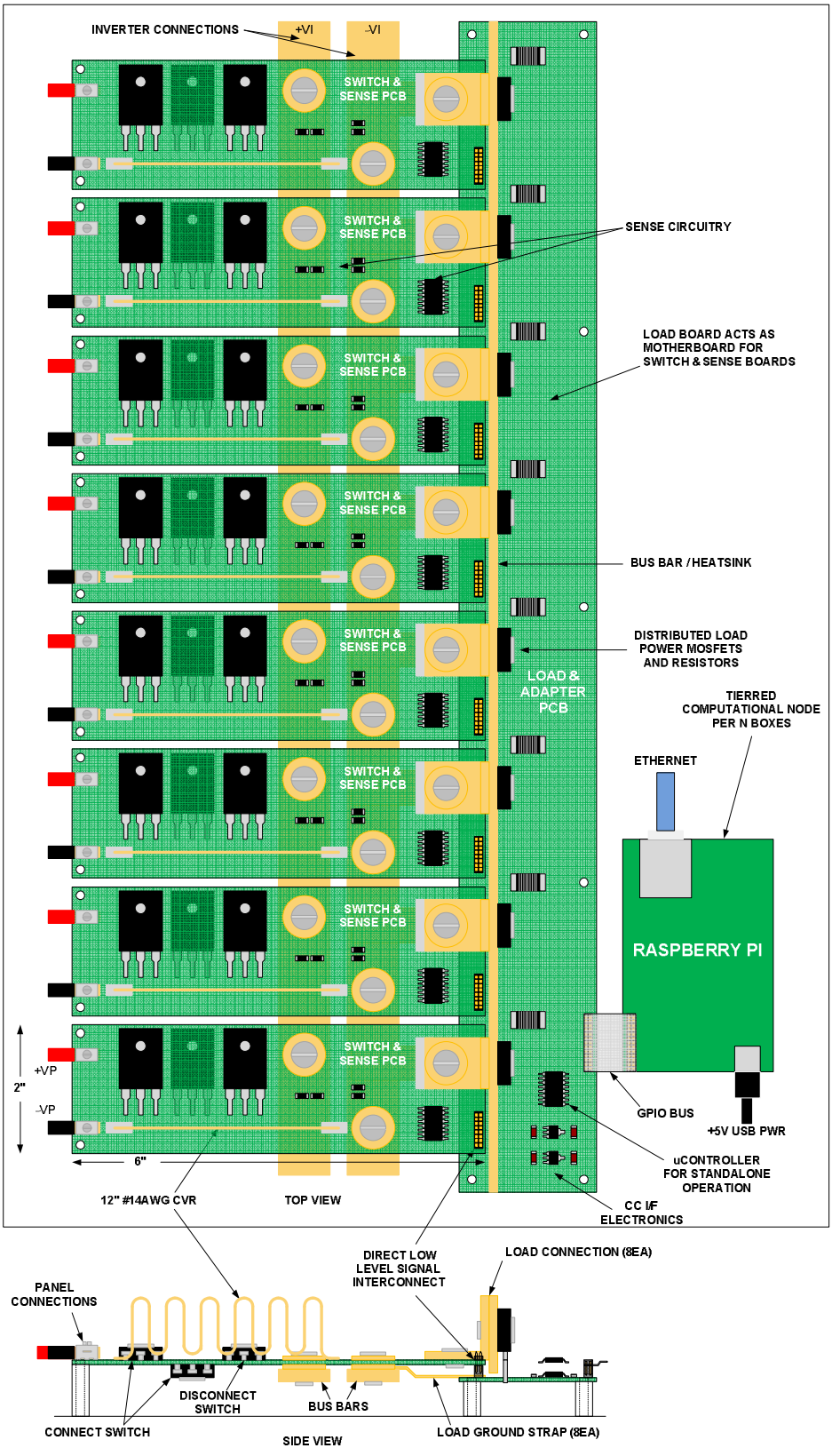

Figure 7: Artistic Rendering of Shared Load Concept

Per Substring

Per substring versus string trades really comes down to a matter of string capacity. Smaller string capacities would offer lower per switch cost, but more switches. Any option related to capacity is likely constrained by other installation factors. A particular factor to note is that most semiconductor switches are limited to 600W dissipation in a single package, with a few IGBT devices able to reach 1200-1500W. This suggests a solution might be optimized at this power level.

Other Considerations

Safety

The application involves lethal voltages and currents. A number of safety issues have already been noted, still it would be prudent to perform a safety based review of all design efforts.

Reliability and Failures

All designs would benefit from a reliability assessment and failure review as well. Because of the extremely high-voltage and currents involved extra measures should be taken to isolate board interfaces to avoid unintended failures and consequences. For example, a high-voltage switch failure may route excessive power to unexpected points. Some simple efforts such as resistor isolation of I/O can prevent problems from having a ripple effect and extending catastrophic and costly damage system wide. Such failures may also expose abnormal safety concerns that could be addressed.

Loss Trades

An end-to-end system loss analysis would allow better optimization of the design. Losses in a system are like noise or links in a chain. Going to great expense to eliminate one loss may be a wasted effort and costly endeavor if that loss represents an insignificant part of the total. This discussion assigned somewhat arbitrary losses to problems and circuits. A better understanding of where all losses occur would lead to a better understanding of trades and could potentially drive lower costs.

Environment and Fan

The high power dissipation of the load may benefit from an air circulating fan. The fan might be controlled to only operate during load dissipation (i.e. data gathering) as to not lower system efficiency. This goes hand in hand with knowing operational environments.

Standards Establishment

This activity, as demonstrated in the surge of home systems, would benefit from standardized I-V characterization hardware. A demonstration concept provides a solid platform for establishing industry standards. These standards allow multiple parties to implement interchangeable boards or functional elements to lower cost through competition and ensure success and long term support through having alternate vendors.

Summary Notes

The above discussion identifies the elements and concerns for implementing practical in-situ I-V characterization of photovoltaic panel arrays. The task certainly represents obtainable goals and does not require any science or technology development, simply board and system engineering work. As defined and outlined, the scope of development activity represents an excellent under graduate class project. The many specific tasks could be distributed across multiple competing teams. The work has well defined boundaries and encapsulates elements of direct engineering – mechanical, electrical, thermal (power and energy), safety, reliability, and system – as well as a number of financial and deployment trades to serve as a learning tool for many job related skills.