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5-Level MEMS Technology with Integrated n-MOS Electronics

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NNSA National Nuclear Security Administration

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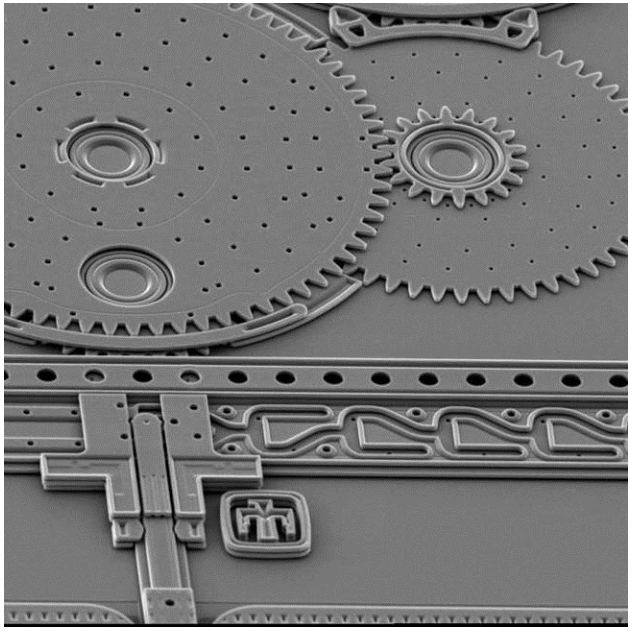
Abstract

The Sandia SUMMiT™ technology is a 5-layer planarized silicon surface micromachining process for fabricating microelectromechanical systems (MEMS). A simple modification of the SUMMiT process flow allows for simultaneous fabrication of n-MOS transistors that can be used for applications such as digital switching and on-chip charge amplification.

SUMMiT™ MEMS Technology

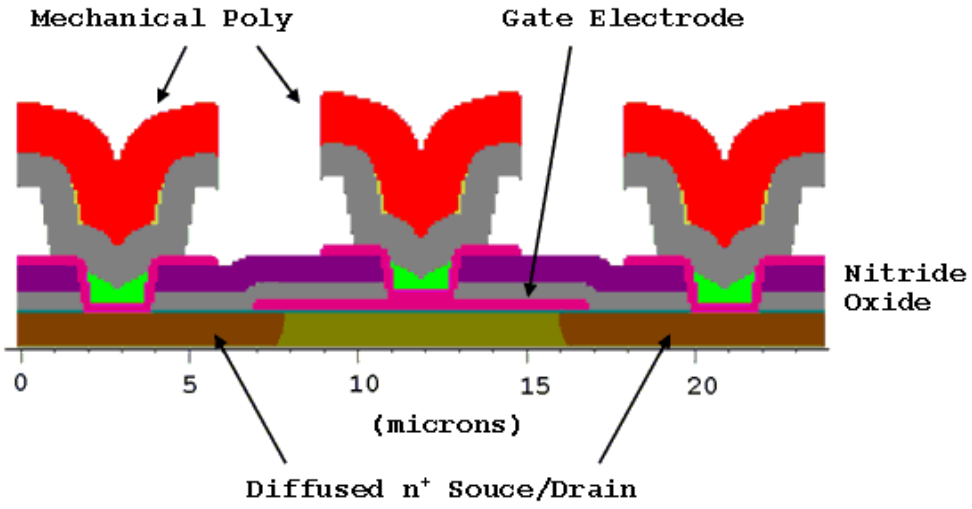
- The Sandia SUMMiT™ technology is a 5-layer MEMS process – 4 mechanical layers + 1 ground plane.
- All layers are fabricated from n-type, in-situ doped polysilicon
- Thermal annealing is used to relieve residual stress in the polysilicon, yielding virtually stress-free structures.
- 4 stress-free mechanical layers allows for fabrication of highly complex MEMS devices.



MEMS mechanical discriminator, fabricated in SUMMiT™

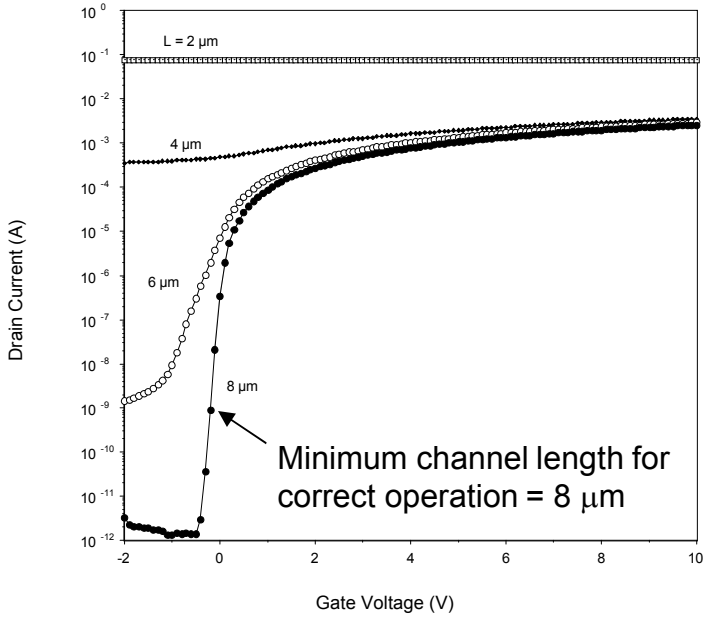
SUMMiT™ + FET (SFET)

- One additional mask level, for the gate electrode, is required to add n-MOS circuitry.
- Transistor gate is defined at beginning of the process; all remaining steps are standard SUMMiT™.
- Source/Drain regions created by solid source diffusion of phosphorous from MEMS n-type polysilicon into a p-type substrate.
- Source/Drain drive-in occurs during stress-relief anneals.



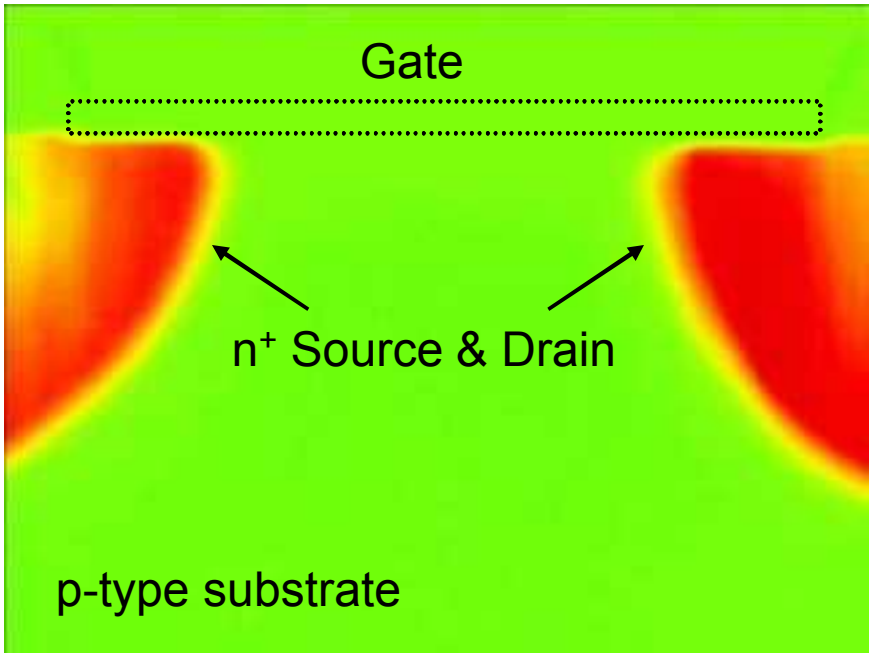
SFET Design Considerations

- SUMMiT™ stress relief anneals result in substantial diffusion depth of phosphorous into the substrate
- Channel length must be long enough to prevent short-channel effects or merging of source and drain regions.
- Thick gate oxides are required to survive the thermal budget and high voltages.
- Relatively large devices (tens of microns) may constrain circuit design.
- ***Ideal for switching and amplification applications.***

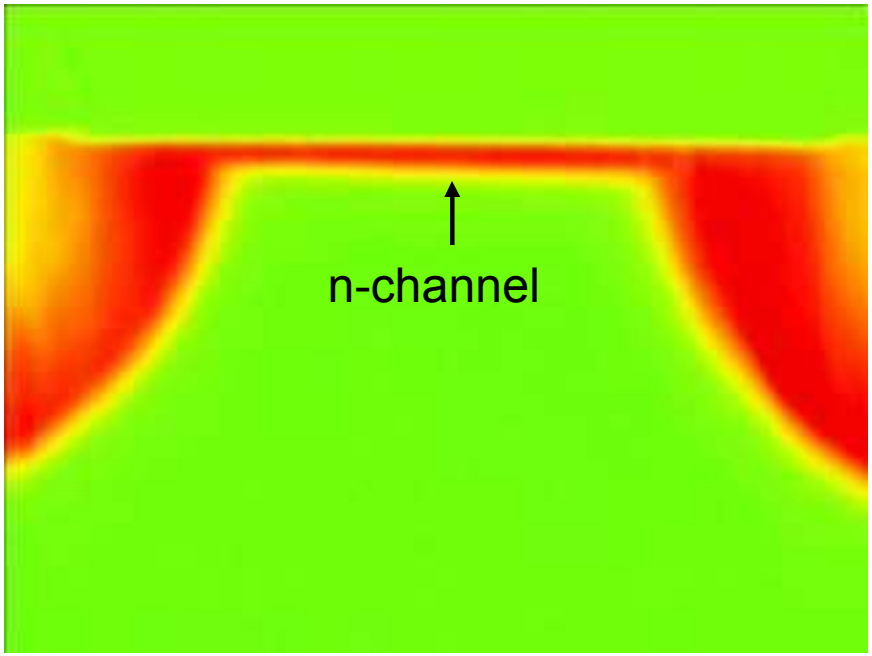


SFET Transistor I-V curves for various channel lengths

Scanning Capacitance Micrographs



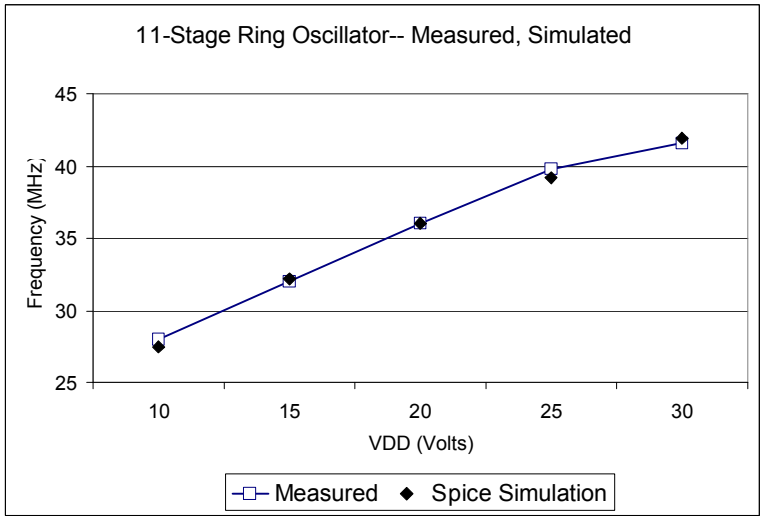
No gate bias (off state)



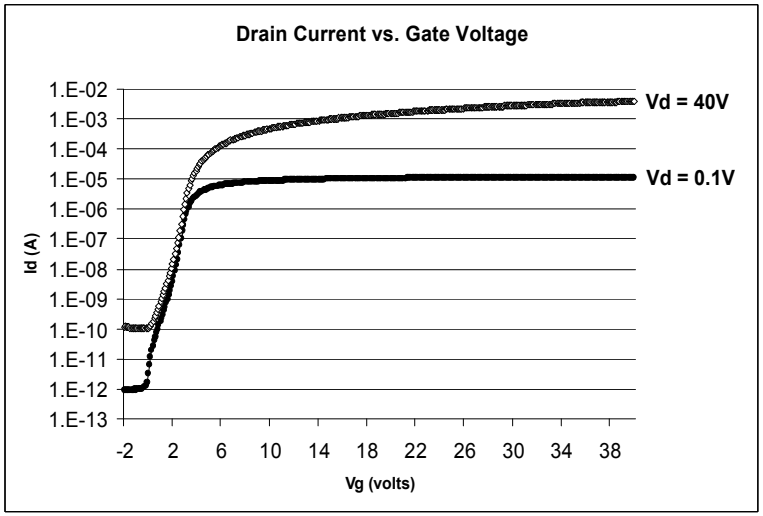
Gate bias applied (on state)

SFET Performance

- Electrostatically actuated devices require high voltage – SFETs have been tested up to 40 V; adequate for many MEMS devices
- Frequencies over 40 MHz have been demonstrated – much greater than the natural frequency of most MEMS devices



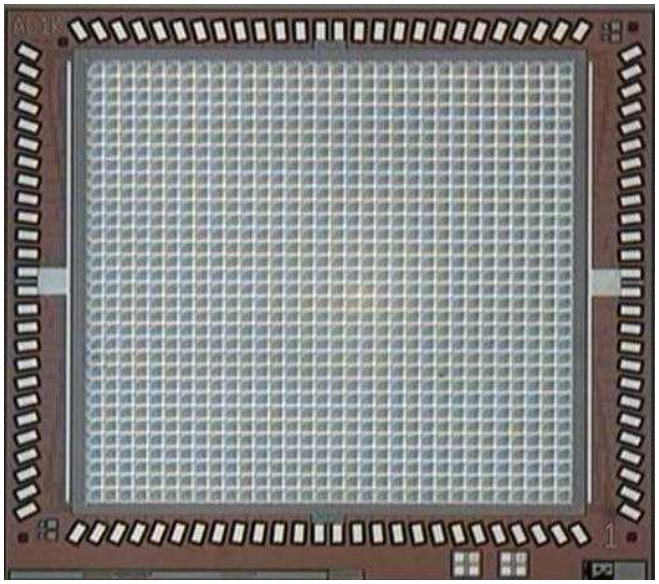
Ring oscillator performance

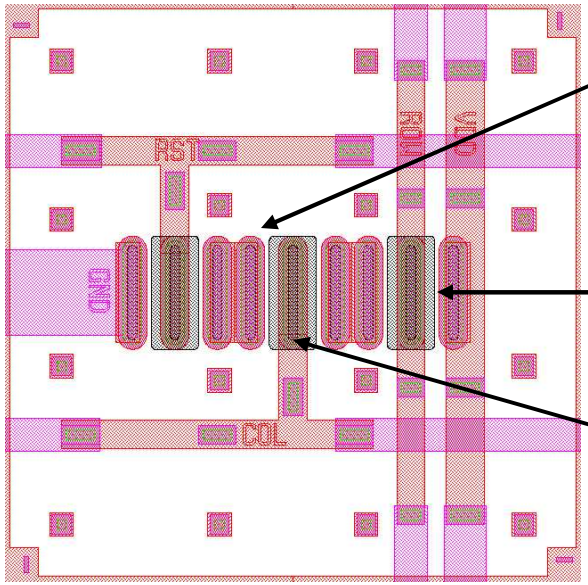


High voltage performance

SFET Application – Mirror Array

- SFET switching fabric used to actuate individually addressable mirrors
- Without SFET, **n^2** leads are required for an n x n array (piston motion only).
- With SFET, **2n** leads are required for the same functionality
- Only 66 leads required for row-column addressing of a 1024 mirror array



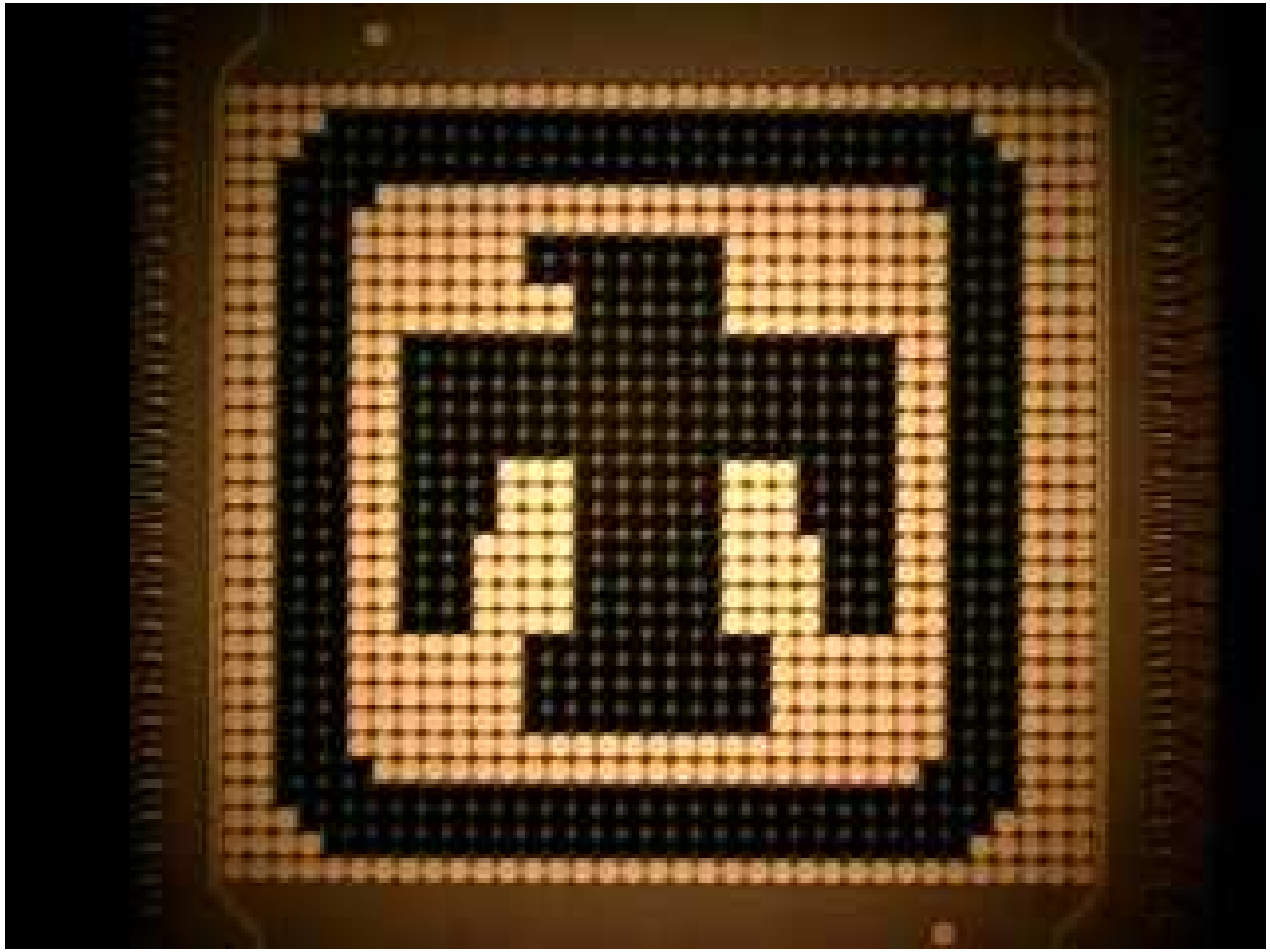


Electrode contact

Row transistor

Column transistor

1120 Element Mirror Array



Individually addressable; 120 Leads

Conclusions

- SUMMiT™ is a robust, manufacturable process for fabricating complex MEMS devices in 5 levels of polysilicon.
- A simple modification (one mask level) provides n-MOS electronics, while maintaining all of the benefits of the SUMMiT™ technology.
- Transistors operate at voltages and frequencies that are compatible with electrostatically actuated MEMS.
- Transistors have been used to control mirror arrays, dramatically reducing the number of leads required for packaging.