SAND2014-3953P

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Sandia's ASC Advanced Architecture Test Beds

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ADVANCED ARCHITECTURE TEST BEDS

U.S. DEPARTMENT OF ENERGY

NNSA National Nuclear Security Administration

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Advanced Architecture Test Beds

- Reduce impact on mission labs in a rapidly changing technology environment.
  - **SIGNIFICANT** production code rewrite or modification may be required
  - Ensure that when we make "the change" it is the right move for code longevity, porting efforts, performance *etc.*
  - Go through all the pain up front so the transition for full codes is made easier
  - Eliminate or reduce missteps
  - **APPLICATION FOCUS**
- **Speed Boat vs. Cruise Ship**
- **Mini-Apps vs. Production Codes**
- *Essential to enable solving many of the challenges discussed this week!*

Advanced Architecture Test Beds

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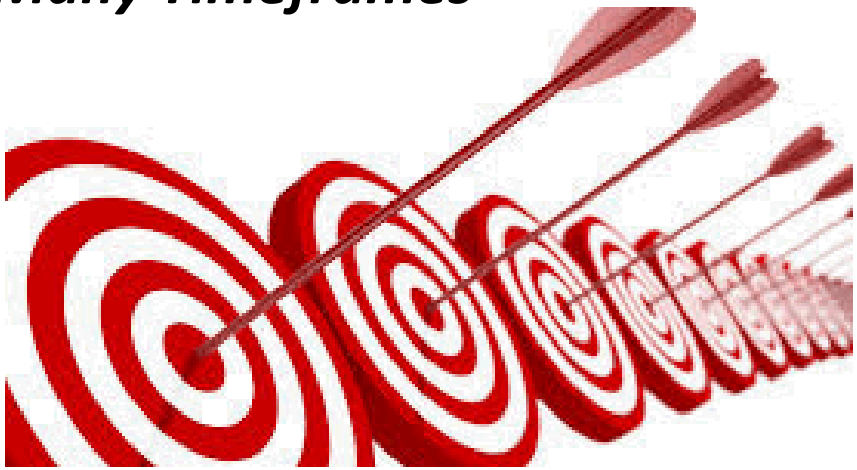
- Current state of technology REQUIRES exploratory R&D of:
  - Alternative Programming Models
  - Architecture-aware algorithms
  - Advanced memory sub-system development
  - Energy Efficient Hardware, Runtime, Systems Software, **AND APPLICATIONS**
- Philosophy
  - Hardware and Software intended (and has proved to be) to be highly dynamic
  - **INTENTIONALLY** closer to prototypes than production
  - Systems are **NOT** for production cycles
  - Priority is to explore a wide and diverse set of emerging architectural alternatives **@ rack scale**
- First Rule of Test Beds
  - NEVER say no
    - At least to any reasonable request ☺
- Numerous custom hardware changes
- Even more custom software configurations

Target(s)

- Long
  - Exascale
  - Best chance to impact hardware
  - Power/Energy
- Medium
  - ATS program
  - Impact hardware
  - Direct NRE
  - Programming Models
  - Power/Energy
- Short
  - ATS/CTS program
  - Programming Models

Many Targets

Many Timeframes



Longer the timeframe
- better the chance for more significant influence

Westmere + Knights Ferry

Arthur

SandyBridge Knights Corner (B)

Compton

SandyBridge Knights Corner (C)

Compton V2

IvyBridge

Volta (XC)

Haswell + PowerInsight V2

TBD

Llano+ PowerInsight

Teller

Trinity + PowerInsight

Teller V2

Kaveri+ PowerInsight V2

TBD

Interlagos + Fermi 2090x

Curie (XK6)

Interlagos + Kepler K20X

Curie (XK7) V2

SandyBridge + Kepler K20

Shannon

SandyBridge + Kepler K20 + K40

Shannon V2

SandyBridge Kepler K20 + K40 + TBD

Shannon V3

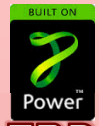
Power 7 + FPGA

Watson

Power 8

ESP

Power 8



TBD

64bit

ESP

64bit

Hammer

HMC

JENGA

PLANNED

Sept. 2011 | Sept. 2012 | Sept. 2013 | Apr. 2014 | Sept. 2014

Example Analysis using Test Beds

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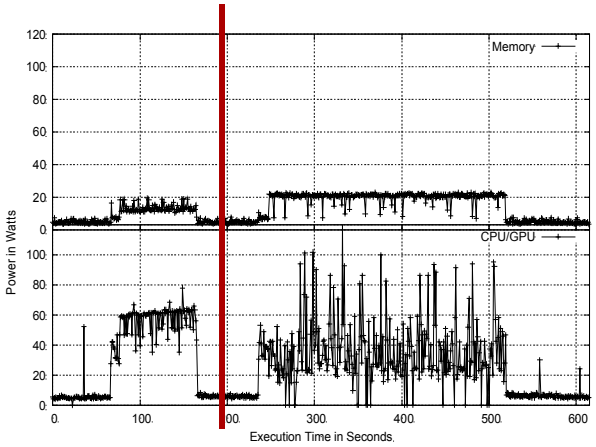
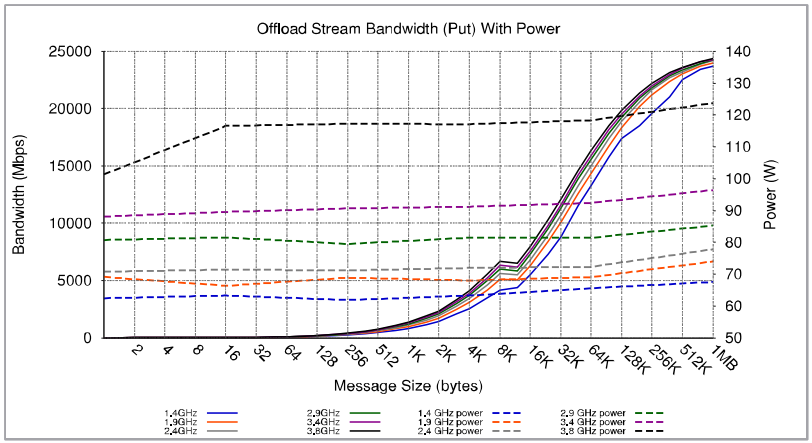
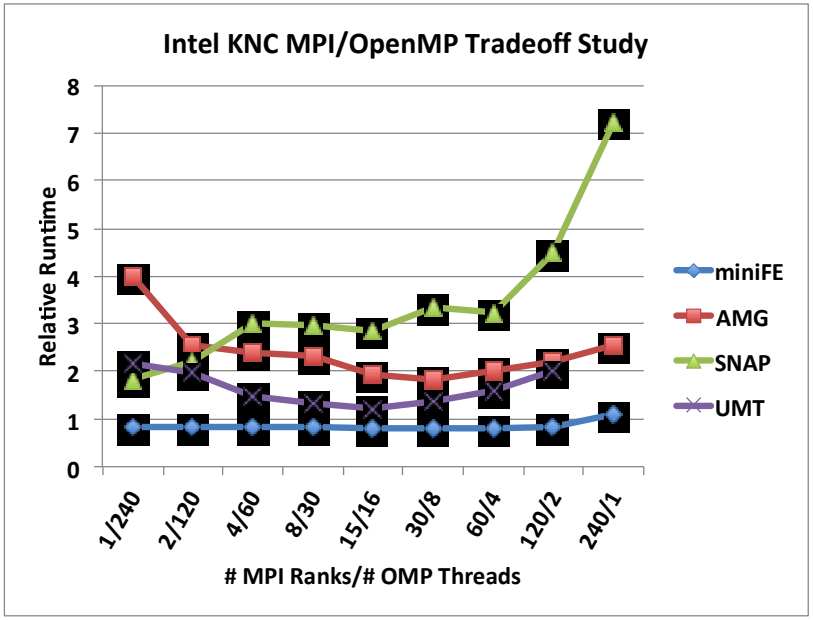
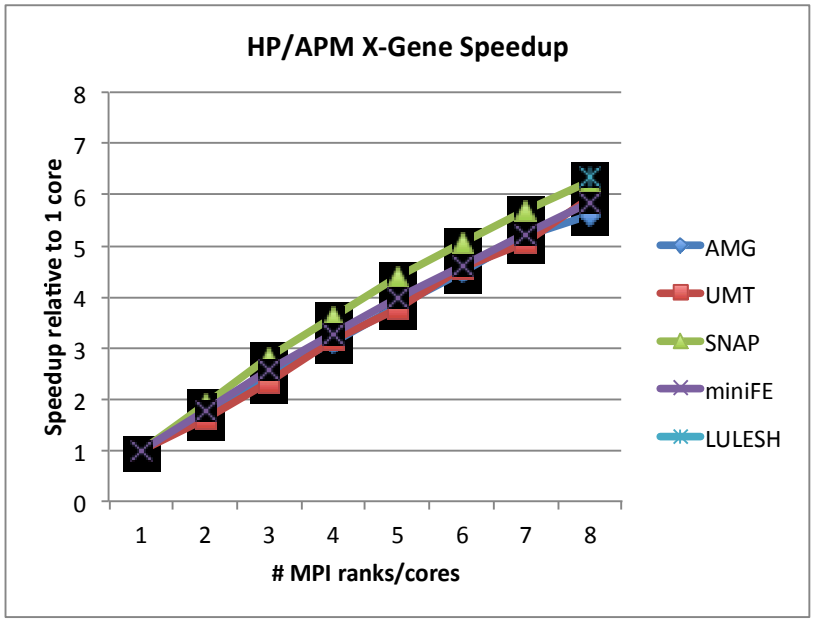


PowerInsight







A Closer Look

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Hostname	**Compton**	**Curie**	**Shannon**	**Teller**	**Volta**	**Morgan**	**Hammer**
CPU	Dual Intel Xeon CPU E5-2670 8 cores @ 2.60GHz Sandy Bridge	Dual AMD 6272 8 cores @ 2.10GHz Interlagos	Dual Intel Xeon CPU E5-2670 8 cores @ 2.60GHz Sandy Bridge	AMD A10-5800K 4 cores @ 3.80GHz Piledriver	Dual Intel Xeon CPU E5-2695 v2 12 cores @ 2.40GHz Ivy Bridge	Dual Intel Xeon CPU E5-2670 v2 12 cores @ 2.50GHz Ivy Bridge	64 Bit ARM APM X-Gene 8 cores @ 2.40GHz
Accelerator	Pre-Production Intel Xeon Phi (KNC) 2 per node	Nvidia Kepler K20X	Nvidia Kepler K20X and K40X	Radeon Northern Islands (on die integration)	None	Intel Phi (KNC C0) Nvidia K40X	None
GPU cores	57 - 1.1GHz	2688 732 MHz	2688 732 MHz	384 @ 800MHz	N/A	57 @ 1.1GHz 2688 @ 732 MHz	N/A
Nodes	42	52	32	104	56	4	8 (to be 45)
Interconnect	Mellanox QDR IB	Gemini	Mellanox QDR IB	QLogic QDR IB	Aries	Mellanox QDR IB	10GigE
Other	80GB SSD per node	Full featured RAS sys SRN	Full PCI Gen 3 NVIDIA GPU Direct	Integrated CPU/GPU+ 256GB SSD/node PowerInsight	Full featured RAS system including power monitoring and control	SRN	

Questions?

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