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What's Beyond Moore's Law?

Point Study Kickoff Meeting
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National Nuclear Security Administration

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Sandia National Laboratories

Study Team

- Mr. K. K. Ma (STE, Contact)
  - Embedded System Architecture; Radiation Effects; Rad-hard CMOS
- Dr. DeBenedictis, Erik (STE)
  - High Performance Computing Architecture; Quantum Computing; Space Borne Computing
- Dr. Dirk, Shawn (PRS)
  - Materials Development of Surface Chemistry, Sensors, Nanocomposites, Molecular Electronics
- Dr. Dodd, Paul (PRS)
  - Rad-hard CMOS Technology; Radiation Effects, Characterization, Modeling and Simulation
- Dr. Lentine, Anthony (PRS)
  - Silicon Photonics
- Dr. Murphy, Richard (PRS)
  - High Performance Computing
- Dr. Siegal, Michael (PRS)
  - Growth and Characterization of Thin Films, Coatings, and Carbon Nanotubes
- Mr. Tarman, Thomas (PRS)
  - Secure, High-performance Systems Architectures; Quantum Information Processing
- Dr. Watts, Michael (PRS)
  - Silicon Photonics

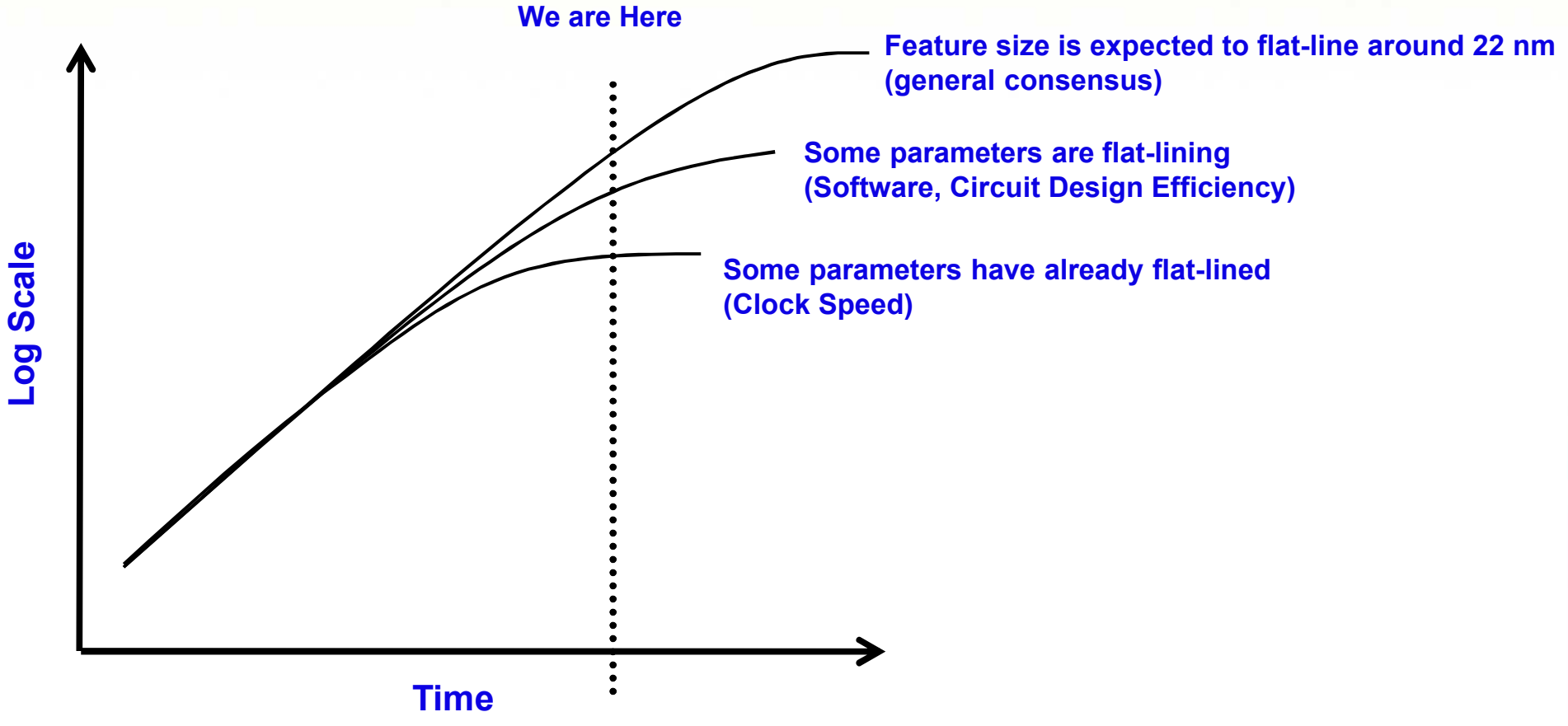
Outline

- Overview of Moore's Law
  - Definitions: Moore, ITRS, Others
  - Flat-lining of Moore's Law and related parameters
  - How long will Moore's Law be sustained?
- Implication of CMOS maturation
  - Architecture
  - Software
  - Hardware
  - Technologies
  - Government Specific Considerations
- Replacement of Silicon Transistor (Beyond CMOS)
  - AND-OR-NOT based technologies
  - Others: Reversible logic; Neural networks….
  - Quantum-effect based technologies
  - Government Specific Considerations

Definition of Moore's Law

- **Moore**
  - **The number of transistors that can be inexpensively placed on an integrated circuit is increasing exponentially, doubling approximately every two years. Power/area is constant with increasing speed.**
- **ITRS**
  - **Density, Speed, Power/op**
  - **More Moore, More Than Moore, Beyond CMOS**
- **Others: Measure of the capabilities of digital electronic devices are linked to the Moore's Law, improving roughly at exponential rate.**
  - **Density at minimum cost per transistor (Moore)**
  - **Transistors per integrated circuit**
  - **Cost per transistor**
  - **Computer performance per unit cost**
  - **RAM storage capacity**
  - **Network capacity**
  - **Pixels per dollar**

Flat-Lining of Moore's Law and Other Related Parameters



Implication of CMOS Maturation – Improving Implementation Efficiency

- Architecture
  - Other Architectures such as multi-core, SIMD, MIMD, will become more prominent
- Software
  - Multi-thread programming and other heterogeneous architecture programming
- Hardware
  - Cell-based Design; Structured Design; ASIC; FPGA; Memories (most importantly, NVMEMs)
- Technologies To Improve System Performance
  - Photonics for communication
  - 3D Integration
- Government Specific Topics
  - Trusted Foundry and Supply Chain
  - Radiation Hardening
  - Maintaining Technology Leadership

Replacement of Silicon Transistors – AND-OR-NOT Nanotechnologies

- Examples of AND-OR-NOT nanotechnologies
  - Nano FETs, Nanoswitches, Memristor
- AND-OR-NOT nanotechnologies are subjected to kT energy limit
- These nanotechnologies may be significantly more efficient than silicon-based transistors, hence extending the Moore's Law for several decades
  - Density
  - Speed
  - Power
- Many concepts and devices have been demonstrated
- Investments in AND-OR-NOT nanotechnologies may have a short-term payoffs
- AND-OR-NOT nanotechnology may be a stepping stone to Quantum based nanotechnology

Replacement of Silicon Transistors – Quantum Based Technologies and Others

- **Examples**
  - **Quantum Computer, Spintronics, Artificial Intelligence, Reversible Logic**
- **Major breakthroughs required to make these technologies a reality**
- **We will examine these technologies from two perspectives**
  - **Potential impact**
  - **Schedule (breakthroughs required)**

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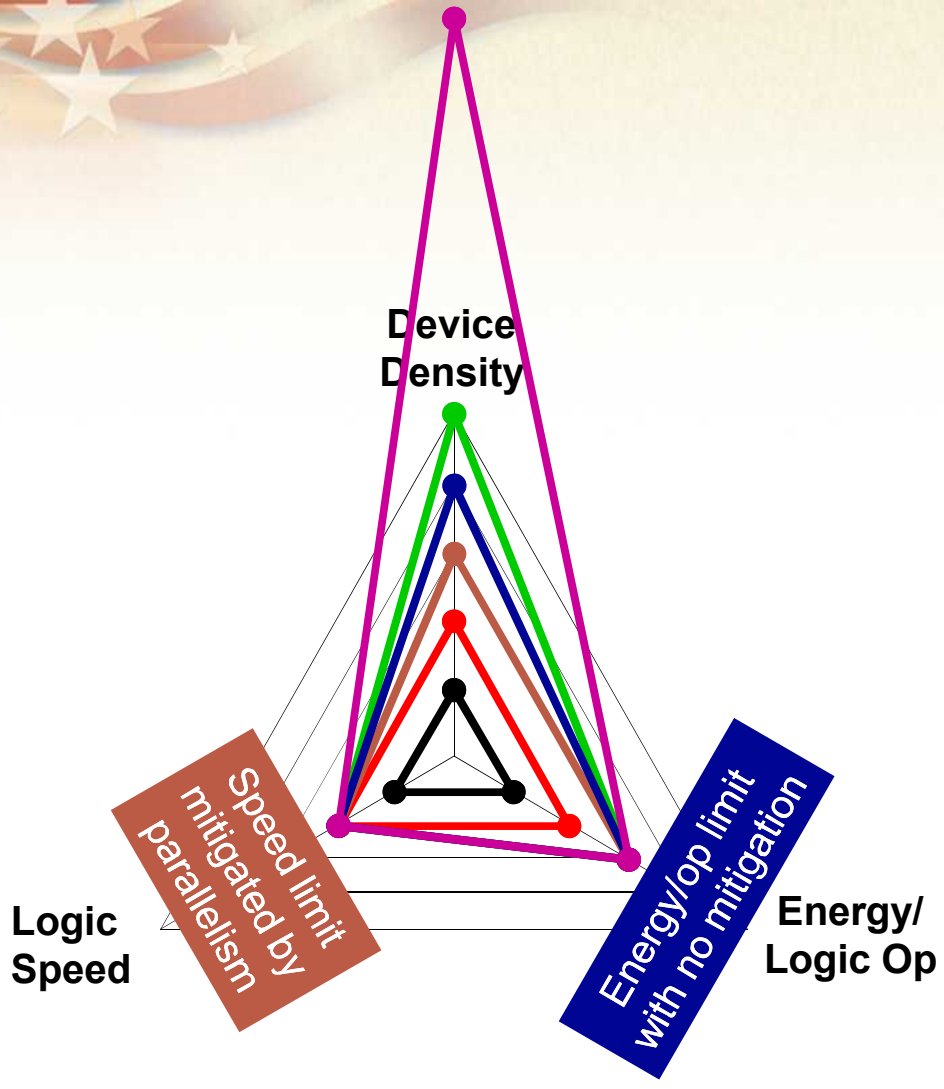
- Theory of Moore's Law
- Implications of CMOS Maturation
- Nanotechnologies to Augment CMOS
- Beyond CMOS
- Implications to Government Policy

Technology Issues



- The original Moore's Law had balanced scaling
- Unbalanced scaling now
  - Speed scaling slowed
    - Mitigation: parallelism
  - Energy/op scaling limit in sight
    - No direct mitigation
    - Temporary fix through architecture
- The only long term options are "exotic approaches"

Forward: Answers to Questions in SOW

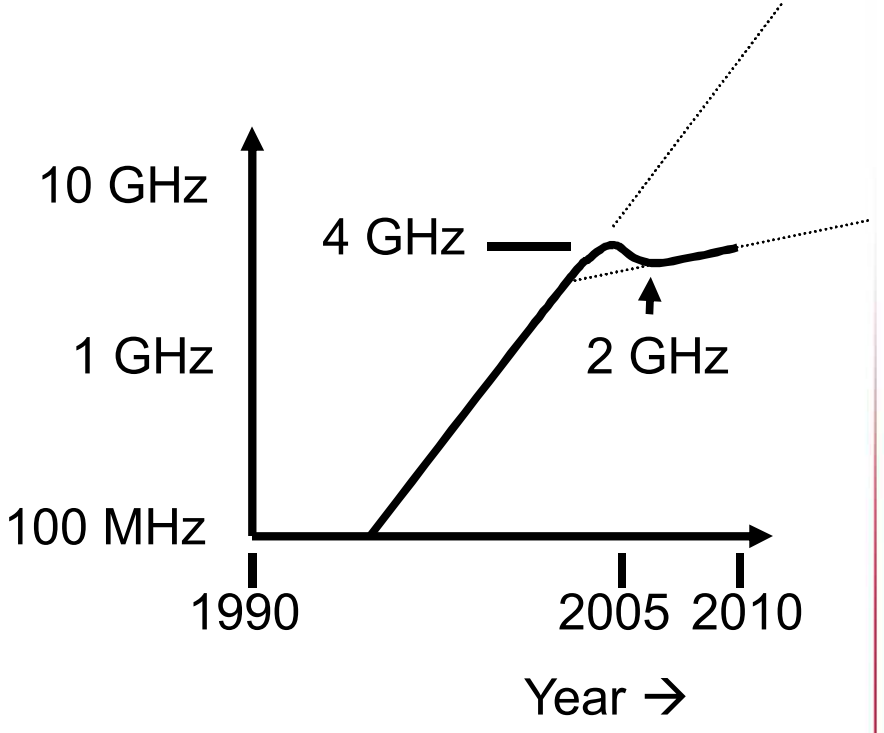
- Q: What will replace development or will it come to a standstill. Nanowires? New materials? Vertical integration?
  - A: CMOS physical evolution will approach an asymptotic limit due to logic power. However, CMOS will be augmented by optical interconnect, nanomemory, …
  - A: Architecture and software advances will raise efficiency of existing devices 10×-100× and will become essential to realizing physical science advances.
  - A: Eventually, a new physical device will emerge and change the game again (quantum computing, etc).
  - A: Industry will diversify to make money ("More than Moore") and marketers will claim whatever actually happens is "Moore's Law" by redefining the term

Forward: Response to "Guidelines & Questions"

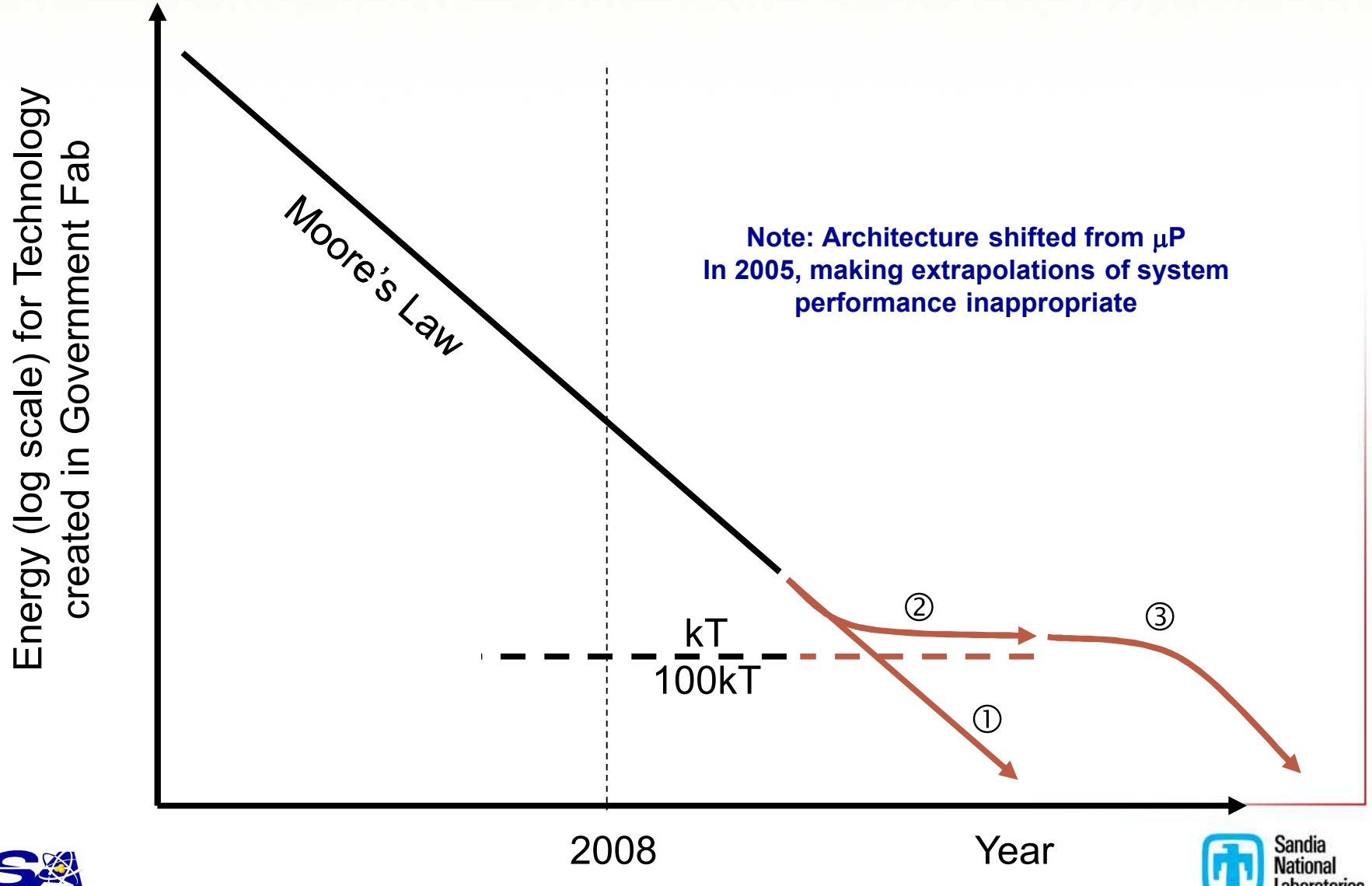
- Q: How long will Moore's Law be sustained?
  - A: Flat lining of clock rate and the shift to multi-core in 2005 violated the original law and caused industry to redefine Moore's Law in 2008. Density increases to 2022+
- Q: What are the most likely technologies to be employed beyond 2020?
  - A: Next phase: CMOS with nanotech enhancements (optical interconnect, nano memory) and alternative architectures.
  - A: Second subsequent phase: A new physical device
- Q: What are the implications of Moore's Law stalling?
  - A: Shift from line width as a driver to device diversification and architecture, with implication that business/Government needs to shift investments to follow the driver

Clock Rate Flat Lined Two Years Ago

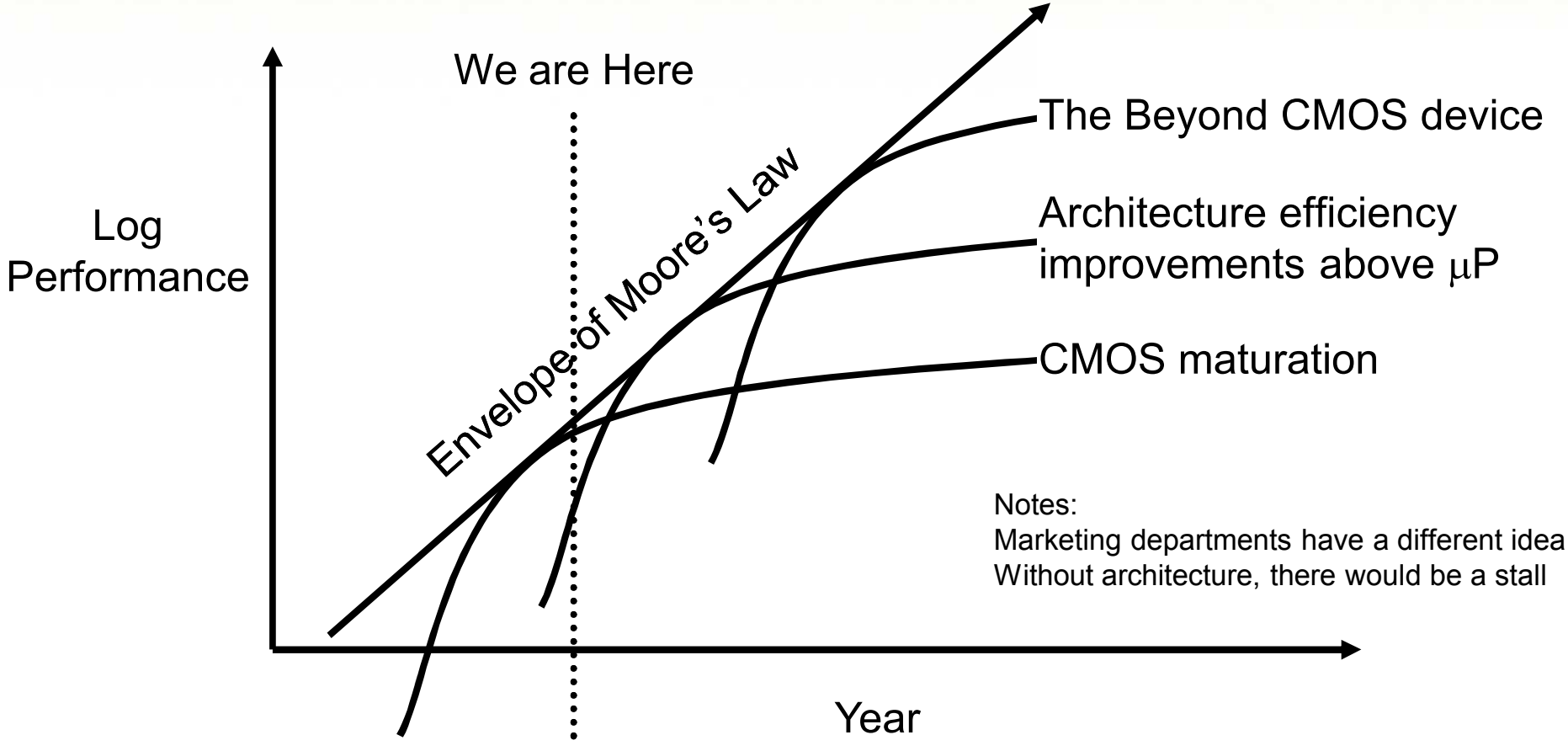
- **Clock rate flat lined two years ago, as vendors put excess resources into multiple cores**
- **This is a historical fact and evident to everybody, so there is little reason to comment on the cause**



Device Power Scenarios for Moore's Law



Candidate Position for the Report on the Information Revolution



Technological Surprise: Device physics will be insufficient to maintain the expectations of Moore's Law in the near to mid-term future

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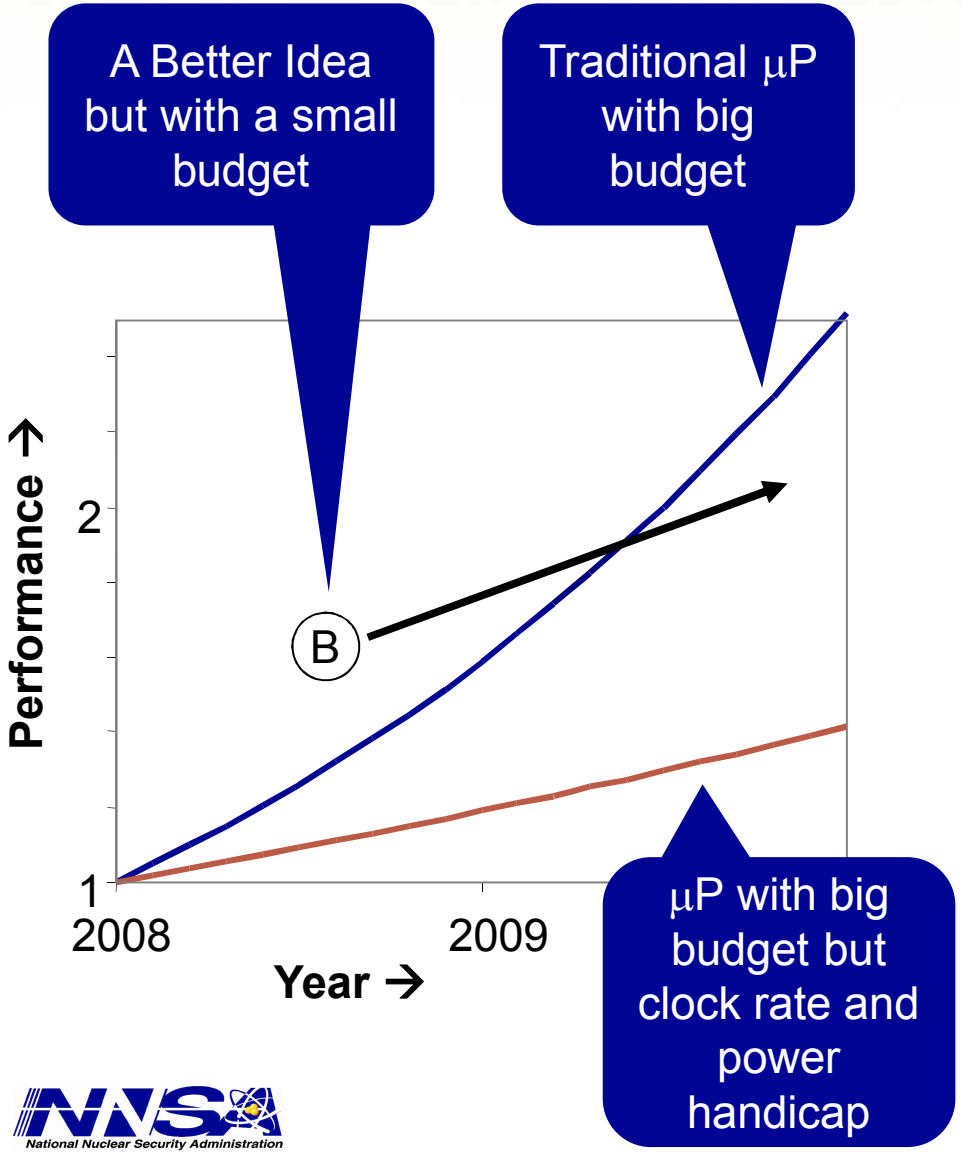
Special Architectures Go Mainstream



- **Conclusions**
  - **Mainstream and embedded technology will become more similar**
    - Power
    - Parallelism
  - **Architectures will become more special purpose**
    - General systems may be comprised of multiple special purpose sections

Special Technology Needs for Government Applications

- **HPC community has R&D needs above what industry will support (Zettaflops 2007)**
  - **High capacity integrated memory**
  - **Intra-chip optical interconnect**

Architecture Summary

- Flat lining clock rates make the μP a weaker competitor, so alternative architectures can rise
- Flat lining clock rate requires more parallelism
- Slowing power scaling requires architectures with a higher ratio of logic supporting the application to overhead
  - Vector, GPU, SIMD, Accelerator, FPGA, ASIC, …

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Pick Successor To CMOS by 12/31/08 ??

- **Below is industry's action item to address the need for "Beyond CMOS"**
- **The technical group expects the answer will be that "option narrowing is premature"**
  - **The meeting will actually be July 11**

The IRC has requested ERD/ERM to begin to narrow options for "Beyond CMOS" technologies. Of the various options for new Beyond CMOS Information processing technologies (including various charge based – SETs, QCA, RTD, etc. - , molecular, spintronics, nanomechanical, etc. we are asked to:

- Recommend one of the major classes as being most promising by no later than Dec. 31, 2008
- Identify one or two devices approaches within the recommended class to pursue with a detailed roadmap with a time line. We will define a process for accomplishing this task by arriving (hopefully) at a consensus with ERD.

Beyond CMOS Technology Candidates

- **The report will include a summary of the device technologies being considered by industry and Government as CMOS successors →**

Candidate "Beyond CMOS" Device Technologies for Information Processing

Device Technology	Advocate Lead	Advocate Team	Counterpoint Lead
Nanoelectromechanical Switch		Karem Akarvardar Tsu-Jae King Adrian Ionescu	
Spin Gain Transistor			Supryo Bandy
Spin Torque RAM	Robert Buhrman	J. Stohr David Awschalom U.-In Chung	
Spin Torque Transfer Oscillator	B. Dieny Andrew D. Kent	D. Houssameddine	
Collective Spin Device	K. Wang		Supryo Bandy
Magnetic QCA	W. Perod or G. Csaba or M. Niemere		
Electronic QCA*	C. Lent		V. Zhirnov
Single Electron Transistor	T. Hiramot		
Atomic Switch Logic	M. Aono		
CMOL and FPNI**	Kostia Likharev		Jim Tour
Molecular Logic	Jim Heath or Francis Stoddard		Jim Tour
Quantum Computation***	D. DiVincenzo or Geordie Rose		

* Electronic QCA – I (Jim H.) do not think this is a viable candidate since the ERD WG eliminated this from our Tables in the 2005 edition of the ERD chapter.

** FPNI – Field Programmable Nanowire Interconnect (see http://www.iop.org/EJ/abstract/0957-4484/18/3/035204)

*** Quantum Computation may be outside the scope of this project. However, this topic was suggested by 2 members of the ERD WG. Their reason to consider this is the possible criticism if we don't include it.

Ratings of Individual Technologies in Report

- Subject to customer guidance, we propose to summarize technology ratings
- The technologies picked for inclusion will follow relevance to Government interest, which is different from industry or academia

Summary of Review of Devices

- Most of the nanotech devices under study are targeting AND-OR-NOT (irreversible) logic. If CMOS reaches the irreversible logic limit, no alternative nanotech device could ever do better than a tie
  - But could have better system performance, be cheaper to manufacture, or be more radiation hard
- To do better than CMOS will require a different paradigm
  - Reversible logic, quantum computing, neural networks, maybe a few others
  - Industry not working on these, except for IBM

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- **Beyond CMOS**
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Government + Industry Computing Model Categories for Beyond CMOS

Name	Data Representation	Program Representation	Information processing	Performance (e. g. factor n-bit number)
Incumbent				
Boolean logic computer	0, 1	Gate wiring, software	AND-OR-NOT Logic gate	$e^{n^{1/3}}$
Reversible logic computer	0, 1	Gate wiring, software	Toffoli or Reversible gate	No power, $e^{n^{1/3}}$ time
Quantum computer	Quantum State Vector	Unitary rotation	Rotate and measure	n^3 power, n^3 time
Analog computer	V(t) voltage signal	filter	Filter signal input→output	n/a
Neural network	Neuron firing	Synapse weights	Recognize Pattern (Hopfield)	n/a

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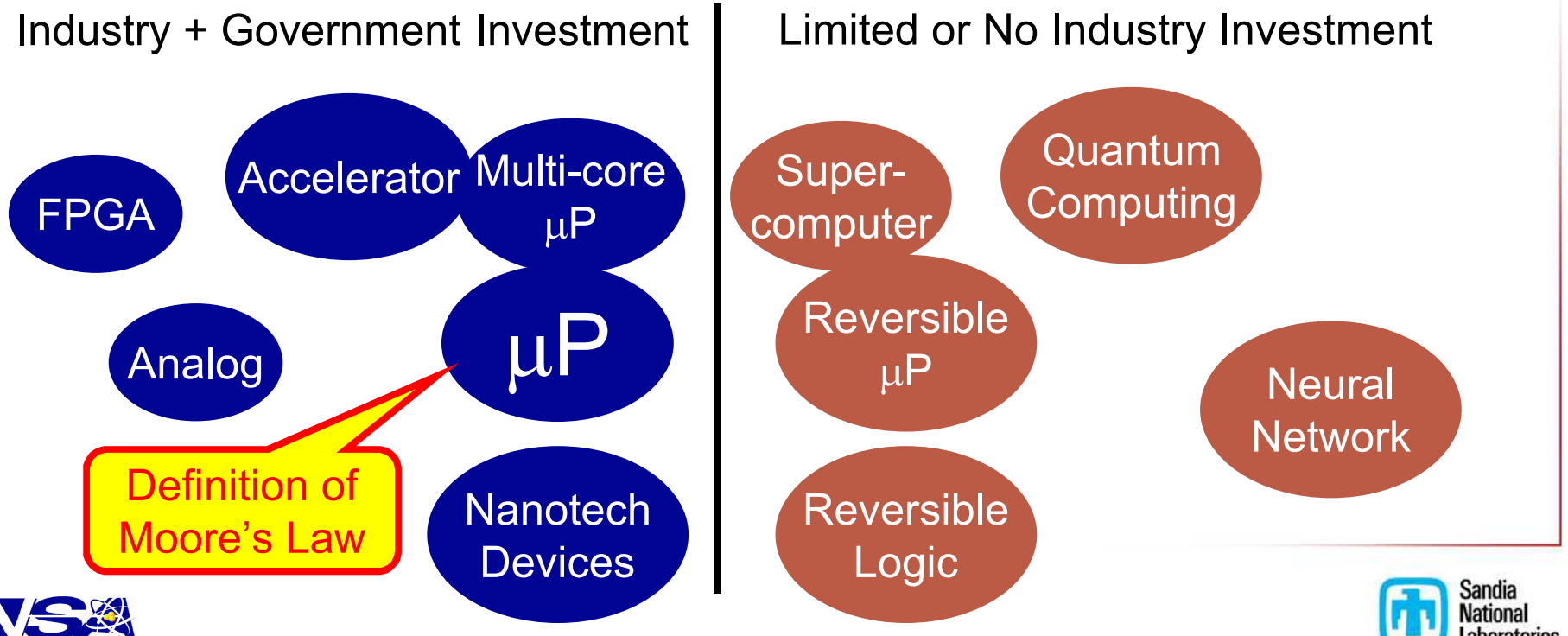
Government-Industry Roles

- **In general, industry is investing heavily in technologies that can reach the CMOS limit**
- **Technologies that can beat CMOS significantly are primarily Government investments, if any**



Radiation Hardening

- Emerging memory and logic technology enhancements vary widely in radiation hardness
- The study will address possible combinations of devices that could create a rad-hard computer with reasonable performance

Trust Issues
Foundry and Supply Chain

- As the action shifts away from decreasing line width, the US Government will be better able to support one expensive foundry
  - it's lifetime will be longer, so the amortized cost will be lower
- If military advantage shift proportionally to architecture, many architectures can be implemented on a single foundry

Other Government Issues

- **To be discussed verbally**

Conclusions

- Multi-core is the first example of an undesired architecture shift caused by the approaching end of CMOS scaling. The architecture shifts will get more profound until device scaling is irrelevant
- To harness the remainder of Moore's Law will require changes in architecture and software to pace changes in devices
- A new era of computing could emerge based on a different information processing principle, but this will require a discovery
- Industry is only exploring a subset of the options

Backup

Downselect Criteria

Basic description	This section comprises a description of the proposed device family. The section may include textual and graphical descriptions but should be independent of (or parameterized by) feature size F	
Principle of Operation	Control mechanism	*Thermal injection over gate barrirer*
	Operating temperature	*Usually 25C - 125C*
Materials and Geometry	Base	*Si*
	Device Architecture	*FET*
	Patterning	*Lithography*
	Design	*2D layout*
	Circuit element	*Transistor, 3 or 4 terminal*
	Device density as a function of feature size F	*~ 1/F^2*
	Size in units of feature size F of a gate equivalent to a 2-input NAND gate, including contacts and isolation and necessary peripheral circuitry	*>~65 F^2*
State variables and control	State variable	*Voltage*
	Number of logic states	*2 (high and low)*
Logic Family	Information processing basis	*Universal set comprising NAND, NOR, NOT logic gates, also pass gates*
	Interconnects	*Wire*
	Compatible memory	*SRAM (fast) , DRAM (dense)*
	Clock	*CMOS based clock circuits*
	CMOS compatible	*N/A*

Downselect Criteria

Limitations	This section comprises a list of known limiting factors for performance and manufacturing	
Materials and Geometry	Sources of variability	*LER, Doping fluctuations ~ 1/SQRT (LW)*
	External parasitics	*Access resistance, fringe capacitance*
State variables and control	Noise margin	*(Vdd-Vth)/ KT/q > 5*
	QM limit	*Tuneling: Band to Band, Source-to-Drain*

Performance Potential	This section comprises an extrapolation of the technology to about the year 2020, stipulating F=14 nm. Provide best estimate numerical values.	
Switching speed and energy	Intrinsic speed of single element	*Lchan/v ~ 0.1ps*
	Self Gain	*gm/gd ~ Vdd/DIBL*
	Proposed clock rate	*xxx*
	Switching Energy per gate or gate equivalent @ proposed clock rate	*0.5*Cload*Vdd^2*
	Static Power Dissipation per gate or gate equivalent	*Vdd*Ioff*(2/5)*
Interconnect	Interconnect delay per micron	*RC*
	Interconnect energy as a function of distance at proposed clock rate	*CV^2*