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Highly Pixelated Hypertemporal Sensors for Global Awareness

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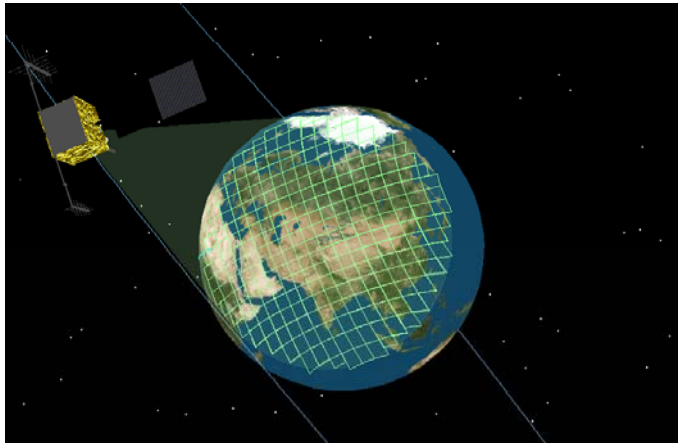
Grand Challenge Vision

"See everything, everywhere, always, and do it fast"

Develop new focal plane array (FPA) architectures and key enabling technologies in preparation for the future production of advanced very large, high pixel count, very high sample rate FPAs for full-earth persistent monitoring, fast event detection and national security missions.

Emphasis on preserving transient information of interest while suppressing an enormous volume of background data



Sandia's remote sensing systems are not used for imaging, but rather for transient signal detection, recording, and processing

Program Goals

Program goal was not to realize a fully functional focal plane array. Rather the program goal was to develop critical enabling technologies to accelerate the realization of future state-of-the art FPAs in advance of a specific mission applications.

- **Packaging and Assembly**
  - Demonstration of 2- & 3-layer (with through-wafer via) daisy chain structures
  - Size compatible with 2K x 2K 30-µm pitch FPA
    - 4 x4 array of 15.36-mm signal processing stacks
    - Layer-layer interconnect density compatible with FPA
  - Demonstration of passives, optoelectronics, and next assembly integration
- **Silicon Circuits**
  - Design, fabrication and test of “flat” signal processing concept
  - Demonstration of extensible 3D design concept
- **High-speed Data Interconnects**
  - Low-temperature VCSEL fabrication, test, reliability assessment
  - Next assembly integration design and fabrication
  - Transmitter / Receiver prototype demo
- **System Modeling and Analysis**
  - Mission analysis and full-system modeling tools in place
    - Background, clutter, target simulation

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HTS Technology Development: Coupled, Parallel Paths

System Design

Circuit Architecture

Packaging Technology

Optoelectronics

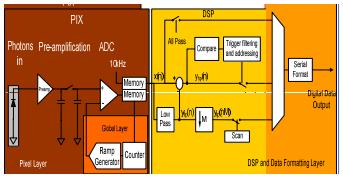
Spreadsheet System Modeling

Technology Review & Analysis

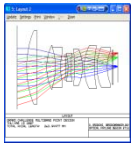
MIT/LL 3D Chip

FPA Specs

Architecture Synthesis



Optics Feasibility

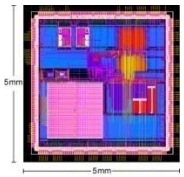


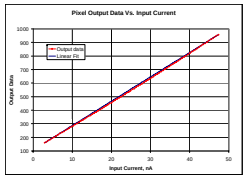
HTSP (2D) Design, Fab, & Test

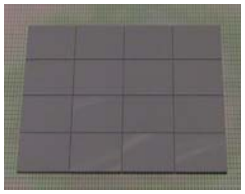
Phase 1 Demo

VCSEL Device Design

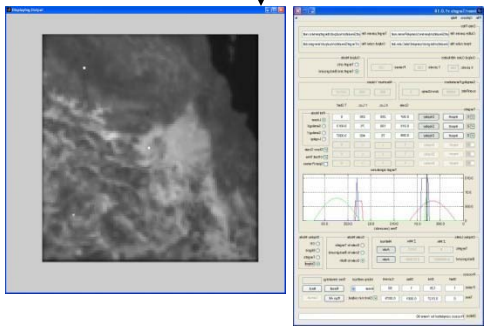
Detailed System Modeling







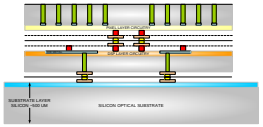
XMIT/RCV Demo

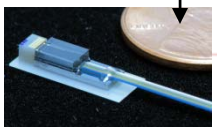


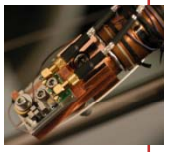
Phase 2 (3D) Design, Fab, & Test

Phase 2 Demo

PKG Dev







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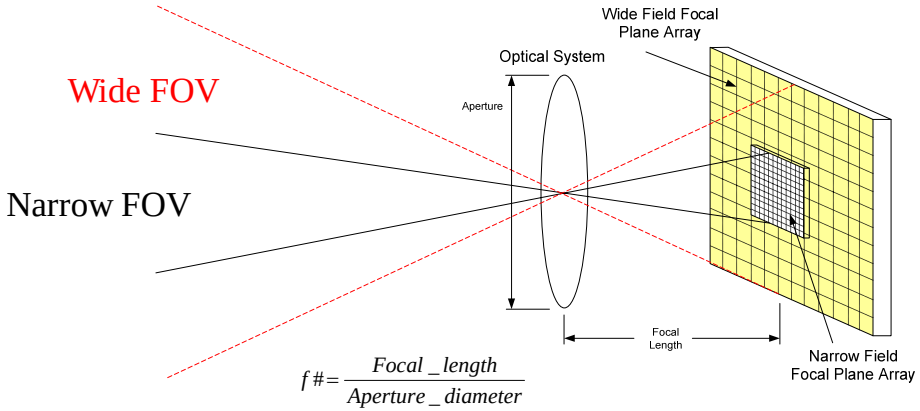
Problem

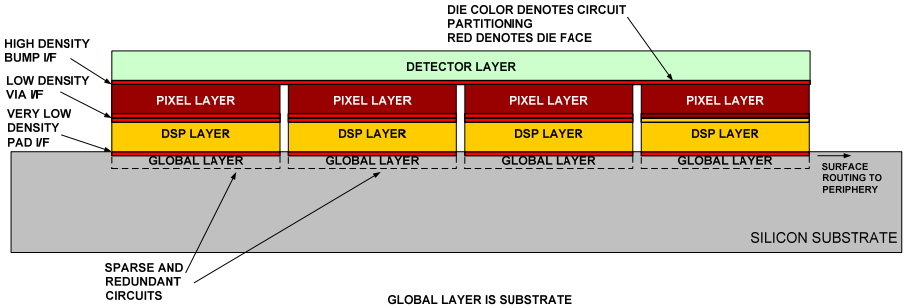
Why are Large FPAs Important?

$$fpa\_size \approx Aperture\_diameter * f\#*FOV(rad)$$

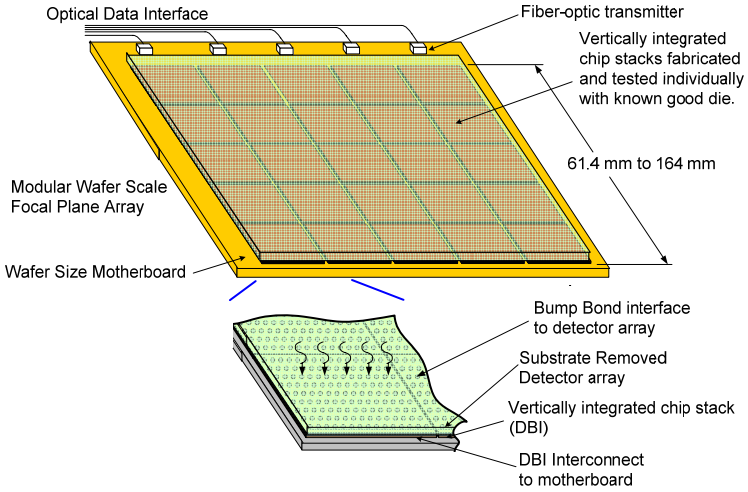


$$f\# = \frac{Focal\_length}{Aperture\_diameter}$$

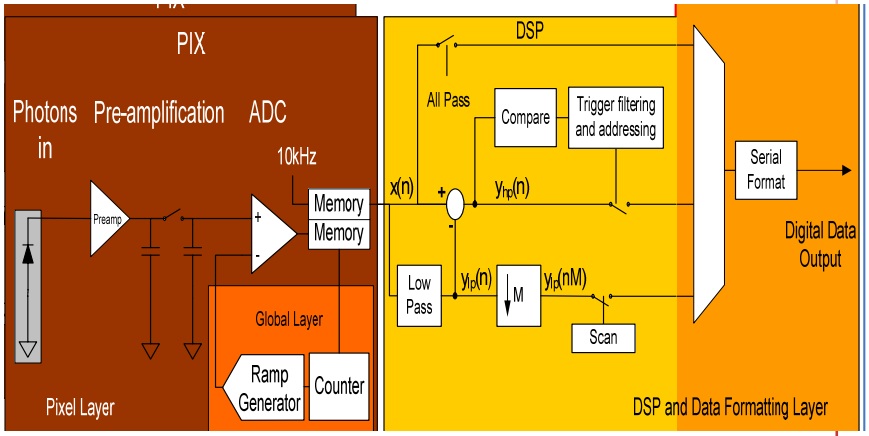
3D Packaging



Tiled Scalable Architecture



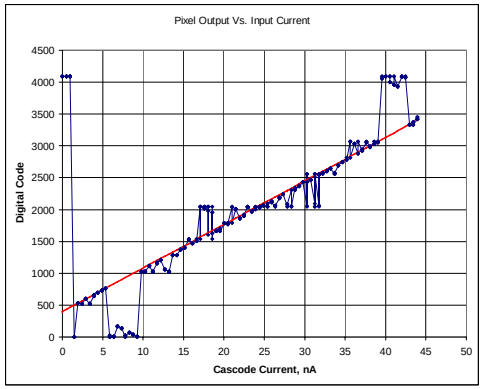
3D Circuits

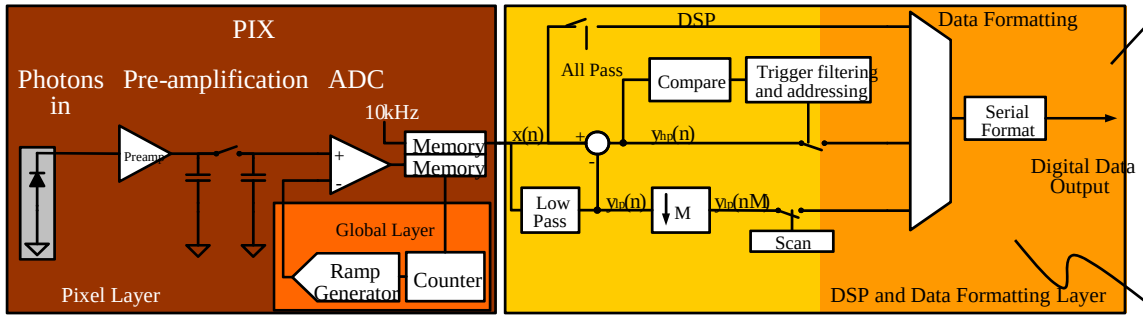


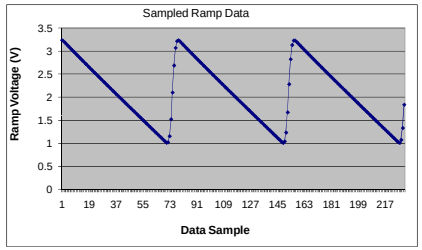
Silicon Circuits Success

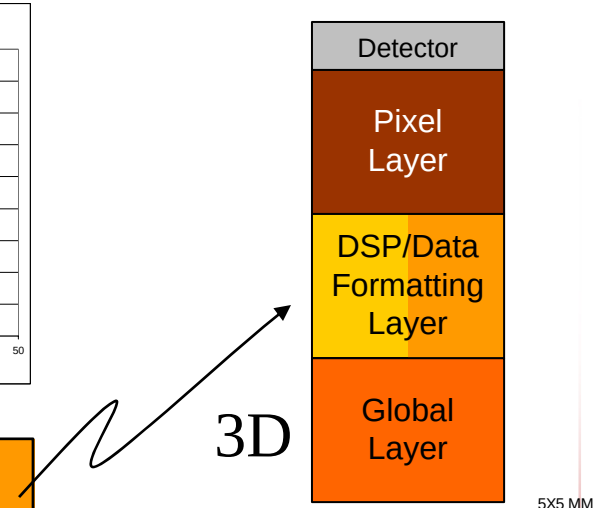
- 1st pass operation
- Demonstrated operation
- Top-down system design
- Built-in test capability

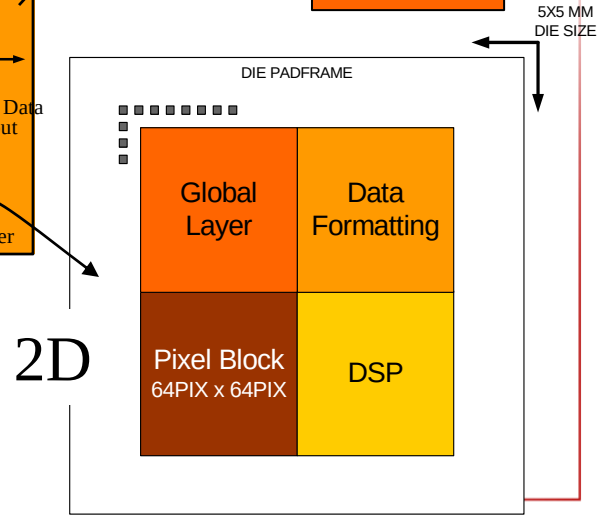
  Enabled root cause resolution and detailed performance evaluation











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Opto Interface Success

Sandia 200 K-optimized VCSEL's designed and demonstrated

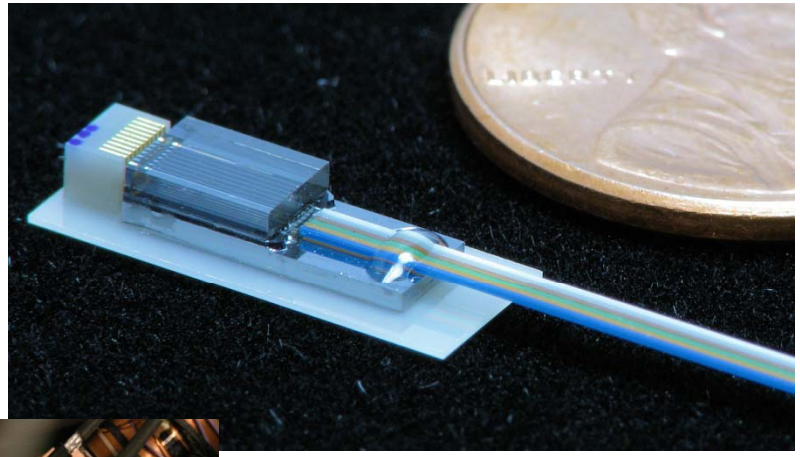
Custom low-power driver/MUX IC designed and delivered by Horowitz group from Stanford University

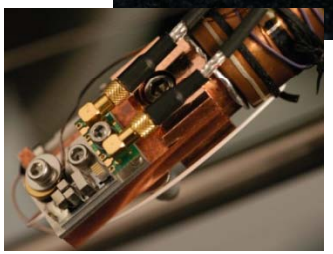
MUX/driver function demonstrated at **~4.5mW/ch at 3Gb/s**

With shared PLL (~30mW) and VCO (~10mW) and 10mW for VCSEL's estimate **power consumption for 4-ch 12Gb/s transmitter at ~70mW.**

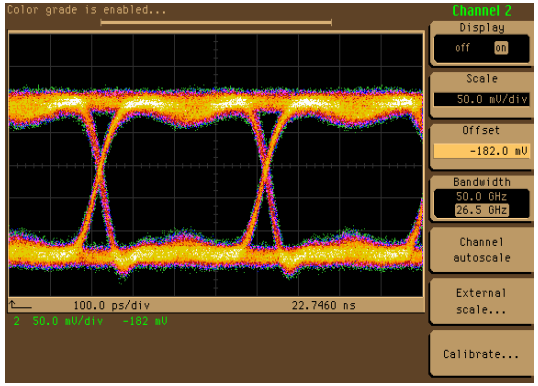
Power consumption reduced by factor of >30 compared to COTS components (2.36W at 3Gb/s)

Optoslim optical package developed and demonstrated
Small footprint, rugged, no optical feedback/crosstalk

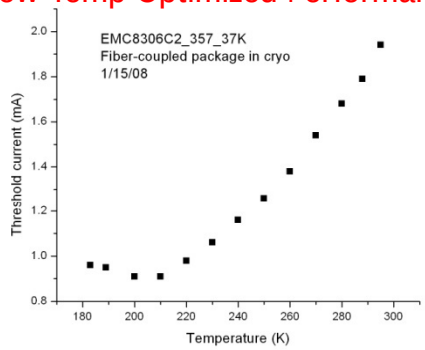


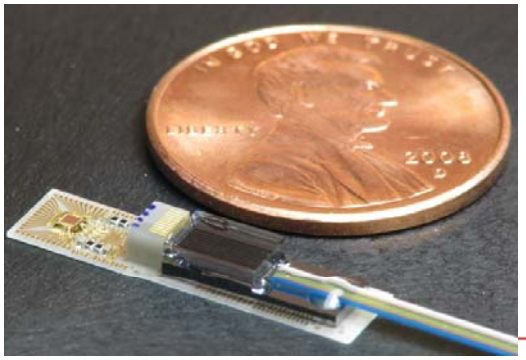


Optical, T=200K , I=3.3mA
DATA, BR=2.48832Gb/s, 500mV_p-p



Low Temp Optimized Performance





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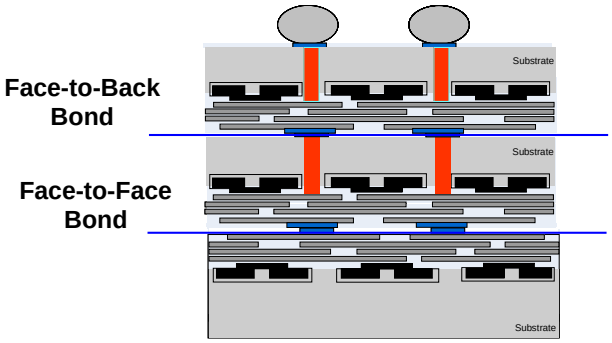
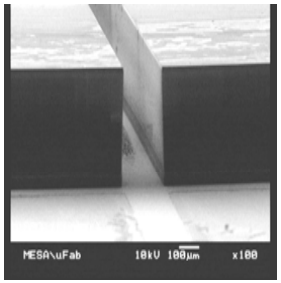
Packaging Success

Provides clear enabling advantages:

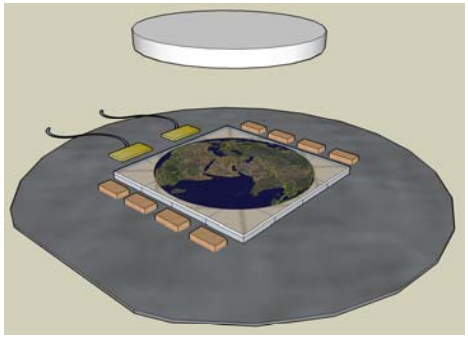
1. Ability to fabricate large FPAs
2. Increased yields over traditional reticule stitching techniques
3. Enables development of innovative advanced pixel and FPA architectures
4. Applicable to other microelectronic circuits



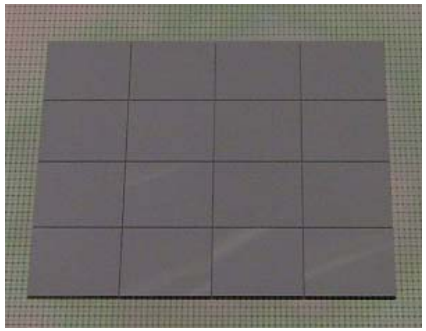
3D Silicon integrated circuit stacking & Bulk Si through–wafer vias



Precision Silicon Die Singulation



Scalable FPA Architecture

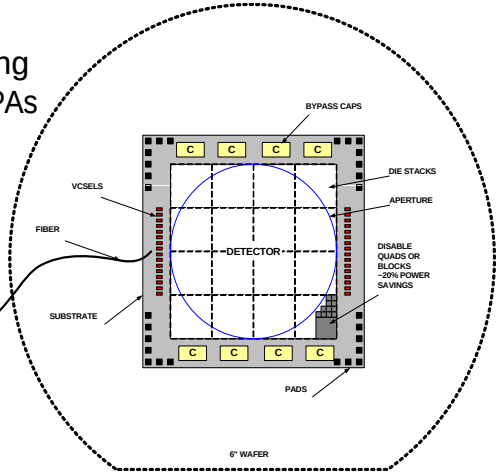


4 Side Buttable with Sub-pixel Gaps

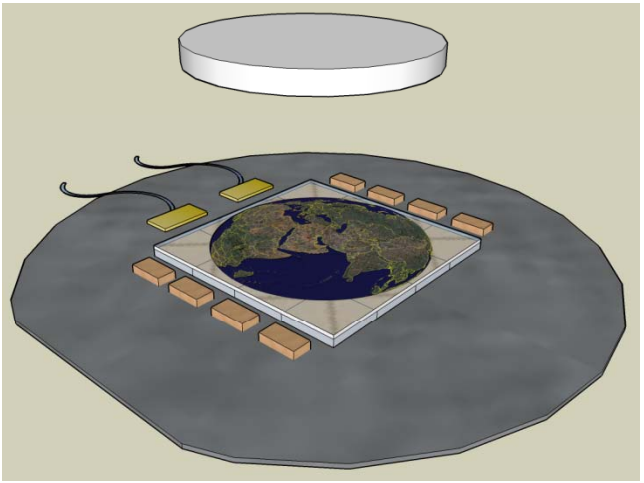
Impact

HTS Focal Plane Concept - Technologies developed on this Grand Challenge are key to realizing future FPAs for the most challenging national security remote sensing missions.

Scalable packaging enabling large FPAs

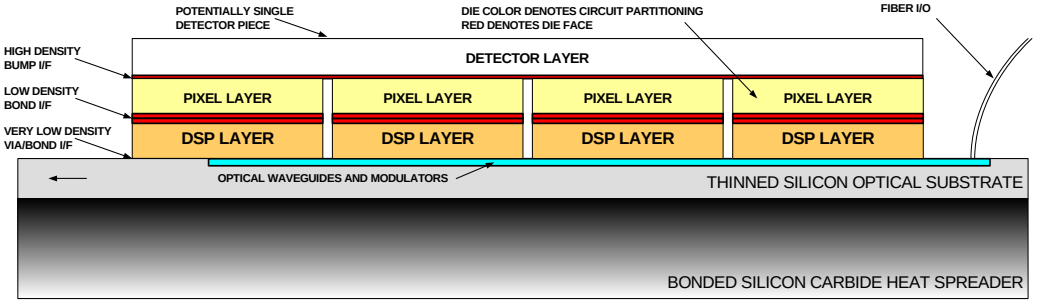


Low-temperature operation fiber interfaces moving Terapixels per second of data



Direct impact and performance improvements in many diverse mission areas

Low power advanced 3D circuit architectures



Reduced size, weight & power