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Si Spin Quantum Computation in MOSFETs

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Double Quantum Dot Team Members

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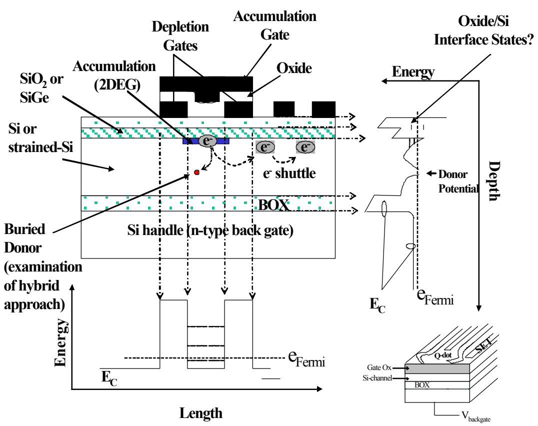
Quantum Information Science and Technology Grand Challenge

QIST Quantum Information S&T

Silicon Qubit Hardware



Qubit Gates & Lay-out

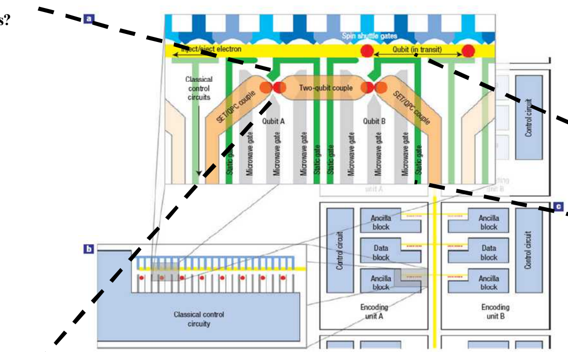
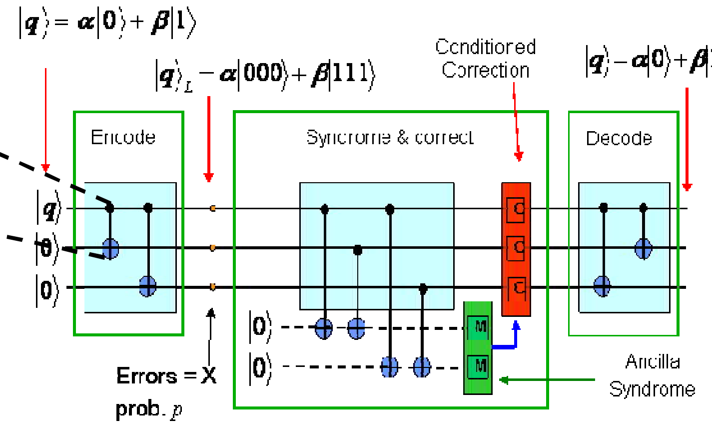


Figure 2 Architecture proposed by Taylor et al., Nature 2005. Silicon based DQDs and QPCs would replace the proposed GaAs devices. Donors are proposed as a supplement to enhance the architecture in this work.

Error Corrected Logical Qubit



- *Primary goal: demonstrate feasibility of silicon qubits at silicon/insulator interface*
  - GaAs has demonstrated that qubits may be formed in semiconductors
  - Silicon is appealing because of promise of long T_2
  - The dominating doubt about Si QC is the qubit existence proof
- *Grand Challenge => develop silicon qubit hardware and plans to extend physical qubits to a logical qubit*

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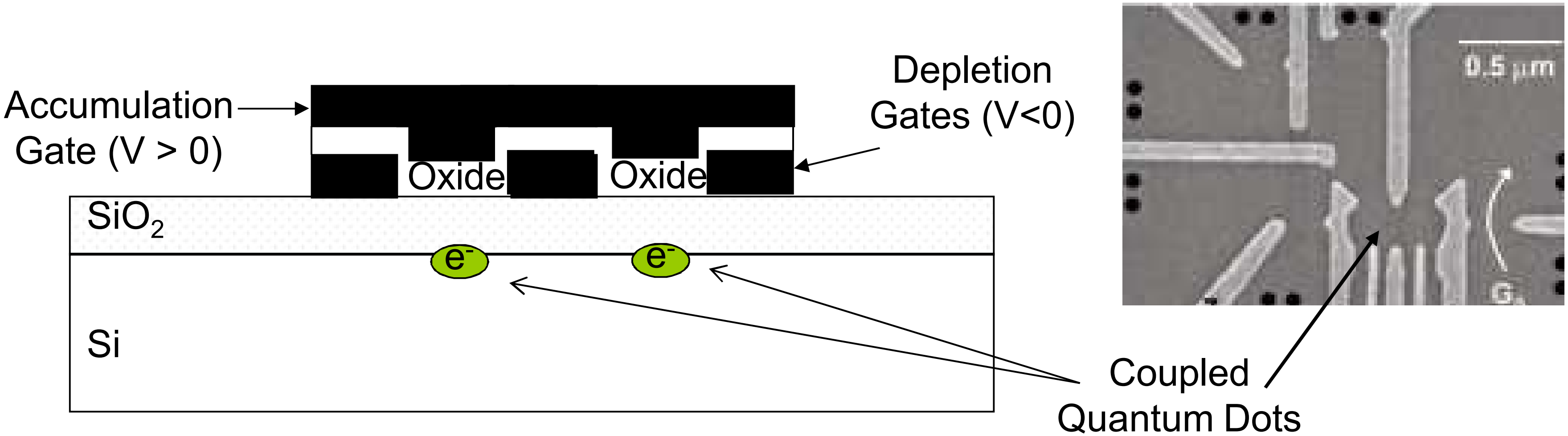
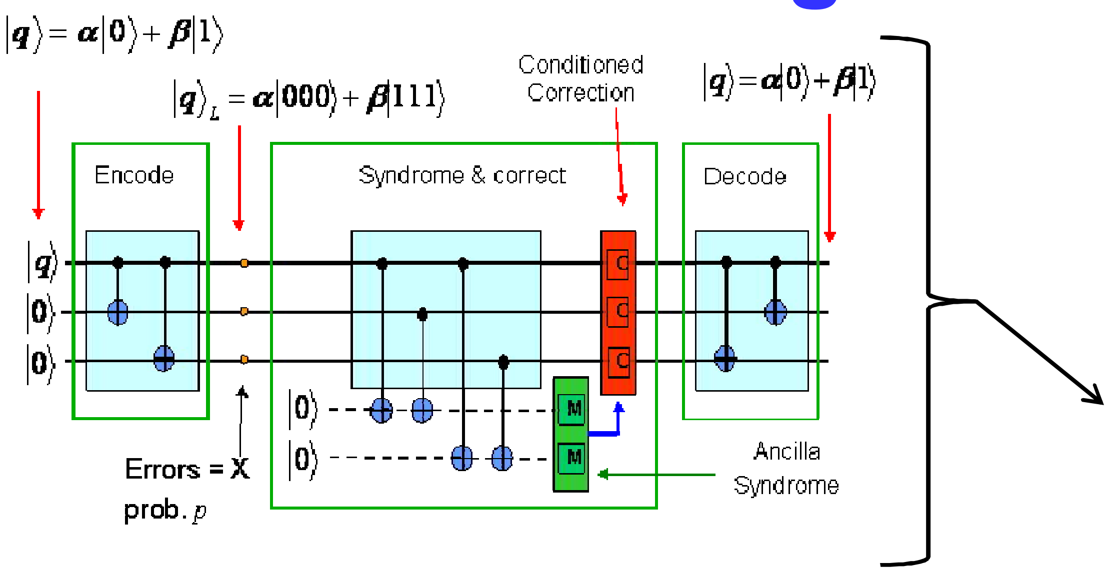
Technical Challenge (1): Si Qubit!

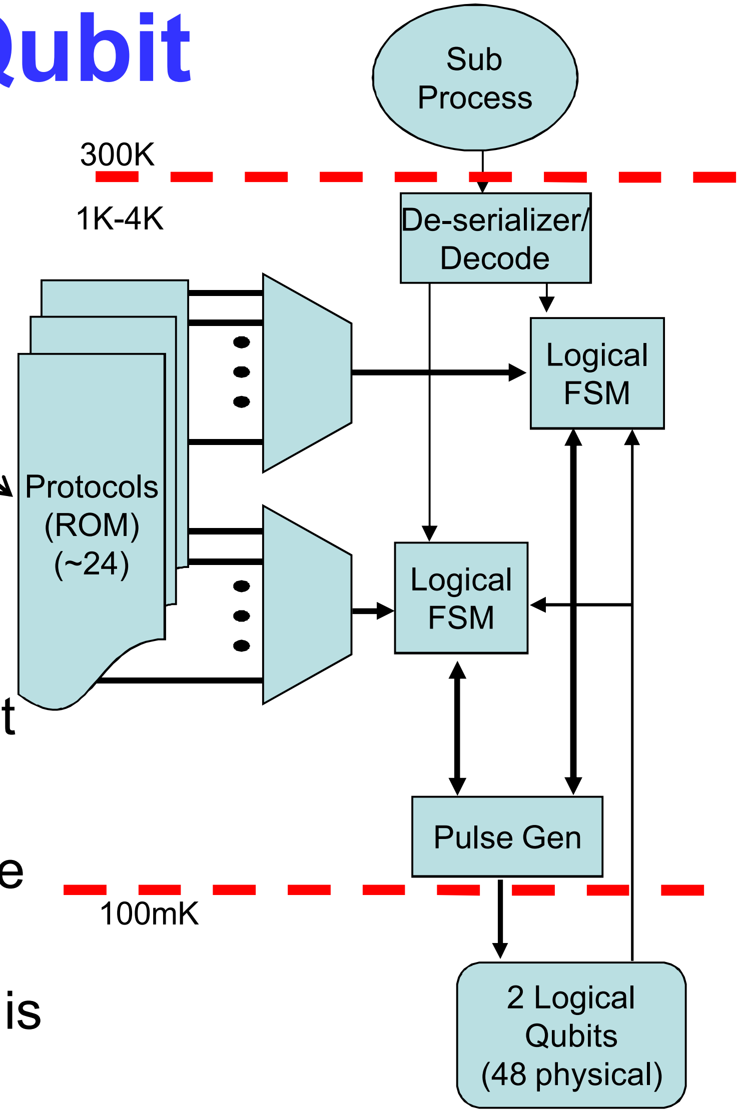
J. Petta, et al., Science



- Pauli-blockade recently demonstrated in SiGe/sSi and UTB-SOI (i.e., MOS)
- Our approach: pursue surface Si MOS-DQD
  - Compatible with ^{28}Si epitaxy => long T_2
  - Charge stability demonstrated with MOS system [e.g., Zimmerman et al.]
  - Gates very close to 2DEG => smaller dots than modulation doped case
  - Possible drop-in with SNL CMOS process flow (e.g., fast, low noise sense)
  - Pathways to adopt SiGe/sSi or donors through 2nd generation structures

Technical Challenge (2) : Logical Qubit





- Goal: <u>DESIGN</u> an error corrected logical qubit
- Challenge:
  - Design error correction for which hardware can achieve $p_{threshold}$
  - AND for which classical circuit realization is possible in cryostat
    - Costs: power, bandwidth, density, etc.

Grand Challenge Organization

- Electrostatic gated double quantum dots
- Donor / dot coupling
- Theory and modeling
- Architecture issues
- CMOS devices for quantum computing

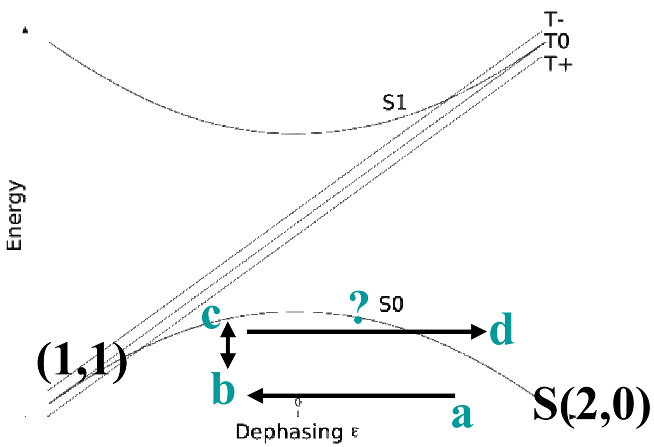
Outline

- 2DEGs in MOSFETs
- Nanoelectronics
  - Quantum dots
  - Disorder and fabrication
  - Quantum point contacts
- Silicon devices – fast detection

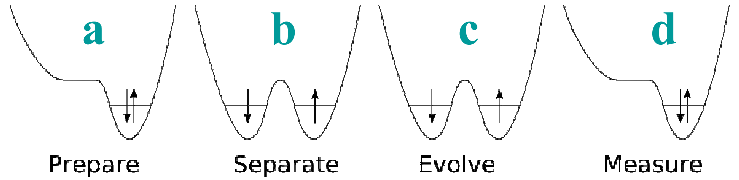
Double Quantum Dot Qubit

Petta et al., Science 2005

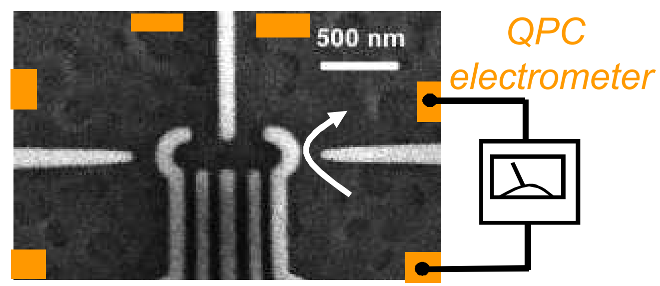
Energy levels



Electron sequence



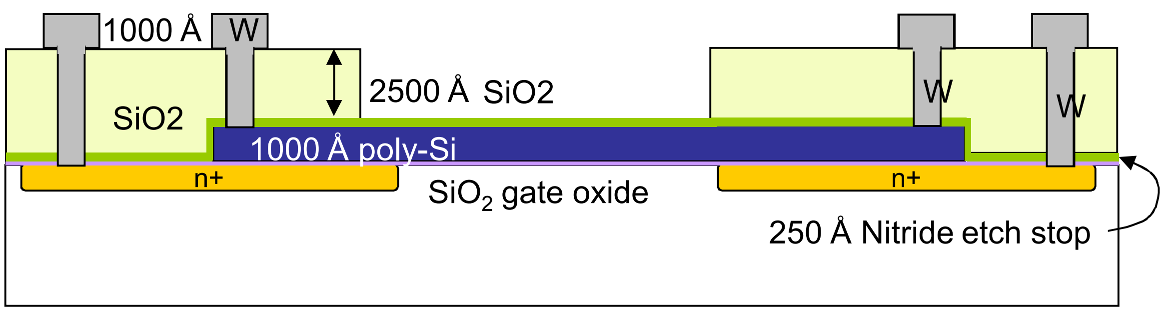
Electrometry



- GaAs community showed a singlet-triplet DQD qubit in 2005
- Our approach will focus on Si MIS-DQD version of GaAs work
  - Collaboration with U. of Wisconsin on this topic
- The state is detected through single charge electrometry
- Quantum point contacts are the initial choice for electrometry

MOSFET Process Flow

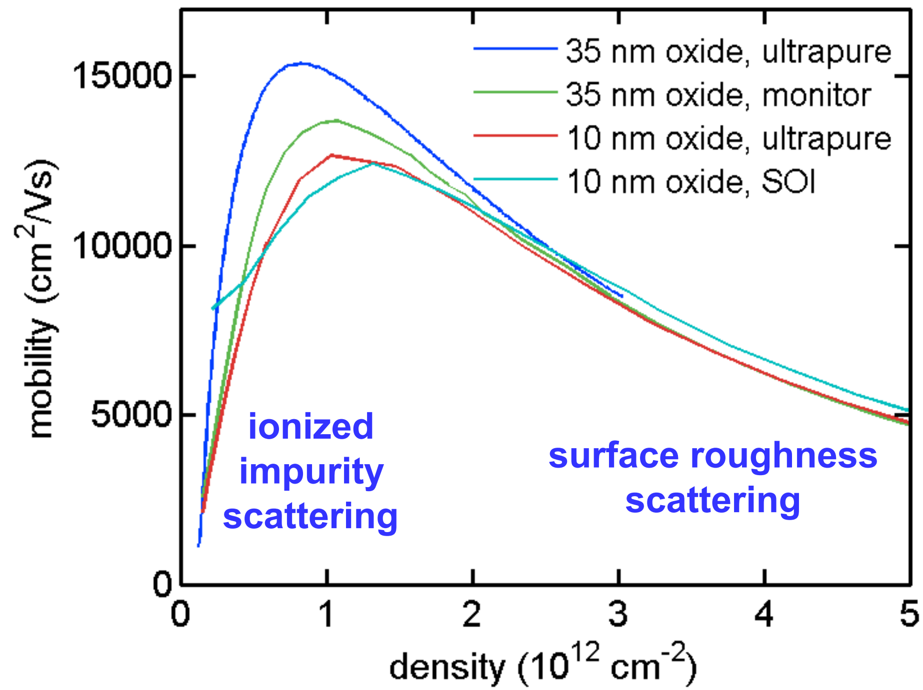
- Silicon or Silicon on Insulator (SOI) Wafer
- Gate Oxide Grown
- Source-Drain Lines Implanted
- Poly-silicon Deposited, Doped, and Patterned
- Contacts and Vias Formed



- Many devices can be fabricated on the 6” wafers
- Linewidth ~ 180 nm → Additional nanolithography steps are required for making quantum dots

MOSFET Two-Dimensional Electron Gas

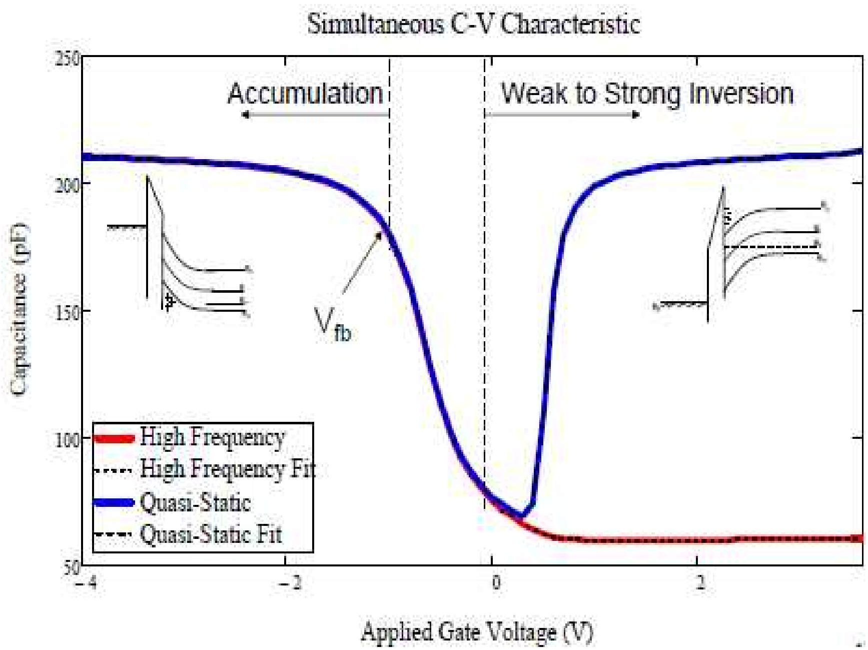
- Mobility is high for thin oxides.
- Peak mobility varies by 20%, but real gains in cleanliness occur for threshold and low electron density.
- Short-loops in the silicon fab improved mobility and low temperature characteristics (i.e. no DCE in oxide growth furnace)
- Additional improvements are possible, however we will focus on maintaining this mobility throughout the backend processing.

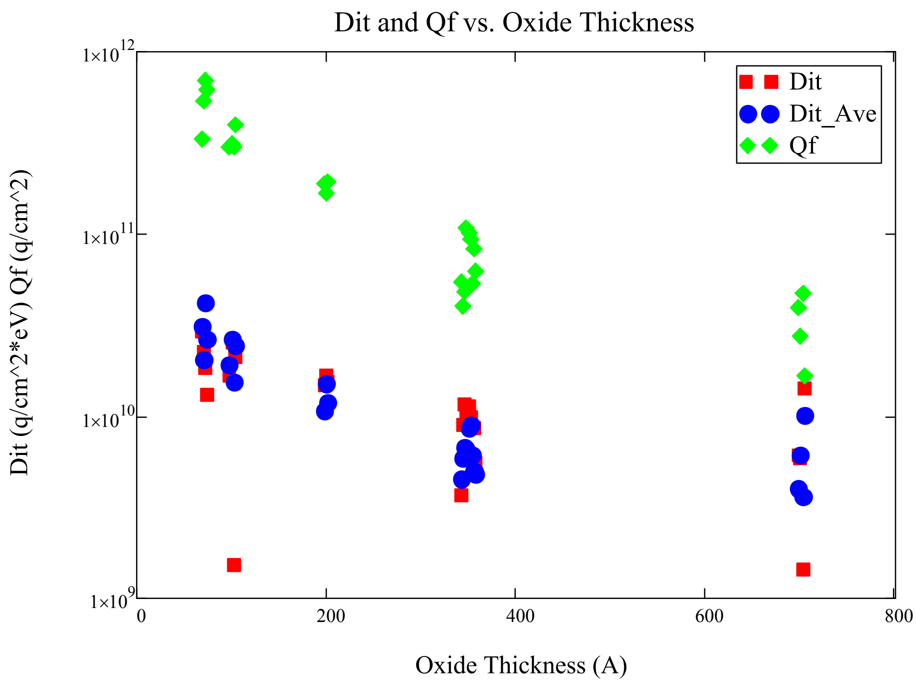


Quantum dots in silicon

S. Angus, Nanoletters ***7****, 2051 (2007).*
A. Fujiwara, APL ***88****, 053121 (2006).*
J. Gorman, et al., PRL ***95****, 090502 (2005).*
D. Abush-Magder, Physica E ***6****, 382 (2000).*

SiO_2 Interface





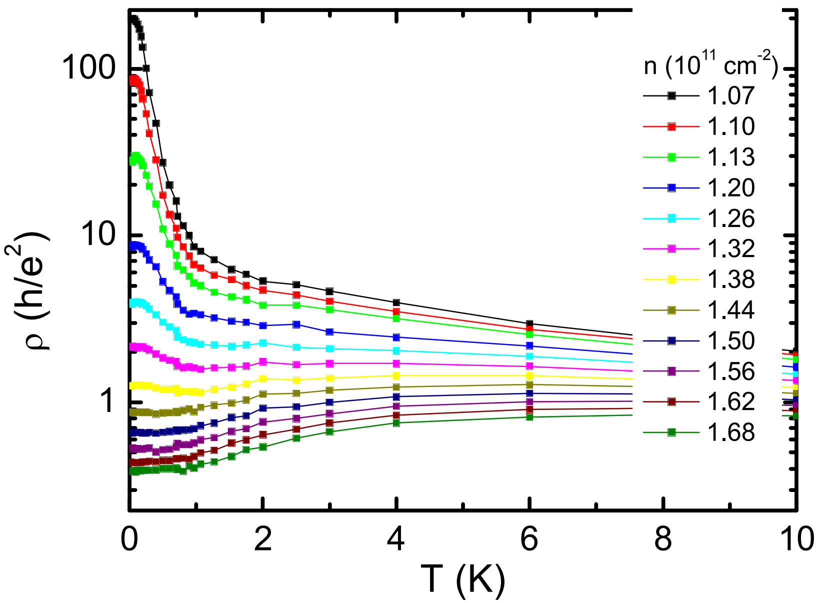
Dit and Qf are of concern for qubits at silicon / silicon oxide interface

Dit not significantly different from ionized impurity density from theory

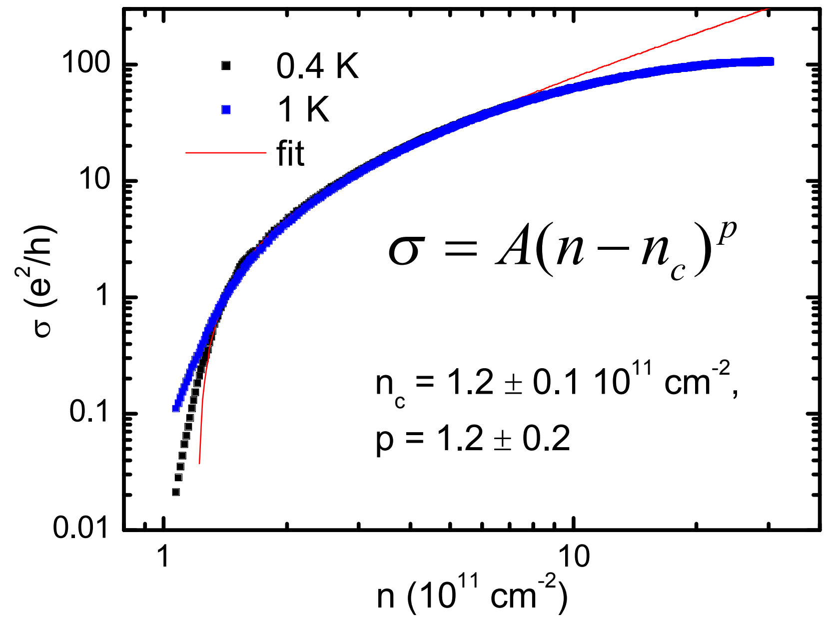
Dit increase for thin oxides – one of many tradeoffs

Electrical Transport at Threshold: 2D Metal-Insulator Transition

Metal-Insulator Transition



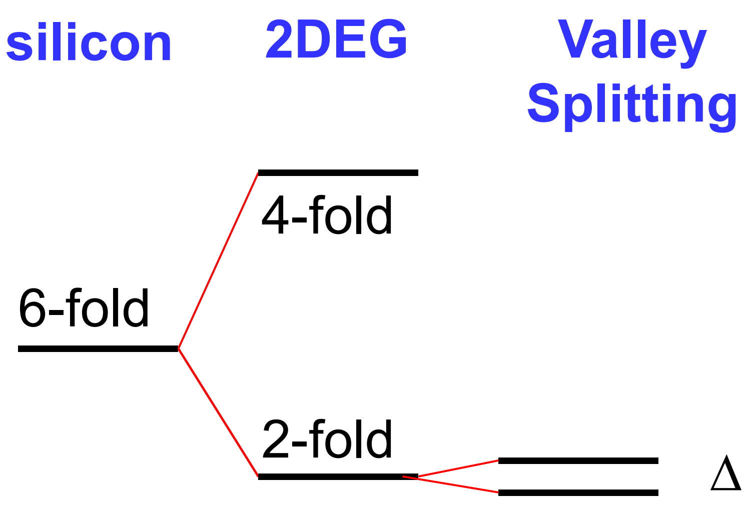
Percolation in 2D

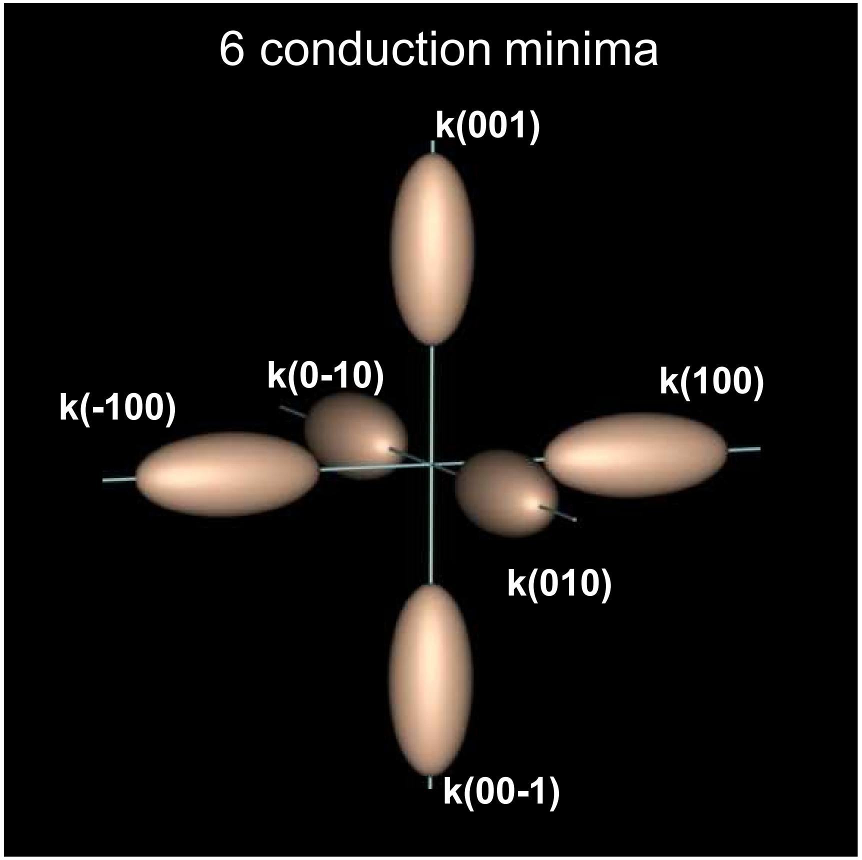


- Low density regime is dominated by ionized impurity scattering.
- Detailed understanding of transport near threshold provides a very good window to issues of disorder and localization.
- Understanding MOSFET threshold at low temperature is a very important issue for SPICE modeling of CMOS circuits.

Valley Splitting in a Si-MOSFET

Valley degeneracy → decoherence





see poster by L. Tracy

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Silicon 2DEG Magnetoresistance

Cyclotron

$$E_c = \hbar\omega_c = \hbar\frac{eB_\perp}{m^*}$$

=7.17K/T

Zeeman

$$E_{Zeeman} = g\mu_B B_{total}$$

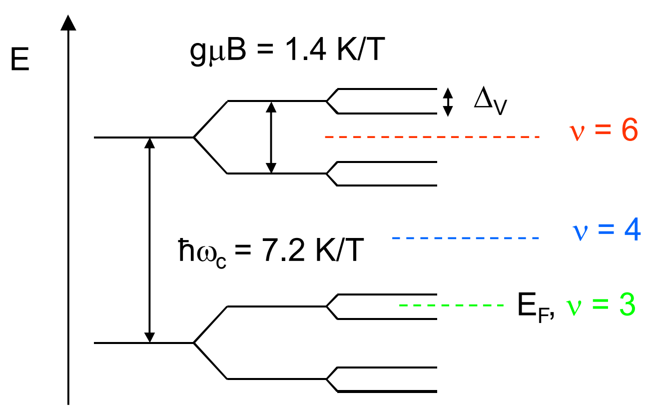
=1.36K/T

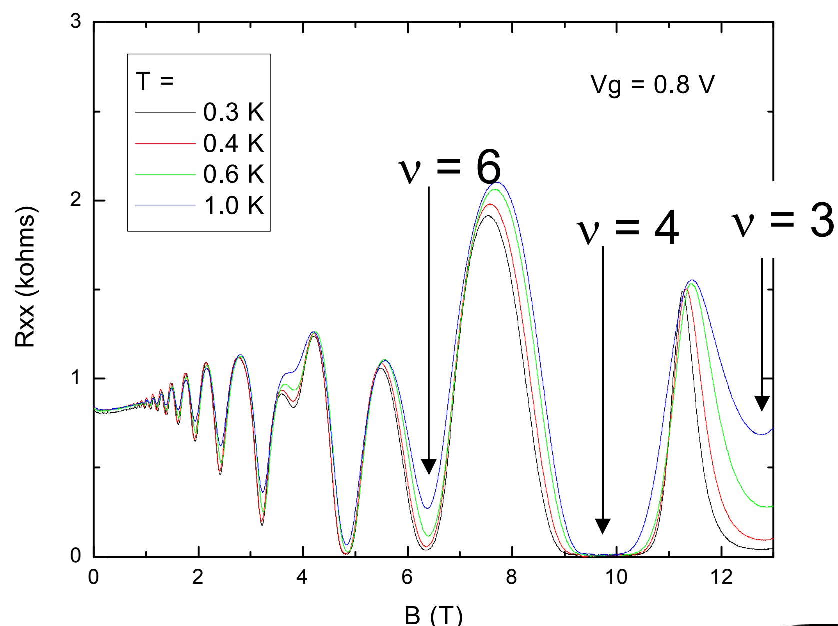
Valley splitting

$$E_V = \Delta_V(B)$$

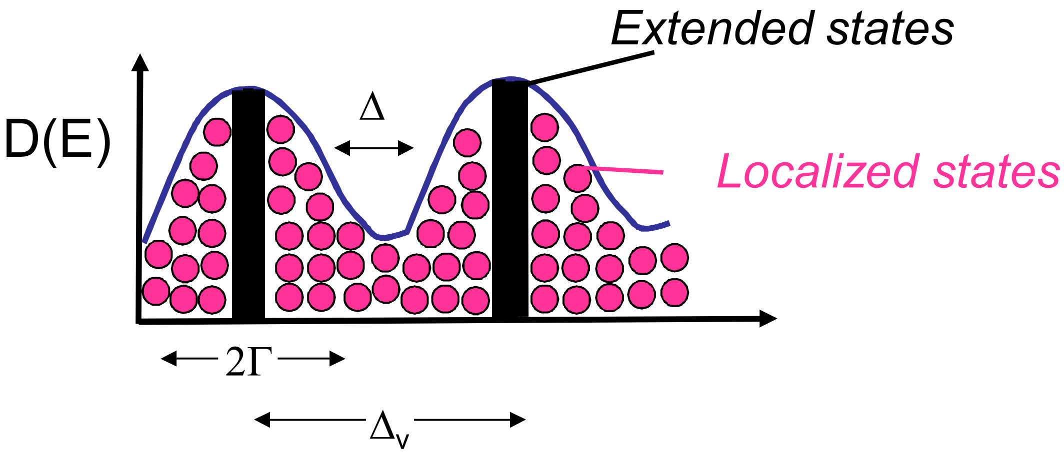
= ?

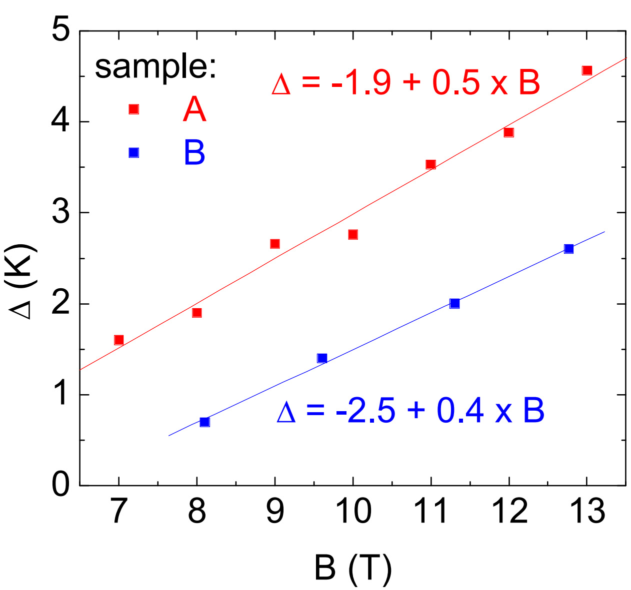
(*Assumed g* =2 and m* =0.19m_o*)





Activation of Quantum Hall States





From low B-field SdH data:

$\Gamma \sim$

A: 4.3 K

B: 4.6 K

At $\nu = 3$

$\Delta = \Delta_\nu - 2\Gamma$, then:

$\Delta_\nu^A = 6.7$ K

$\Delta_\nu^B = 6.7$ K

→ extrapolation to B = 0 is not ideal

→ nanostructure measurements of Δ_ν are better for DQDs

(S. Goswami et al., Nat. Phys. 2006)

Valley splitting in nanostructures

- SiGe work identifies a reduced valley splitting in 2D; one explanation is due to steps from wafer mis-cut
- Shrinking sizes with either magnetic fields or confined sizes leads to valley splitting closer to (or slightly larger than) the theoretically expected value for a "perfect" interface.
- Role of disorder at Si / SiO_2 interface is a question of current interest.

Our experiments beyond quantum Hall studies:

- Electrically detected valley resonance with microwaves – unsuccessful (needle in a haystack)
- Magnetic depopulation in quantum point contact – experiments underway

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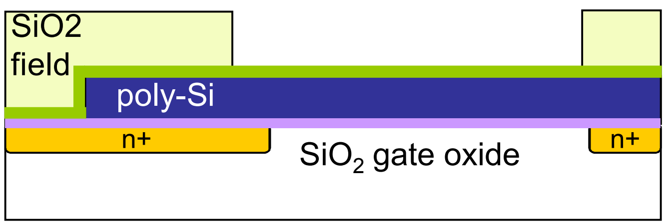
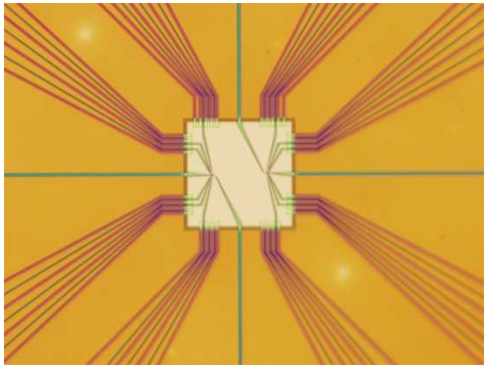
Nanolithography

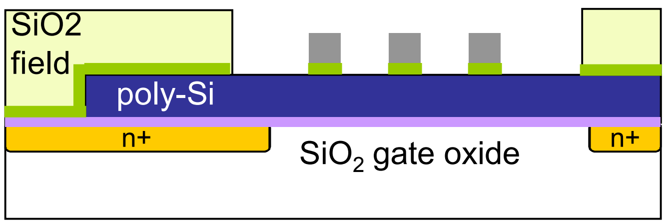


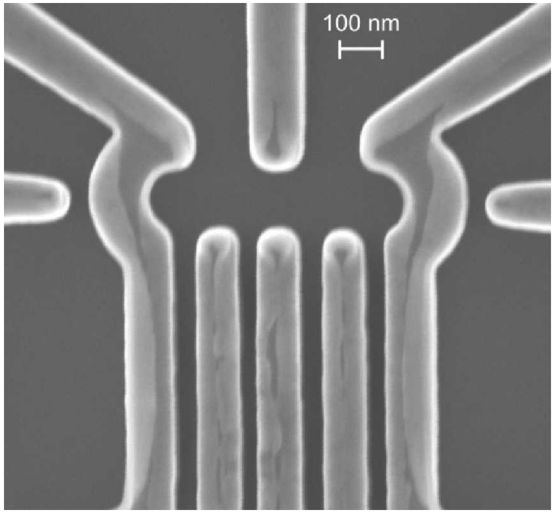


- Variation of the CINT electrical transport discovery platform

Nanolithography

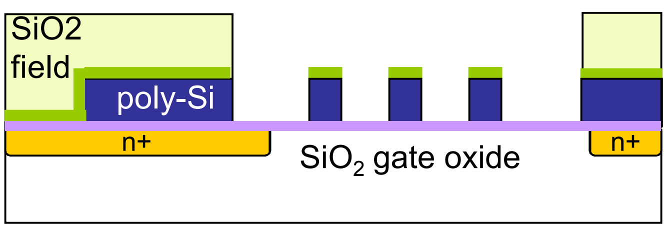
1. Electron beam lithography and form SiN hard mask

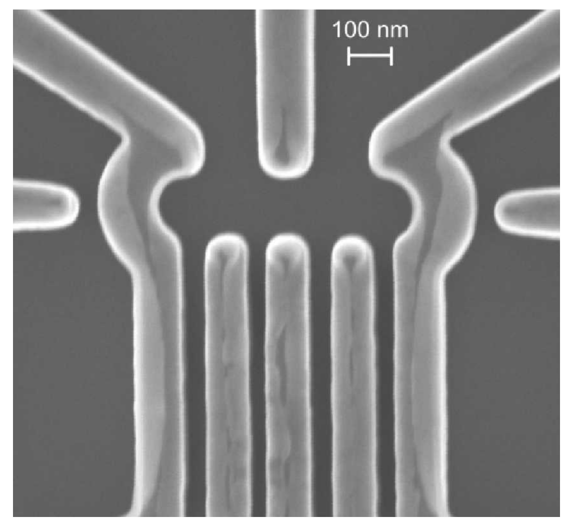




Nanolithography

1. Electron beam lithography and form SiN hard mask
2. Polysilicon patterning with plasma etch





Nanolithography

1. Electron beam lithography and form SiN hard mask
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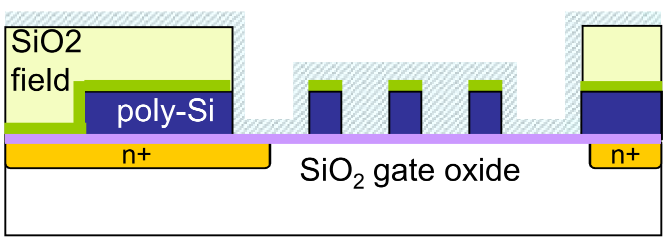
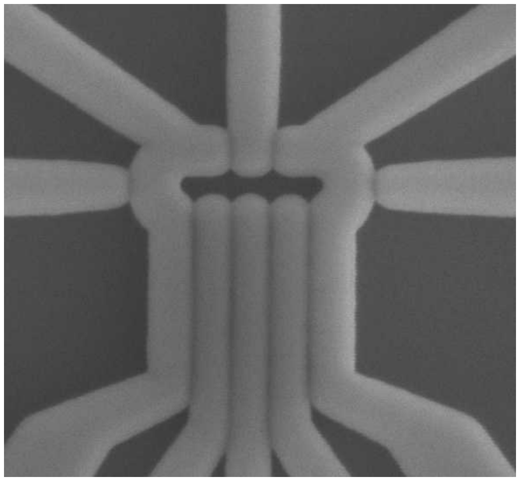
3. Deposit 2nd dielectric: atomic layer deposition of Al_2O_3





Nanolithography

1. Electron beam lithography and form SiN hard mask
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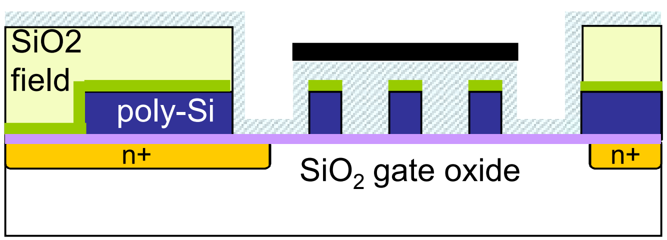
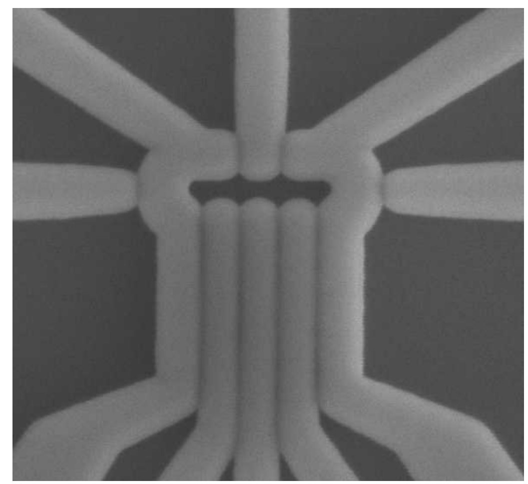
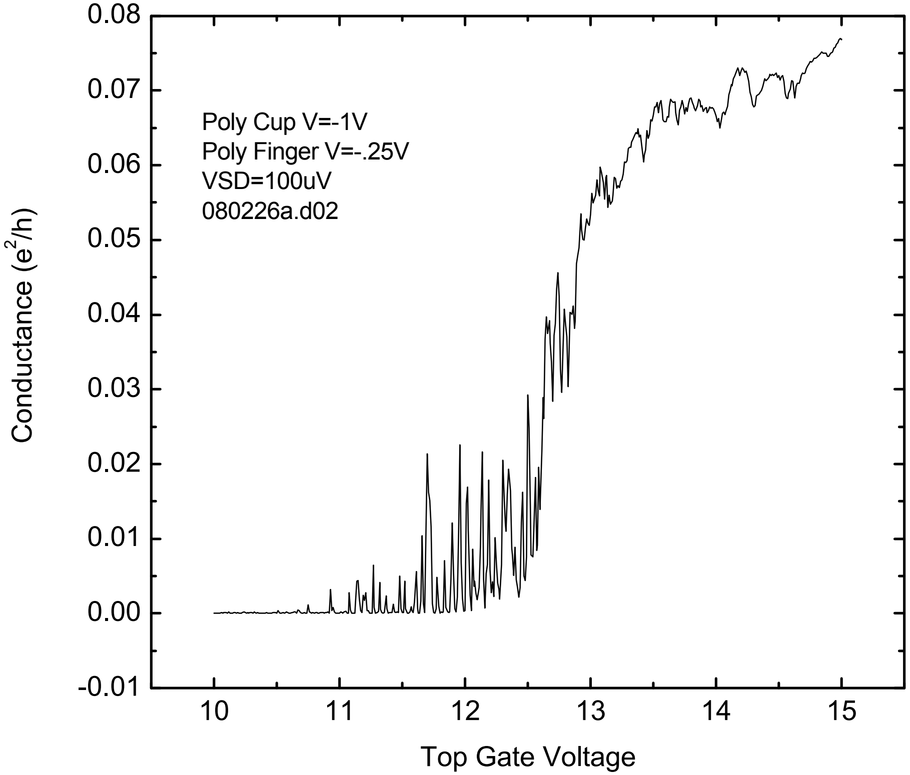
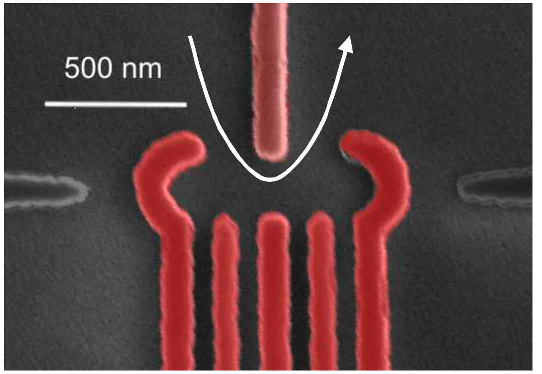
4. Al top gate





Quantum Dots





- Operate as large, oval quantum dot
- Transport can be stable over hours.
- Mobility drops after processing
- Coulomb blockade appears to be due to a series of dots, and disorder is a likely source of unintentional quantum dots.

Initial nanostructures have significant room for improvement

see poster by E. Nordberg

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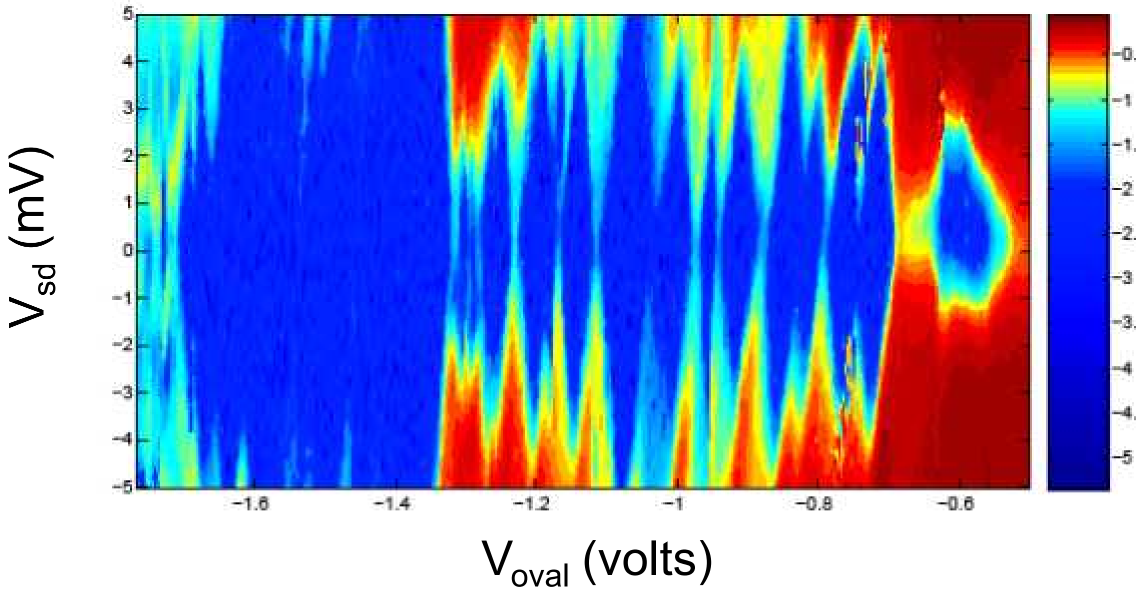
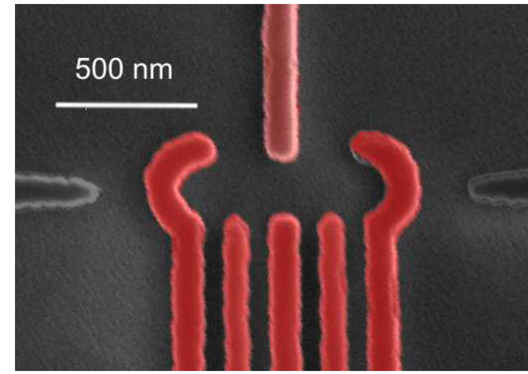
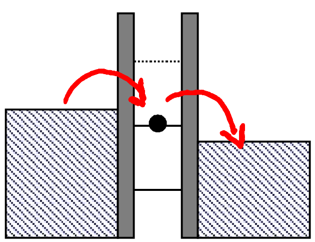
Coulomb Diamonds





Dot energy levels



Capacitances from diamonds

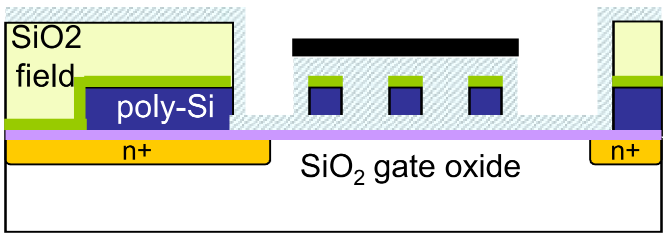
~20 aF to source and drain

~3 aF to oval gate

Even with disorder, regions of CB seem to be dominated by one dot

Why did the Mobility Decrease?

1. EBL
2. Polysilicon etch
3. atomic layer deposition of Al_2O_3
4. Al top gate



Damage leading to increased DIT

Incorporation of mobile charge

Additional scattering from fixed charge in SiO_2 or ALD

Undesired contamination

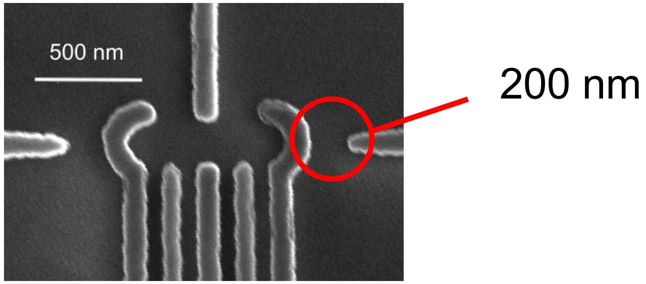
What can we do about disorder

Materials Improvement

- Reoxidation
- Forming Gas RTA
- Minimize plasma etch damage
- Al deposition

Size Reduction

Large gaps – disorder more important



Characteristic length-scale of disorder potential

Reduced Mobility after Metal Deposition

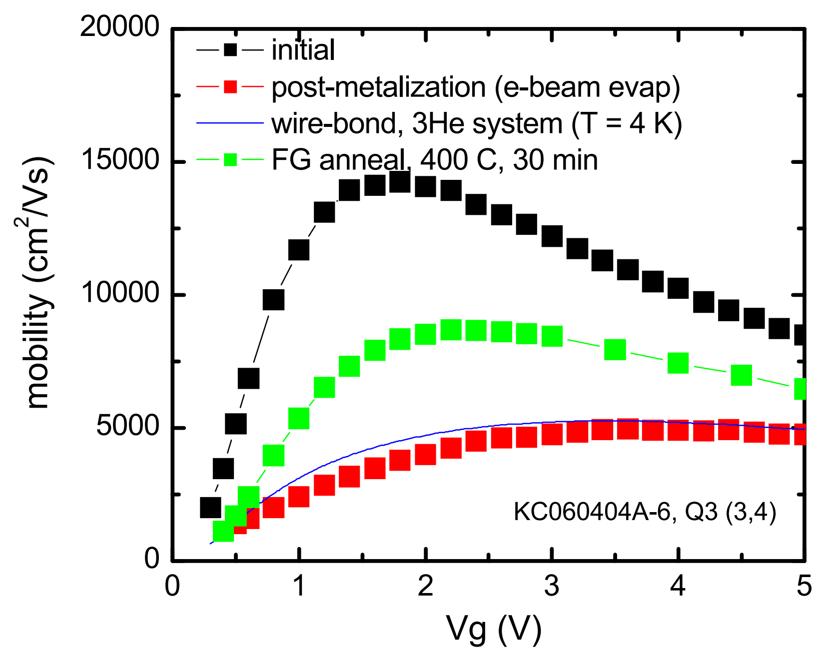
Size Reduction
Materials Improvement

Problem

Metal deposition technique can damage the oxide (x-rays and UV)

Solution

- Final step forming gas anneal can recover some damage
- Thermal and sputtering techniques are currently being employed



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Metal Failure on RTA/oxidation

Size Reduction

Materials Improvement

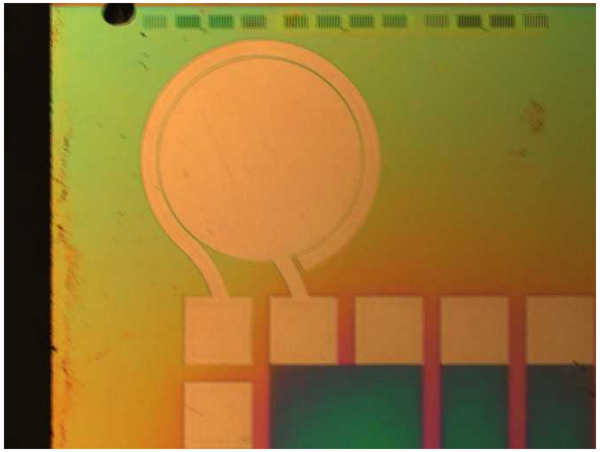
Problem

Thermal annealing with forming gas or re-oxidation can reduce damage. These anneals cause tungsten metal failure.

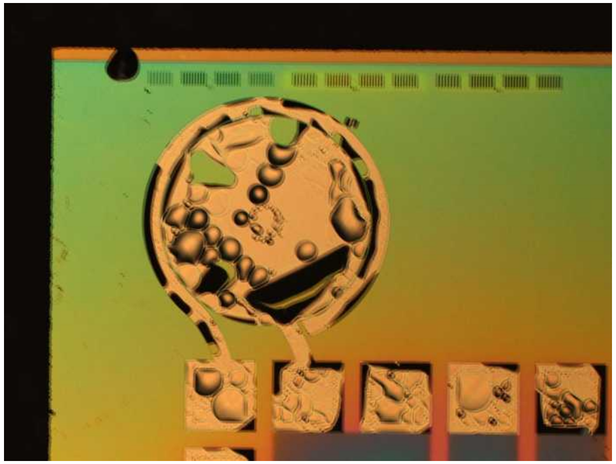
Solution

1. Completely remove metal after EBL of polysilicon depletion gates.
2. Perform high temperature operation
3. Deposit metal to make electrical contact

Contact pads before anneal



After 950 C anneal in forming gas



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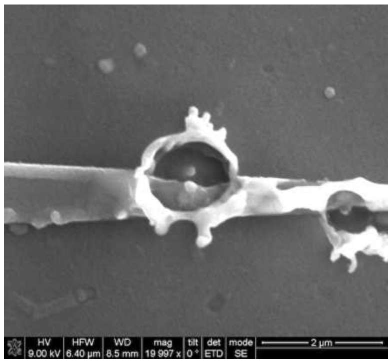
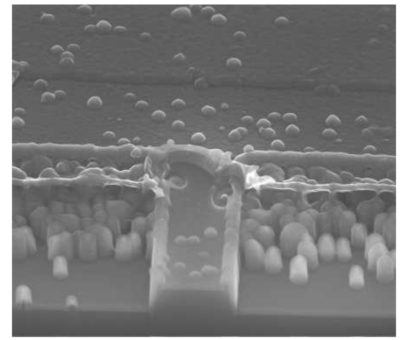
Processing Issues are getting Resolved with Work and Iteration

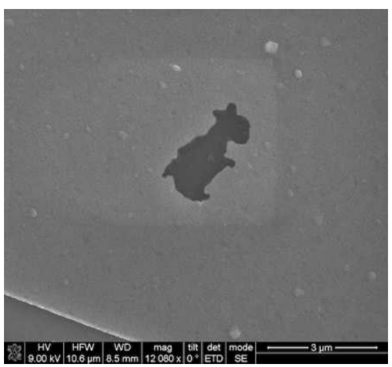
subsurface explosions



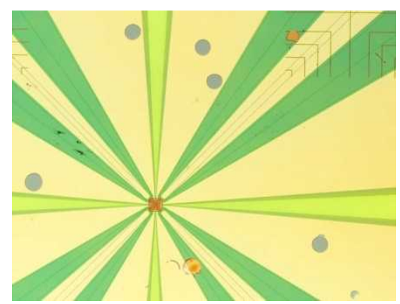
pillar formation



metal adhesion problems (non-partisan)



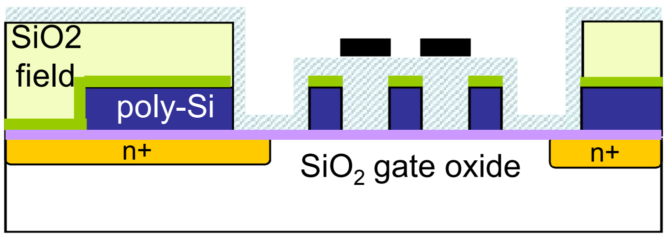
ALD etch undercut



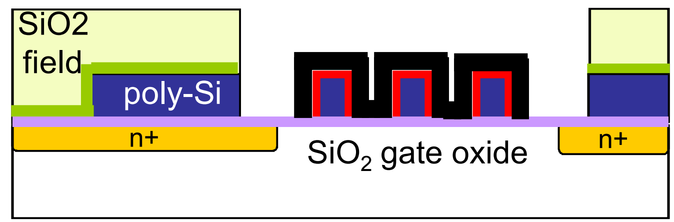
Multiple Designs to Address Disorder

Size Reduction
Materials Improvement

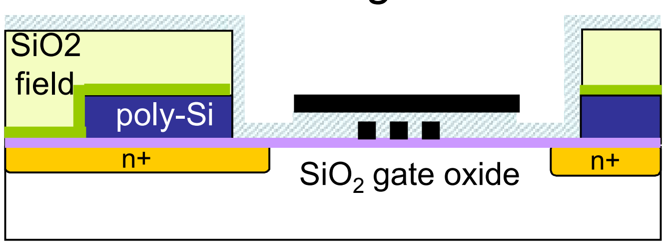
EBL poly / ALD / EBL Al
control nanostructure size



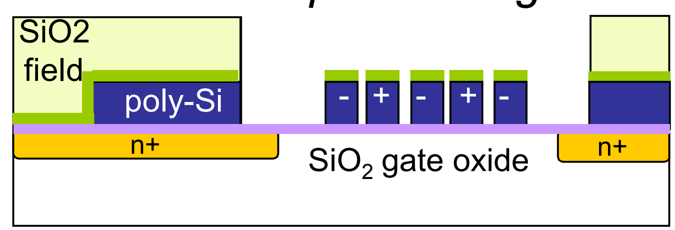
EBL poly / reox / Al gate
eliminate ALD



Double Al
reduce gate size



Single Poly Sheet
minimal processing

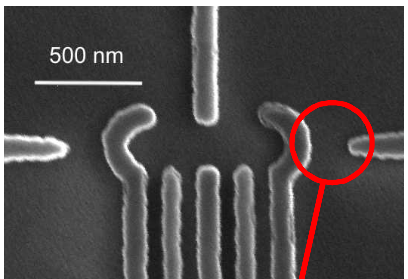


Minimizing Device Sizes

Size Reduction

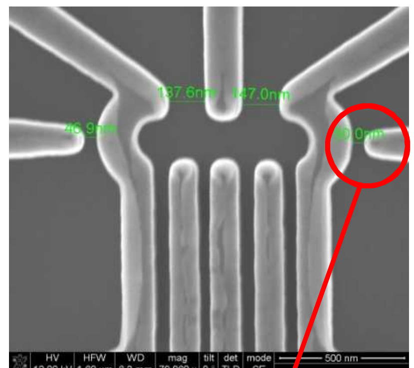
Materials Improvement

Large gaps – disorder more important



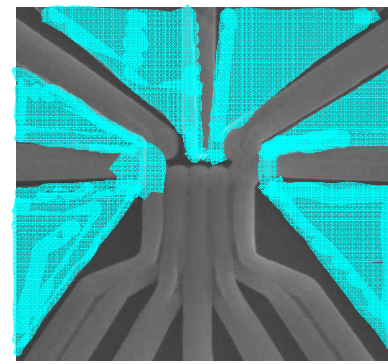
200 nm

Small gaps minimize role of disorder



50 nm

Patterned top gate



- Poly-silicon etching requires a *negative* tone ebeam resist.
  Limit: 70 nm lines, 50 nm gaps
- Ultimate small size: use Al liftoff and *positive* resist. Double Al device are being developed now.

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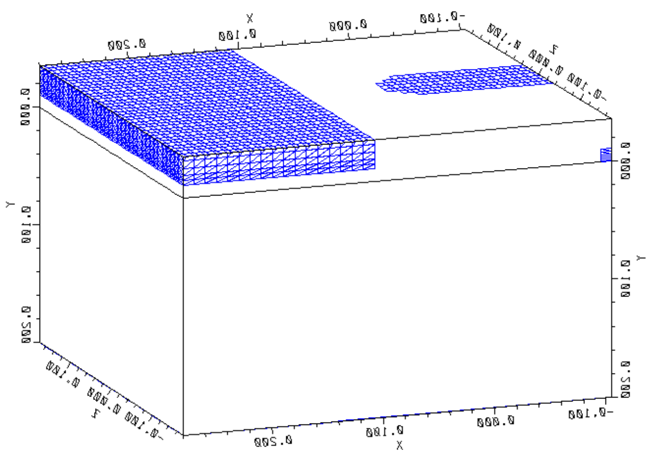
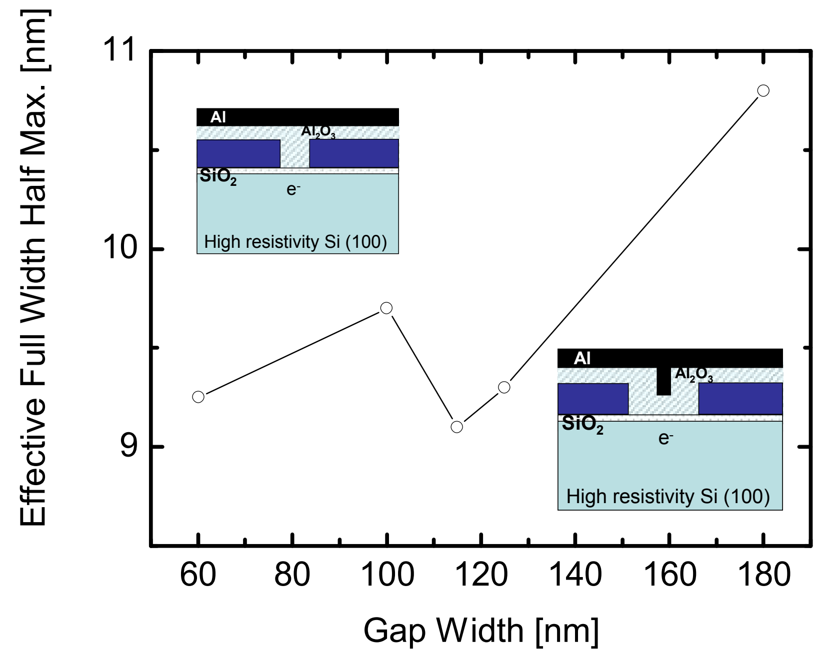
Modeling Al in Depletion Gap

Size Reduction

Materials Improvement



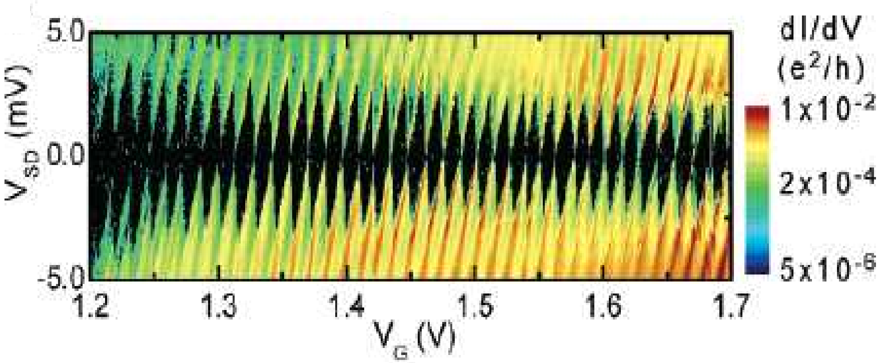
Semi-classical device modeling



- For a fixed ALD thickness, vary gap in quantum point contact
- Depth of potential is estimate by comparing to parabolic confinement
- Interplay between intermediate dielectric and feature size is very important

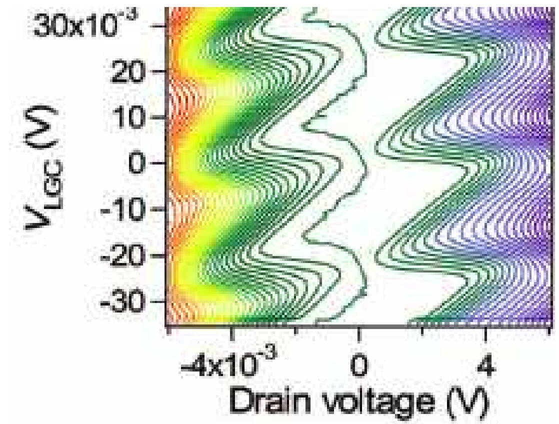
Si SETs

~ 40x60 nm lithographic dot - CQCT



Angus, et al. Nanoletters ***7****, 2051 (2007)*

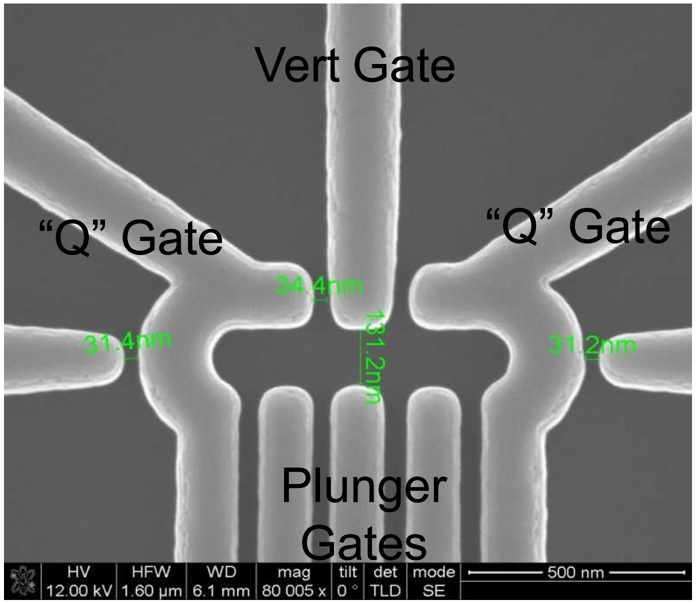
~ 20x70 nm lithographic dot
NTT and NIST

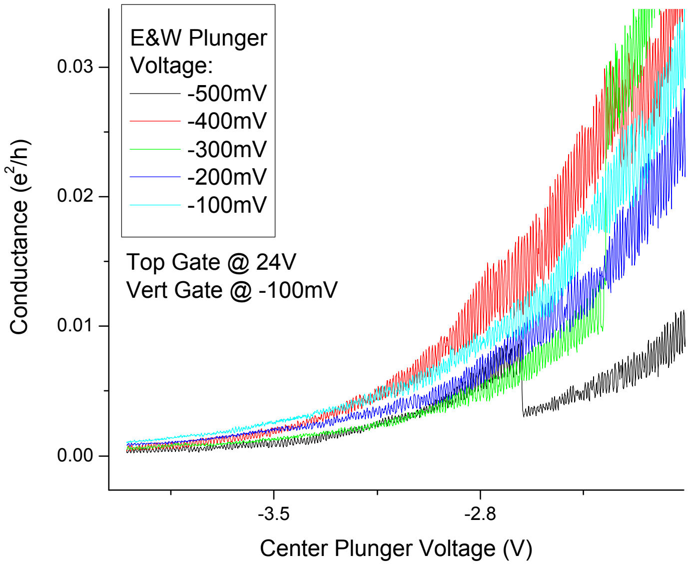


Fujiwara, et al. APL ***88****, 053121 (2006)*

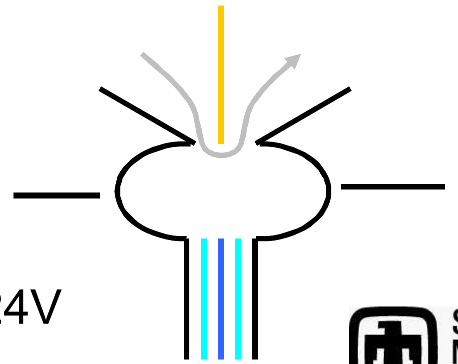
- Coulomb blockade, diamonds and double dots are well defined for very small devices.

Coulomb blockade recently observed in SNL dots





GND
Stepped
Swept
-100mV
Top Gate = +24V



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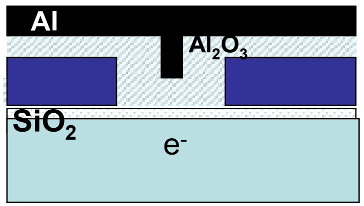
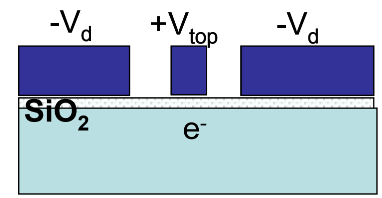
Quantum Point Contact

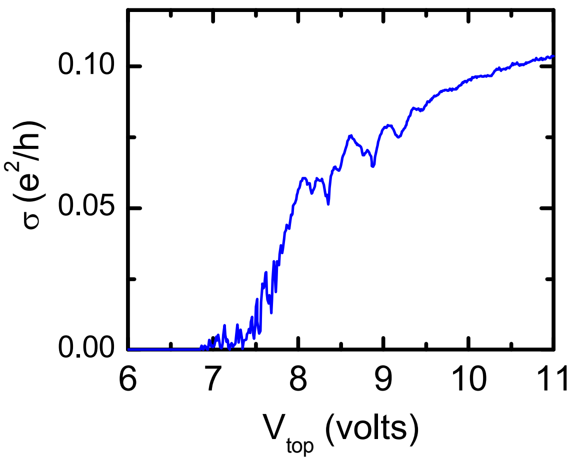
Double Top Gate QPCs



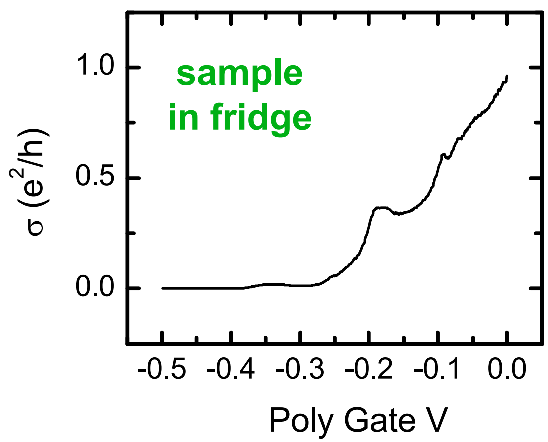
Single Poly Sheet



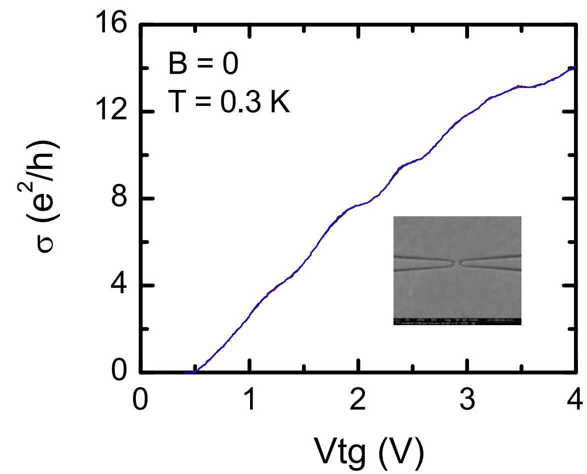
disorder case



reoxidized, RTA



mimimal processing



Avoiding and/or repairing damage will result in good devices

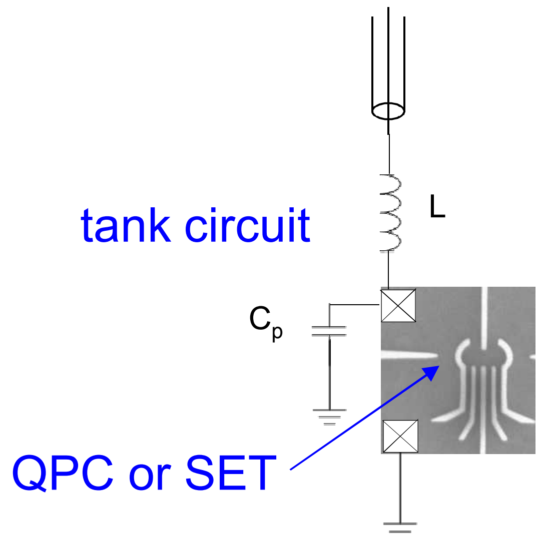
see poster by L. Tracy

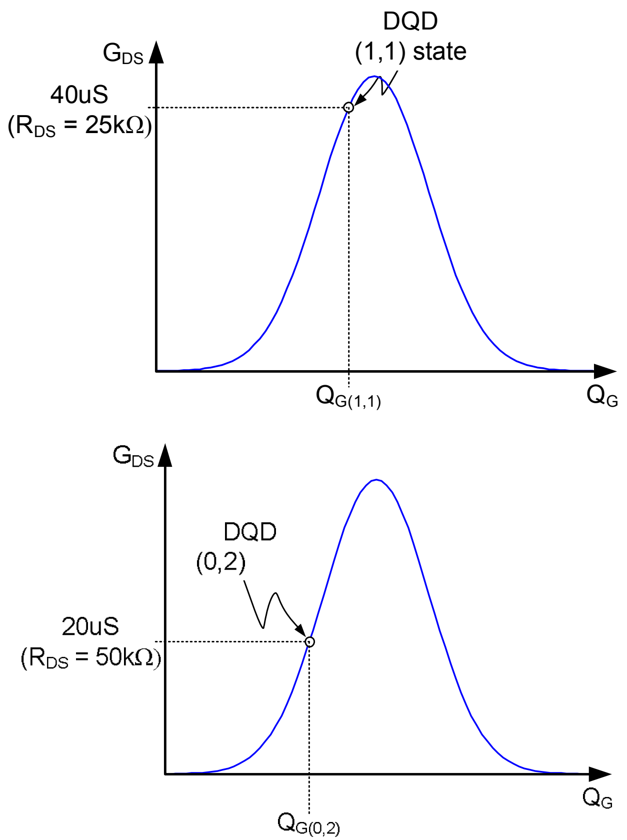
Outline

- 2DEGs in MOSFETs
- Nanoelectronics
  - Quantum dots
  - Disorder and fabrication
  - Quantum point contacts
- Silicon devices – fast detection

Fast Readout: rf-SET

Technique developed to beat large RC times resulting from high impedance devices (~50 KΩ) and large cable capacitance for cryostats (~1 nF)

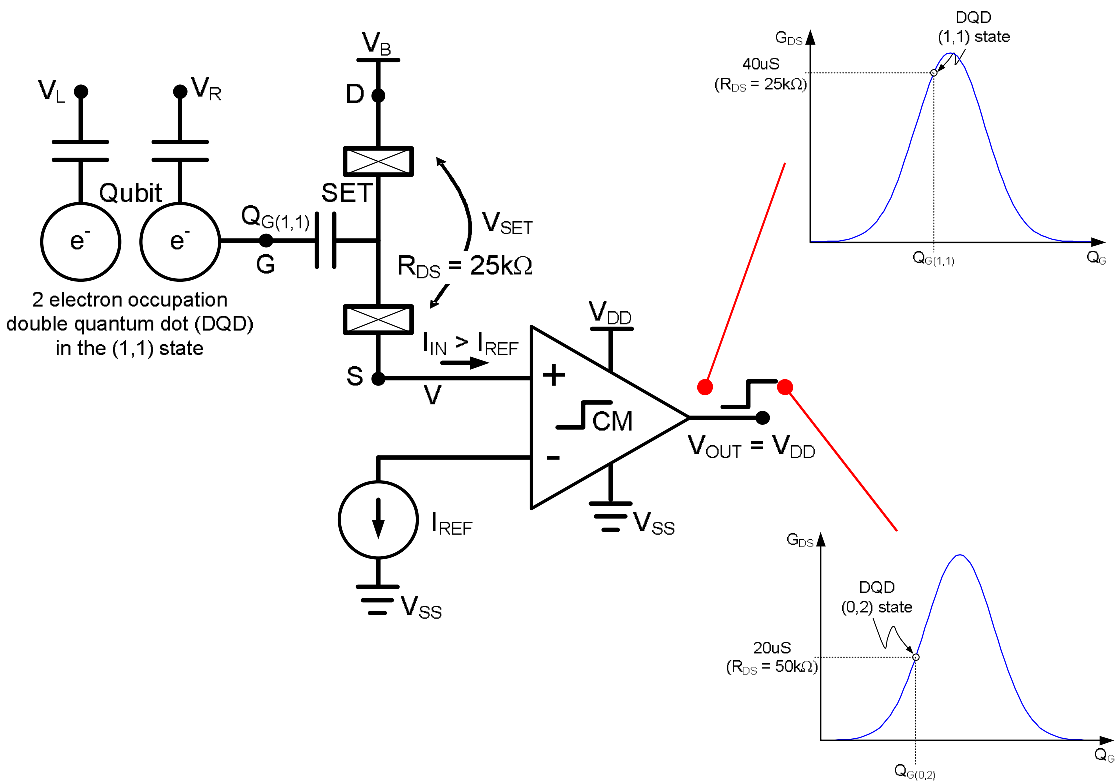




- Carrier frequency ~ 500 MHz
- Bandwidth ~ 10 MHz
- Averaging > 1 μsec

Digital Readout

- **Si CMOS foundry invites consideration of <u>integrated</u> circuit assisted solutions**



	RF-SET	CMOS Design
Speed	~1usec	~1nsec
Area	discrete	monolithic
Power (100mK)	~10uW	2nW (10ns sample time)
Power (4K)	~1mW	<1nW
state SNR	~60dB	~106dB

We can sense the SET conductance to obtain a CMOS digital output
(i.e. a 1-bit Analog–to-Digital conversion)

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T. Gurrieri, IEEE Nano (2008)

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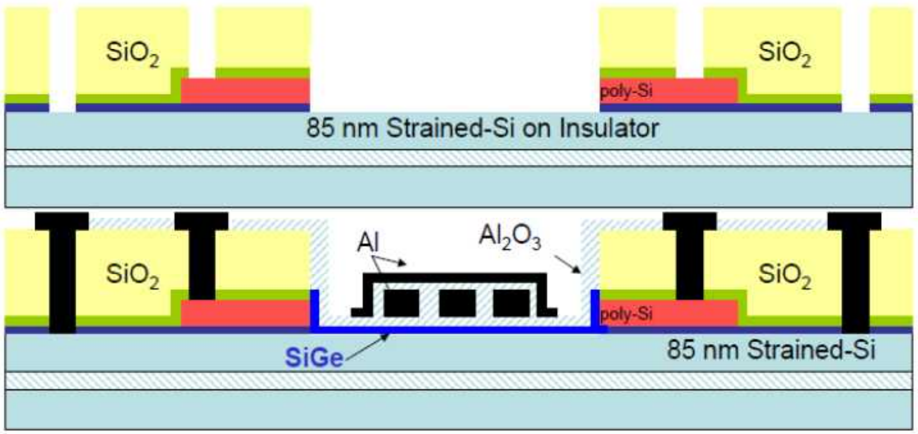
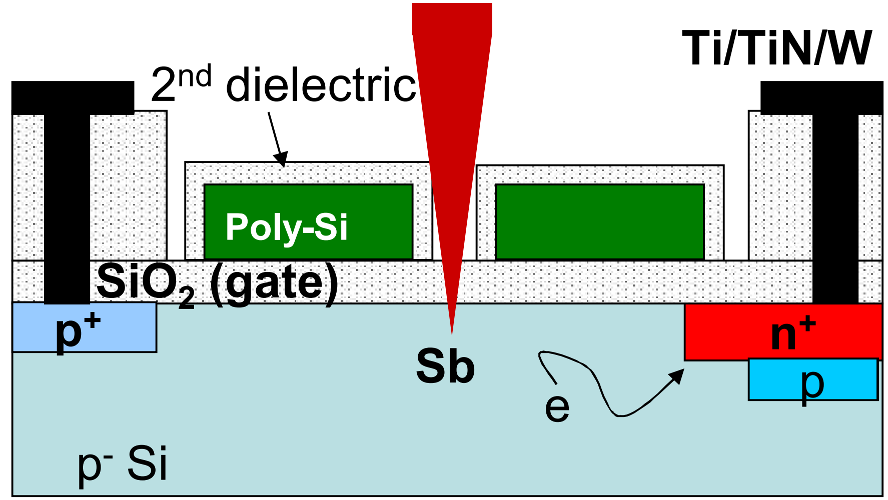
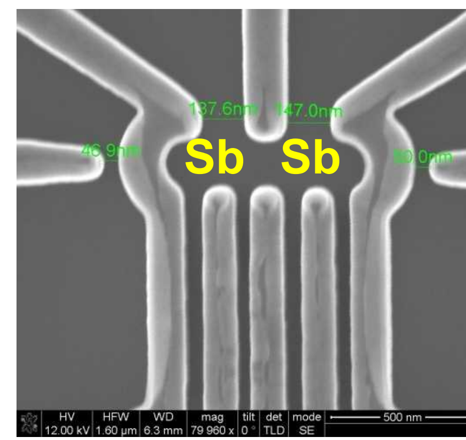
Quantum Information S&T

Flexible Si DQD Platform for 2nd Generation Devices





- Si DQD platform provides paths to SiGe or donor integration
- sSi-SiGe status
  - Little relaxation even after 1100C RTA
  - Peak mobility ~9,000 cm^2/V-s after SiO_2 FET process
- Donor-DQD status:
  - Mark I focused Sb ion beam
  - SIGMA ion detector proof-of-concept demonstrated
  - Initial integrated Ion detectors being tested



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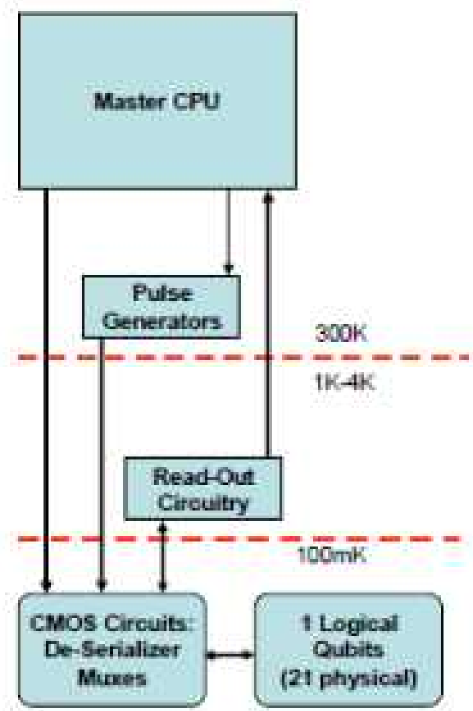
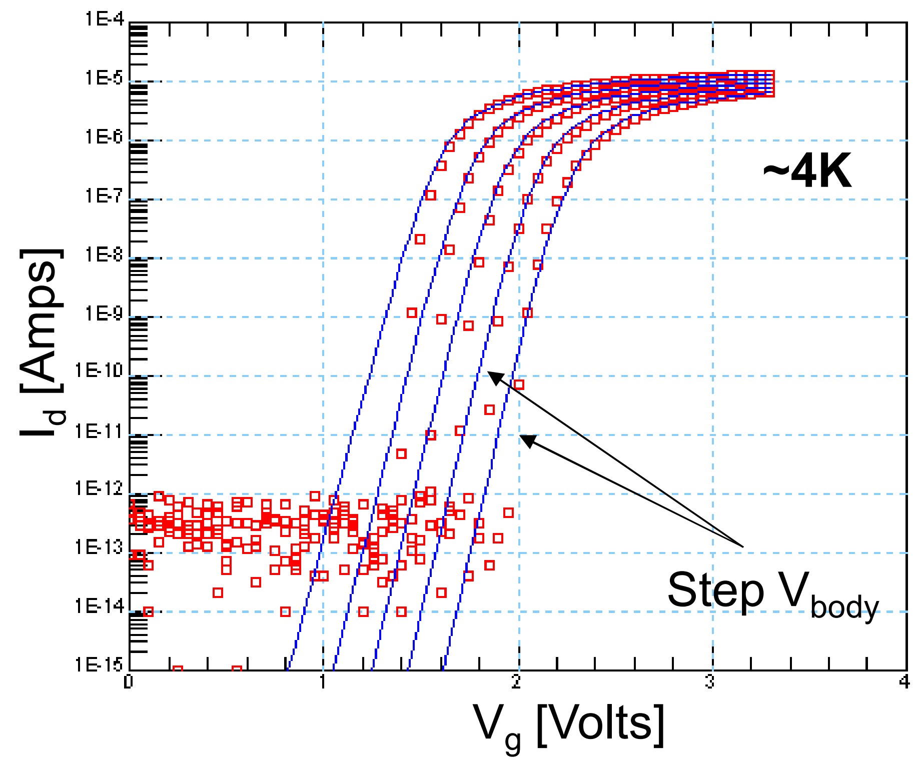
First element of electronics: cryo-CMOS



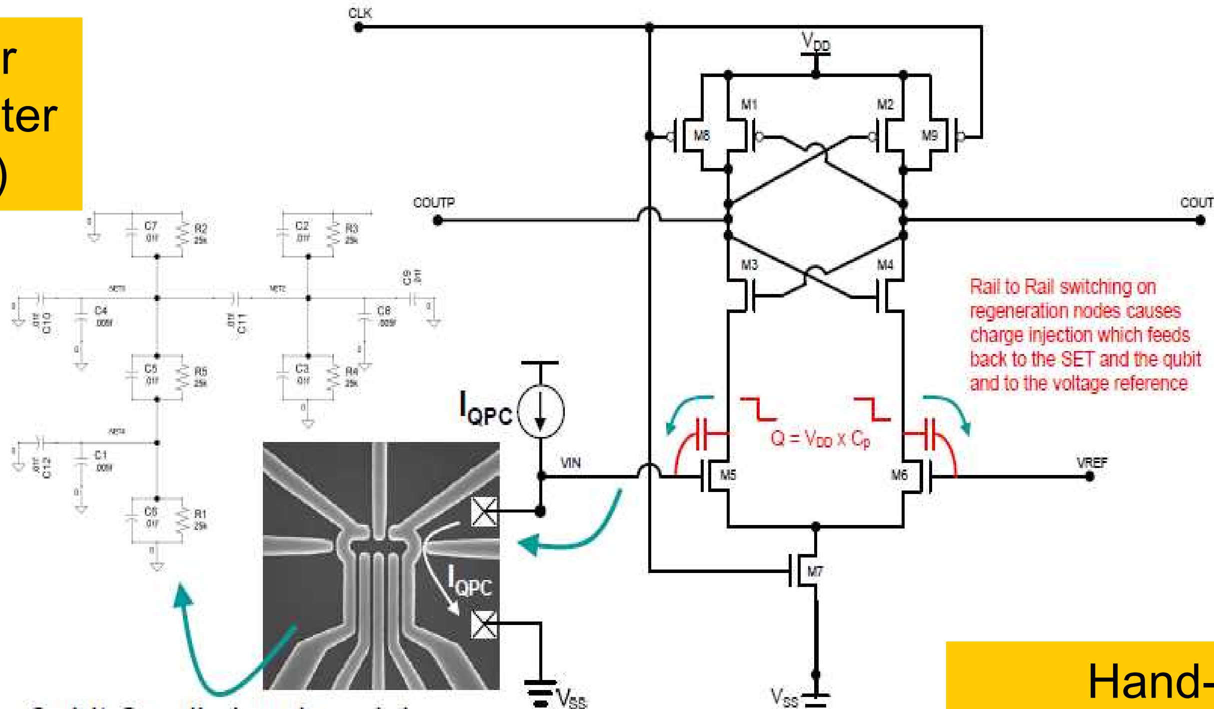


- Discrete CMOS elements are strongly temperature dependent
- Characterization and models needed for circuit design
- Some effects touch on phenomena not well addressed in CMOS community's standard software models
  - Metal insulator transition (sub-threshold & V_t)

Physical qubit & modeling team hand-offs

Second element of electronics: circuits

Circuit model for qubit & electrometer (several teams)



Qubit Small signal model

Introduced digital readout at first EAB

- **<u>Progress since last EAB</u>**
  - **Cryo model simulation**
  - **Current mode comparator examined to minimize feedback**
    - **Circuit fab'ed and now in test**

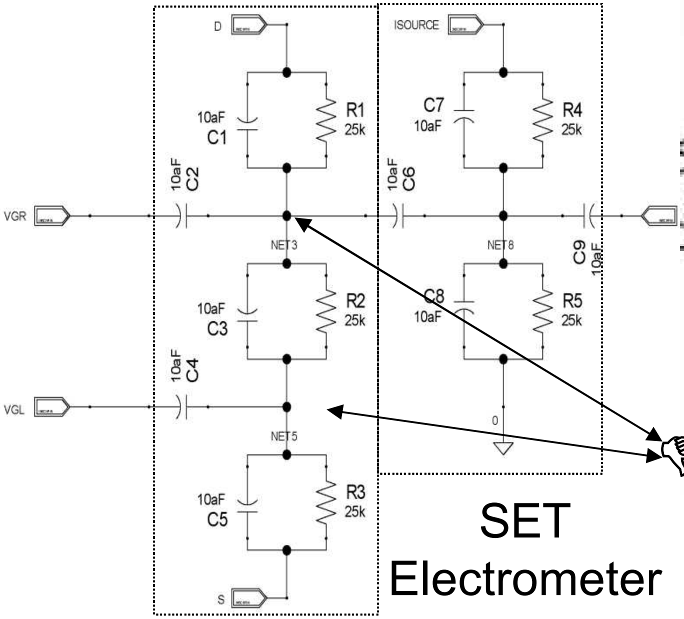
Hand-off: measurement performance & calibration of circuit models

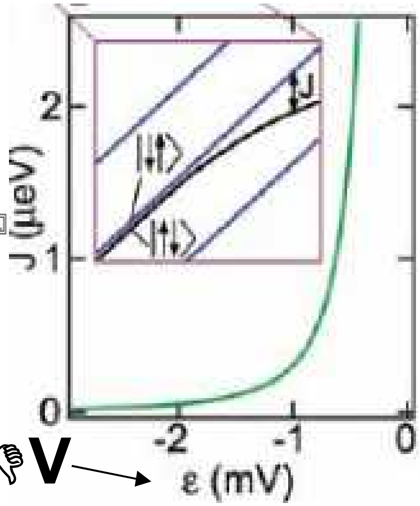
Third element of electronics: qubit models

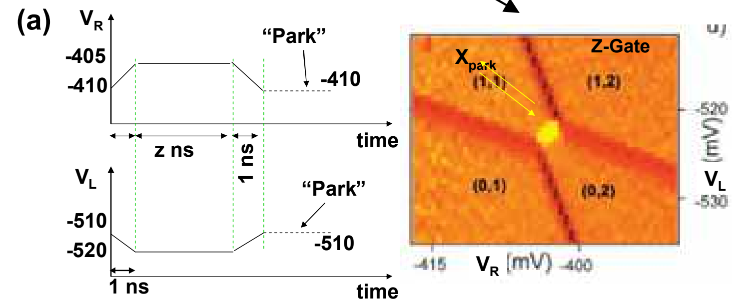
Quantum Information S&T

Petta et al.

Petta et al.







SET Electrometer

DQD

Ties with modeling & DQD teams

- Qubit small signal model being developed to bridge between hardware, classical electronics and architecture
- Several levels of abstraction required
  - Linear circuit element model for qubit, J(V) model & pulse control
- Initial voltage pulse sequences sketched for <u>Si native gate set</u>
- **Estimates of gate speed provided**
  - **assume 1e-4 precision constraint (hand-off)**

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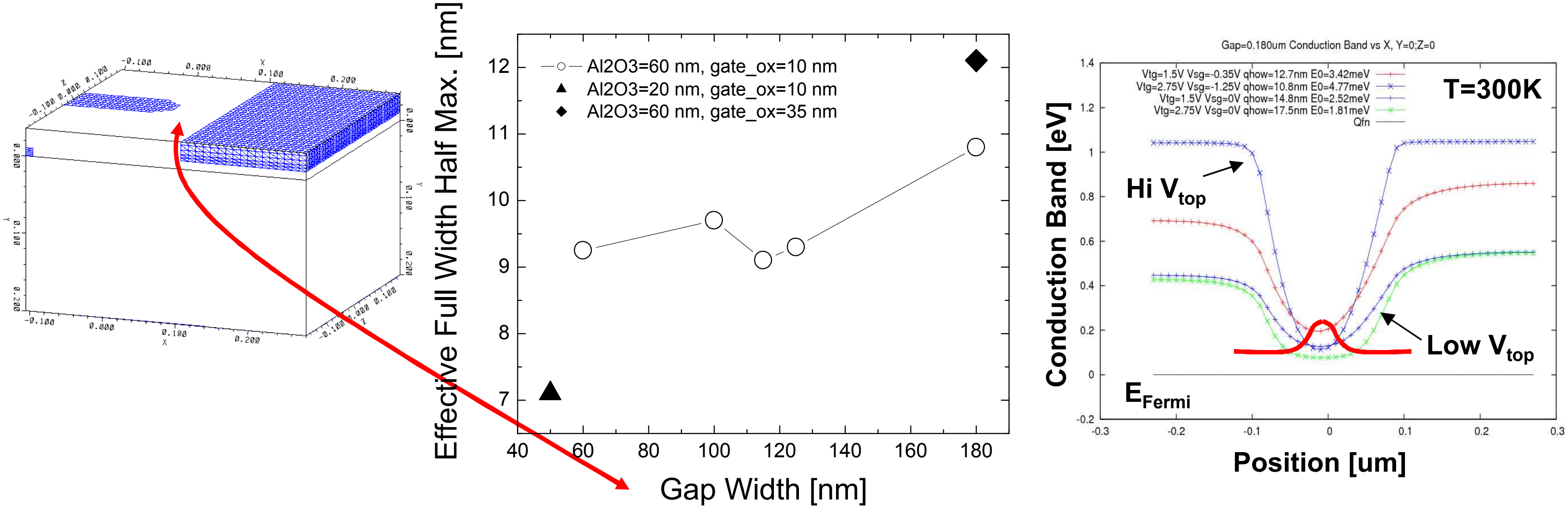
SETE Investigation of TCAD



- Previously mentioned TCAD simulations to optimize size
- Characteristic channel length (harmonic oscillator FWHM) for qualitative insight
- Where do semiclassical assumptions break down?
- SETE simulations in progress to calculate wavefunction in simple 2D cases
  - SETE needs modification for Si double top gate simulations

Decoherence Mechanism Survey

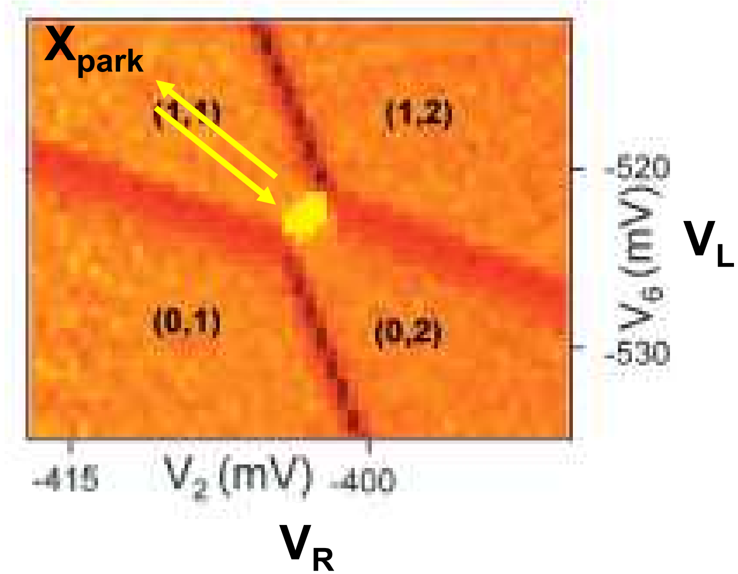
Error Source	T1 (xpt) [ms]	T2* (xpt) [ms]	T2 (xpt) [ms]	dynamic decoupling	Possible range of T2	T2 Estimate Used [ms]	Anticipated effect of noise on dynamic decoupled DQD Gate	Anticipated effect of noise on non-dynamic decoupled DQD gate
Donor spin: 28Si enriched	T1 ~ T2	0.63 ms (inhomogeneous Bz dominated)	60 ms	yes; XUXU; others being investigated	T2 > 60 ms suggested possible	60 ms	*gate error [alpha*X+beta*Y+gamma*Z] - always on* ;P(error)~1-exp(-time/T2);	*unknown X rotation - always on* ; P(error) ~ 1-exp{(-time/T2)-(time/T2*)^3};
Free electron: Valley splitting	NA	NA	NA	not considered	T2 > 60 ms suggested possible	T2~T1 > 60 ms	NA	negligible
donor: Magnetic noise			dependent on proximity to surface & surface condition	yes being investigated	0.01 ms < T2 < ~200 ms [ref 2]	effect not considered yet	*unknown direction [alpha*X+beta*Y+gamma*Z] - always on* ; P(error)~1-exp(-time/T2);	*unknown X rotation - always on* ; P(error)~1-exp{(-time/T2)-(time/T2*)^3};
DQD: Charge dephasing			~1-10 ns [GaAs]; ~200 ns [Si]	unknown	estimates in progress by other groups	T2 ~ 100 ns; factor = 100	unknown	*unknown Z rotation during Z-gate* ; gate error ~ 1-exp{-(Z-gate-time)/(T2*factor)};
Spin-orbit II (DP)			0.001 ms	unknown	0.0001ms < T2 < 0.01 ms	0.001 ms	unknown	*unknown X rotation during transport* ; P(error)~1-exp{(-time/T2)}
DQD: qubit leakage	T1 >> 12 hours					T1 >> 12 hours => neglible effect		

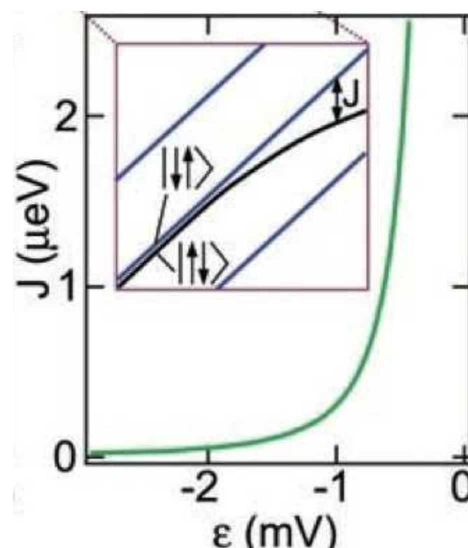
- Survey provided back-of-the-envelope estimates for decoherence induced error
- Dominant decoherence mechanism depends on gate & refocus (e.g., memory, Z-gate)
- Mechanisms of greatest apparent concern: exchange fluctuations & interface spins

Gate Issues

- Z-gate
  - J interactions
  - Sensitivity of Z gate to charge fluctuations
- Park position
  - Move qubit to non-interacting region
  - Sensitivity to stray noise/cross-talk
- X-gate
  - dB interactions, have to produce using induction loop
  - Also contains 2 Z-gates
- CPHASE
  - Modulated Z-gate
  - Modeling is critical, since no experimental demonstration, the only architecture information comes from theory.

Petta et al.

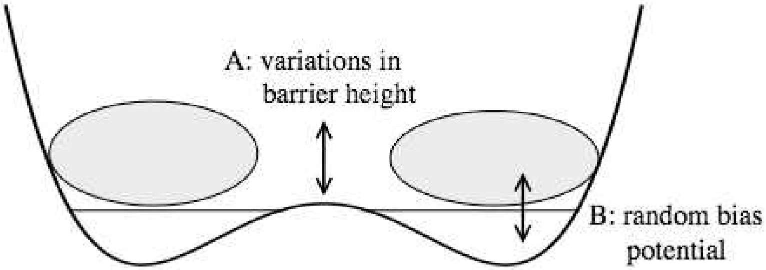




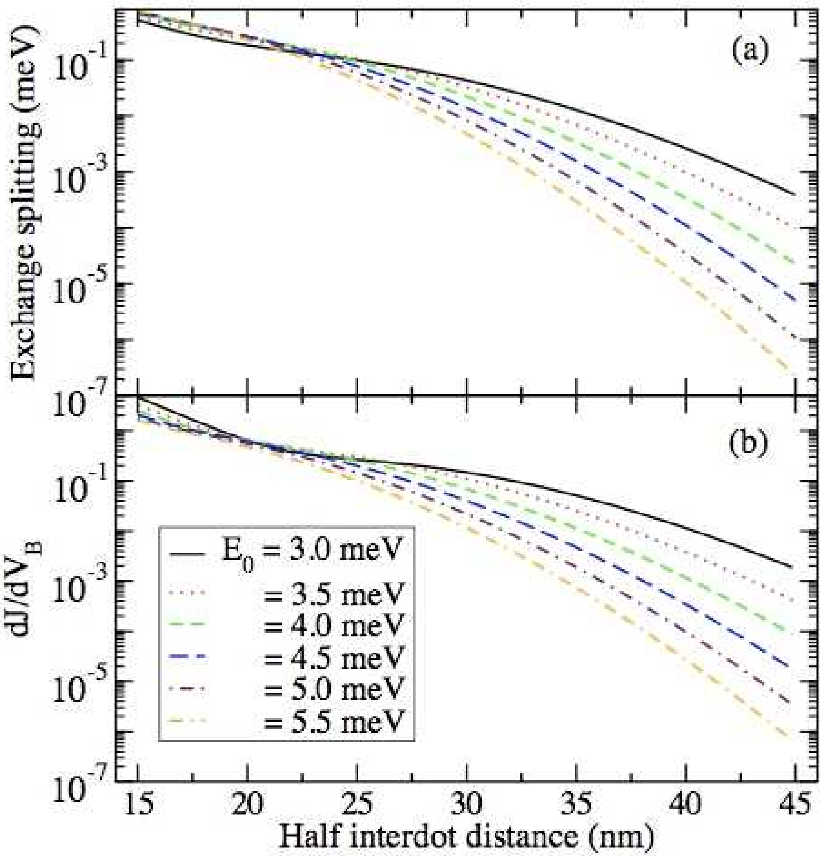
Exchange and Charge Fluctuations

- Seminal work by Hu and Das Sarma (2006)
- Examined DQD defined by
  $$V(x,y) = \frac{1}{2}m\omega^2\left[(x^2-L^2)^2/L^2+y^2\right]$$
- using HL states. Effects both in V_B and E_b
- Consider a faulty gate operation
  $$\int J dt/\hbar = \pi \qquad \int J dt/\hbar = \pi + \delta$$
- can lead to errors

$$\begin{pmatrix}\alpha_1\\ \alpha_2\end{pmatrix}\begin{pmatrix}\beta_1\\ \beta_2\end{pmatrix} \rightarrow \begin{pmatrix}\beta_1\\ \beta_2\end{pmatrix}\begin{pmatrix}\alpha_1\\ \alpha_2\end{pmatrix} + \frac{\alpha_1\beta_2-\alpha_2\beta_1}{\sqrt{2}}(1-e^{i\delta})|S\rangle$$



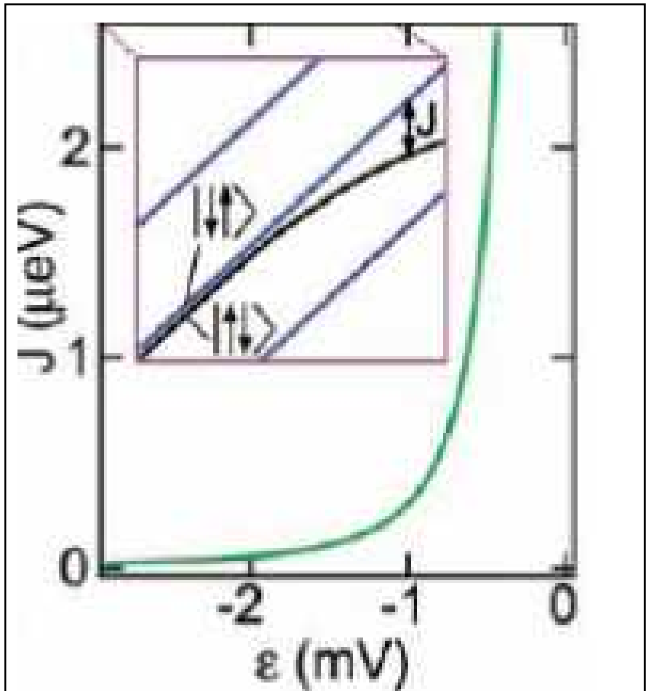
Effects of charge fluctuations on a double dot



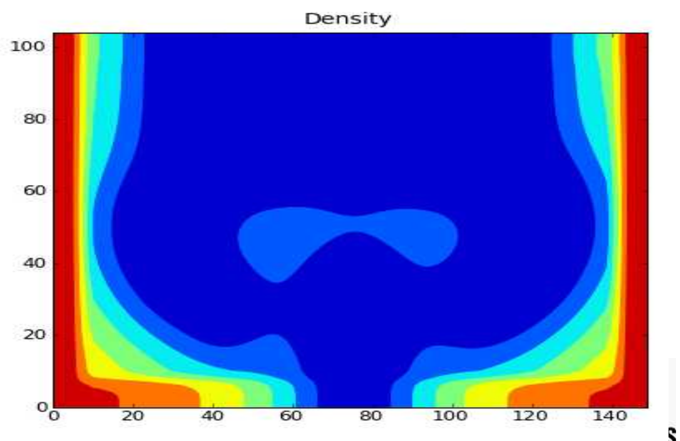
Exchange Energy

- Model of exchange energy dependence on gate bias necessary for gate model
  - Z-gate
  - CPHASE
- Model also needed to better estimate charge/voltage noise on DQD
  - can we "park" dot to turn off J?
  - How sensitive while Z-gate is on?
  - How much tuning is expected?
- Investigating SETE or NEMO+TCAD to model exchange energy effects

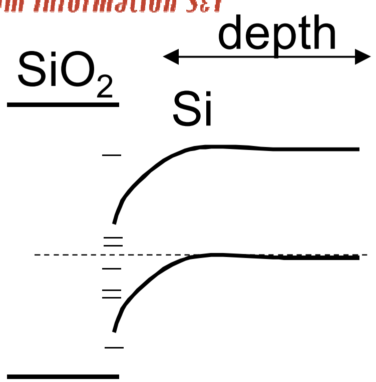
Hand off to DQD, electronics and logical qubit teams



Petta, Science 2005

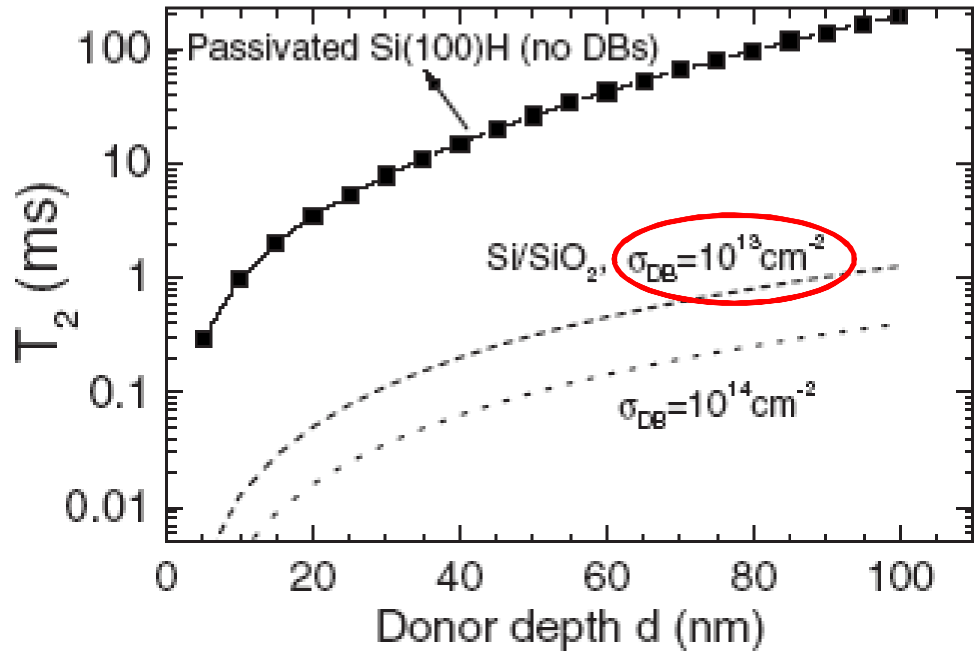


Dipole-dipole interactions "1/f magnetic noise"



Schenkel et al. APL

Sample	Interface	Peak depth (nm)	T_1 (ms)	T_2 (ms)
120 keV	Si/SiO_2	50	15±2	0.30±0.03
120 keV	Si—H	50	16±2	0.75±0.04
400 keV	Si/SiO_2	150	16±1	1.5±0.1
400 keV	Si—H	150	14±1	2.1±0.1



Better error model; needs measurements (e.g., Dit)

- Decoherence time decreases as it approaches surface
- Effect is not well understood
  - Current theory [de Sousa] requires spin density higher than suggested by D_{it} (unpaired electron traps)
  - 1/f character "magnetic noise" may have more general implications
- Also will consider different dynamic decoupling approaches (Grace/Witzel)

Sub-Project Summary

- Highlights
  - Standard TCAD & capacitance modeling effort assist device design/analysis
    - SETE investigation of TCAD semi-classical assumptions
  - Spin decoherence survey completed
    - Coarse estimates of error for each gate
    - Initial prioritization of theory efforts suggested
  - Capacitance model being integrated into small signal model
  - NEMO3D code adapted for Red Storm (future donor-dot coupling)
  - New hires (R. Rahman & W. Witzel) & collab. w/ M. Grace (SNL/CA)
  - Collaborations with many groups in this area beginning to ramp-up

Silicon Qubit Summary

- Highlights
  - MOSFET 2D electrons have high mobility and allow several approaches to nanostructures
  - Quantum point contact and dot measurements are starting
    - Improve disorder through decreasing size and improving materials
  - Experimental platform is available for custom nanoelectronics
  - Integration with CMOS devices is underway.

- Collaborations
  - Mark Eriksson (U. Wisconsin)
  - Australian CQCT
  - Sankar Das Sarma (U. Maryland)
  - Steve Lyon (Princeton)
  - Neil Zimmerman (NIST)
  - Jason Petta (Princeton)

Hue changes based on Sandia logo